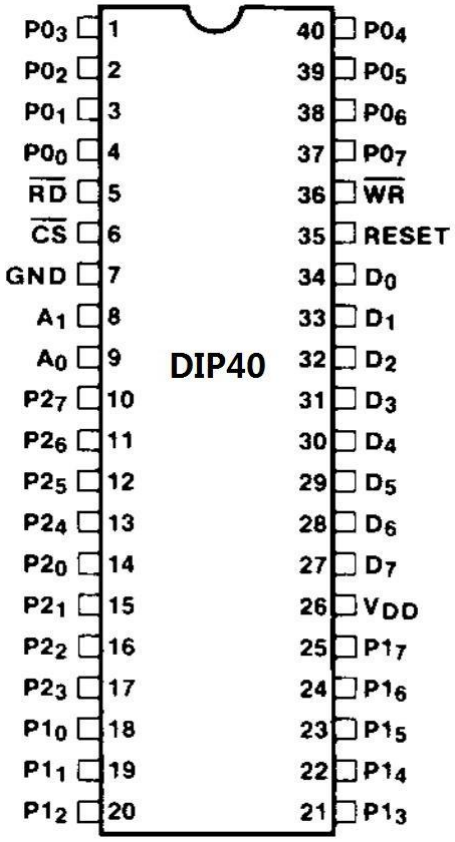
1. DESCRIPTION

The XD71055 is a low-power CMOS programmable parallel interface unit for use in microcomputer systems.Typically,the unit's three I/O ports interface peripheral devices to the system bus.

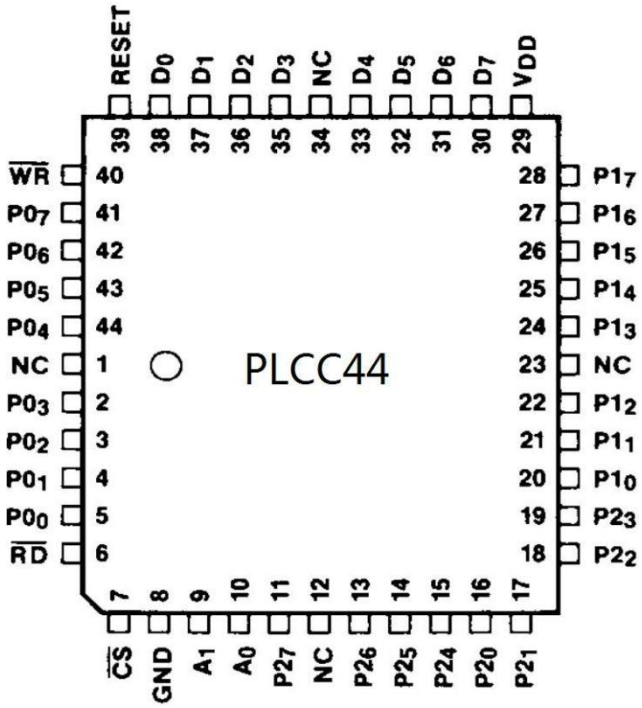
2. FEATURES

- Three 8-bit I/O ports
- Three programmable operation modes
- Bit manipulation command
- Microcomputer compatible
- Single +5V ±10% power supply
- Industrial temperature range:-40 to +85℃
- 8MHz and 10MHz

3. PIN CONFIGURATIONS



(Top View)



4. PIN IDENTIFICATION

Symbol	Function
$\overline{CS}$	Chip select input
GND	Ground
A1,A0	Address inputs 1 and 0
$P0_7$-$P0_0$	I/O port 0,bits 7-0
$P1_7$-$P1_0$	I/O port 1,bits 7-0
$P2_7$-$P2_0$	I/O port 2,bits 7-0
IC	Internally connected
V_{DD}	+5V
D_7-D_0	I/O data bus
RESET	Reset input
$\overline{WR}$	Write strobe input
$\overline{RO}$	Read strobe input
NC	No connection

5. PIN FUNCTIONS

D_7-D_0(Data Bus)

D_7-D_0 make up an 8-bit,three-state,bidirectional data bus.The bus is connected to the system data bus.It is used to send commands to the XD71055 and to send data to and from the XD71055.

$\overline{CS}$(Chip Select)

The $\overline{CS}$ input is used to select the XD71055.When $\overline{CS}$=0,the XD71055 is selected and the states of the D7-D0 pins are determined by the $\overline{RD}$ and $\overline{WR}$ inputs.When $\overline{CS}$=1, the XD71055 is not selected and its data bus is high-impedance.

$\overline{RD}$(Read Strobe)

The $\overline{RD}$ input is set low when data is being read from the XD71055 data bus.

$\overline{WR}$(Write Strobe)

The $\overline{WR}$ input should be set low when data is to be written to the XD71055 data bus.The contents of the data bus are written to the XD71055 at the rising edge (low to high) of the $\overline{WR}$ signal.

A1,A0 (Address)

The A1 and A0 inputs are used in combination with the $\overline{RD}$ and $\overline{WR}$ signals to select one of the three ports or the command register.A1 and A0 are usually connected to the lower two bits of the system address to the lower two bits of the system address bus(table 1).

RESET(Reset)

When the RESTE input is high,the XD71055 is reset.The group 0 and the group 1 ports are set to mode 0(basic I/O port mode).All port bits are set to mode 0 (basic I/O port mode).All port bits are cleared to zero and all ports are set for input.

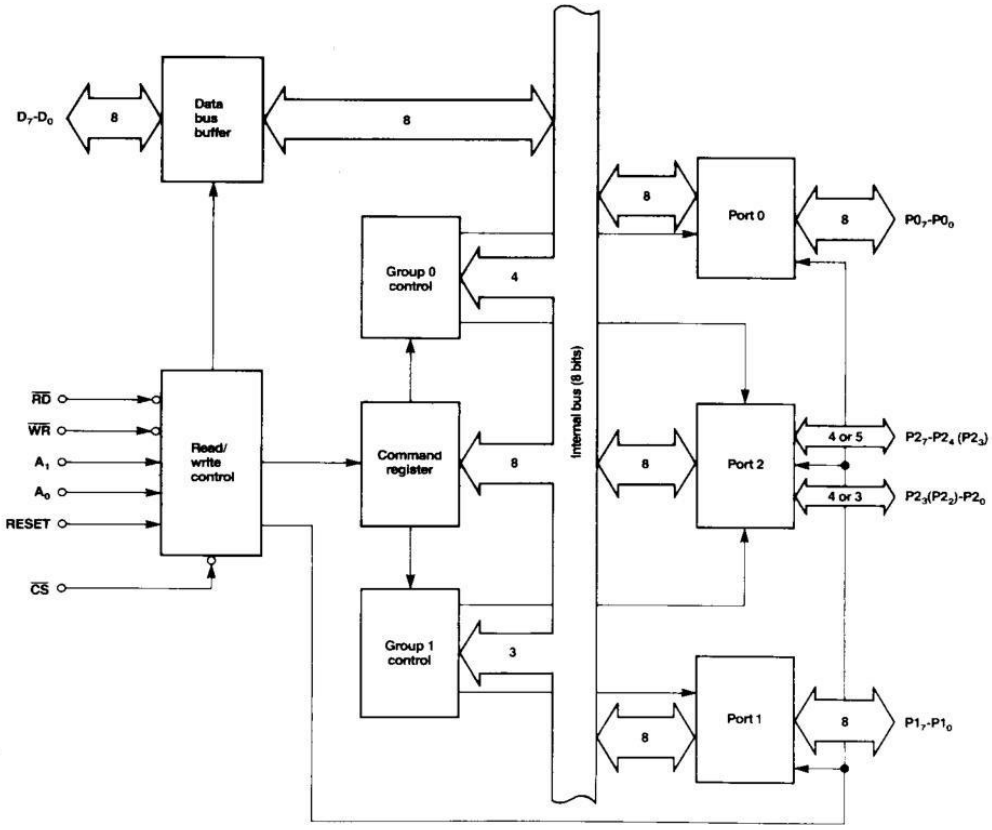
P07-P00,P17-710,P27-P20 (ports 0,1,2)

Pins P07-P00,P17-P10,and P27-P20 are the port 0,1,and 2 I/O pins,bits 7-0,respectively.

IC(Internally Connected)

Pins marked IC are used internally and must be left unconnected.

6. BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

Ports 0,1,2

The XD71055 has three 8-bit I/O ports,referred to as port 0,and port 2.These ports are divided into two groups,group 0 and group 1.The groups can be in one of three modes,mode 0,mode 1,and mode 2.Modes can be set independently for each group.

When port 0 is in mode 0,port 0 and the four upper bits of port 2 belong to group 0,and port 1 and the four lower bits of port 2 belong to group 1.When port 0 is in mode 1 or 2,port 0 and the 5 upper bits of port 2 belong to group 0 and port 1 and the three lower bits of port 2 belong to group 1.

Command Register

The host writes command words to the XD71055 in this register.These commands control group 0 and group 1.Note that the contents of this register cannot be read.

Group 0 Control and Group 1 Control

These blocks control the operation of group 0 and group 1.

Read/Write Control

The read/write control controls the read/write operations for the ports and the data bus in response to the $\overline{RD}$,$\overline{WR}$,$\overline{CS}$, and address signals.It also handles RESET signals and the A0,A1 address inputs.

Data Bus Buffer

The data bus buffer latches information going to or from the system data bus.

8. ABSOLUTE MAXIMUM RATINGS

T_A=25℃

Power supply voltage,VDD	-0.5 to +7.0V
Input voltage,VI	-0.5 to VDD +0.3V
Output voltage,VO	-0.5 to VDD +0.3V
Power dissipation,PD_{MAX}	500mW
Operating temperature,T_{OPT}	-40℃ to +85℃
Storage temperature,T_{STG}	-65℃ to +150℃

9. DC CHARACTERISTICS

Limits					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Conditions**
Input high voltage	V_{IH}	2.2	V_{DD}+0.3	V	
Input low voltage	V_{IL}	-0.5	0.8	V	
Output high voltage	V_{OH}	0.7V_{DD}		V	IOH=-400μA
Output low voltage	V_{OL}			V	IOL=2.5mA
Darlington drive current	I_{OH}	-1	-4	mA	See test setup diagram
Input leakage current high	I_{LIH}		10	μA	VI=VDD
Input leakage current low	I_{LIL}		-10	μA	VI=0V
Output leakage Current high	I_{LOH}		10	μA	VO=VDD
Output leakage Current low	I_{LOL}		-10	μA	VO=0V
Supply current (dynamic)	I_{DD1}		10	mA	Normal operation
Supply current (standby)	I_{DD2}		50	μA	Inputs:RESET=0.1V Others=VDD-0.1V Outputs:Open

10. CAPACITANCE

T_A=25℃;V_{CC}=0V

Limits					
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Conditions**
Input capacitance	C_I		10	pF	fc =1MHz Unmeasured pins returned to 0V
I/O capacitance	C_{IO}		20	pF	

11. AC CHARACTERISTICS

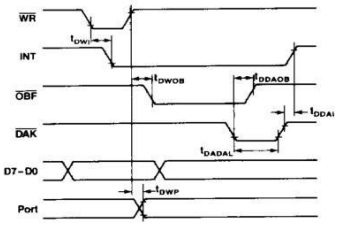
		8 MHz Limits		10 MHz Limits			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Conditions**
Read Timing							
A1,A0,$\overline{CS}$ set-up to $\overline{RD}\downarrow$	t_{SAR}	0		0		ns	
A1,A0,$\overline{CS}$ hold from RD↑	t_{HRA}	0		0		ns	
$\overline{RD}$ pulse width	t_{RRL}	160		150		ns	
Data delay from $\overline{RD}\downarrow$	t_{DRD}		120		100	ns	C_L=150pF
Data float from $\overline{RD}\uparrow$	t_{FRD}	10	85	10	60	ns	C_L=20pF R_L=2kΩ
Read recovery time	t_{RV}	200		150		ns	
Write Timing							
A1,A0,$\overline{CS}$ set-up to $\overline{WR}\downarrow$	t_{SAW}	0		0		ns	
A1,A0,$\overline{CS}$ set-up to $\overline{WR}\uparrow$	t_{HWA}	0		0		ns	
$\overline{WR}$ pulse width	t_{WWL}	120		100		ns	
Data set-up to $\overline{WR}\uparrow$	t_{SDW}	100		100		ns	
Data hold from $\overline{WR}\uparrow$	t_{HWD}	0		0		ns	
Write recovery time	t_{RV}	200		150		ns	
Other Timing							
Port set-up time $\overline{RD}\downarrow$	t_{SPR}	0		0	350	ns	C_L=150pF
Port hold time from RD↑	t_{HRP}	0		0		ns	
Port set-up time to STB↓	t_{SPS}	0		0		ns	
Port hold time from STB↑	t_{HSP}	150		150		ns	
Port delay time from WR↑	t_{DWP}		350		200	ns	C_L=150pF
$\overline{STB}$ pulse width	t_{SSL}	350		100		ns	
$\overline{DAK}$ pulse width	t_{DADAL}	300		100		ns	
Port delay time from DAK↓(mode 2)	t_{DDAP}		300		150	ns	C_L=150pF
Port float time from $\overline{DAK}\uparrow$(mode 2)	t_{FDAP}	20	250	20	250	ns	C_L=20pF R_L=2kΩ

$\overline{OBF}$ set delay from WR ↑	t_{DWOB}		300		150	ns	C_L=150pF
$\overline{OBF}$ clear delay from DAK↓	t_{DDAOB}		350		150	ns	
IBF set delay from STB↓	t_{DSIB}		300		150	ns	
IBF clear delay from $\overline{RD}$↑	t_{DRIB}		300		150	ns	
INT set delay from DAK↑	t_{DDAI}		350		150	ns	
INT clear delay from $\overline{WR}$↓	t_{DWI}		450		200	ns	
INT set delay from STB↑	t_{DSI}		300		150	ns	
INT clear delay from RD↓	t_{DRI}		400		200	ns	
RESET pulse width	t_{RESET1}	50		50		μs	During right after power-on
	t_{RESET2}	500		500		ns	During operation

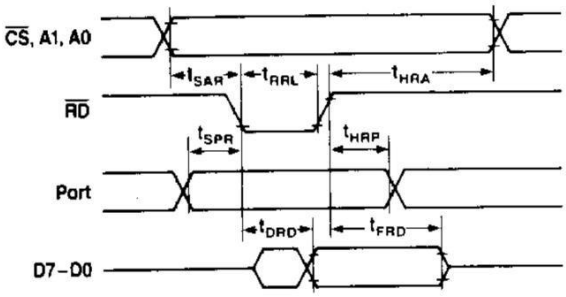
12. TIMING WAVEFORMS

AC Test Waveform

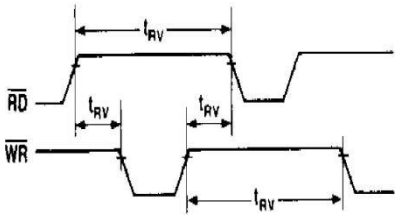
Mode 1:Output



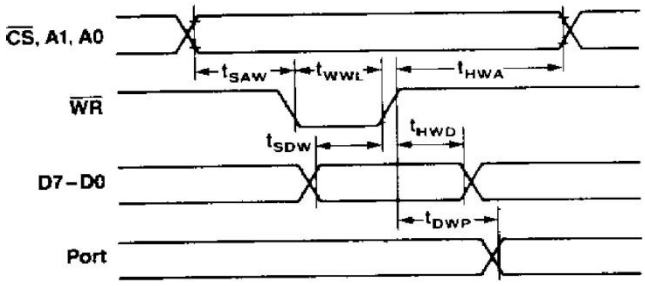
Timing Mode 0:Input



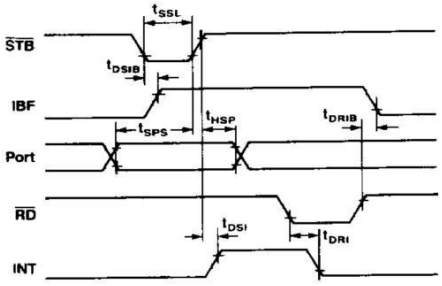
Recovery Time



Mode 0:Output



Mode 1:Input



13. TIMING WAVEFORM

Mode 2

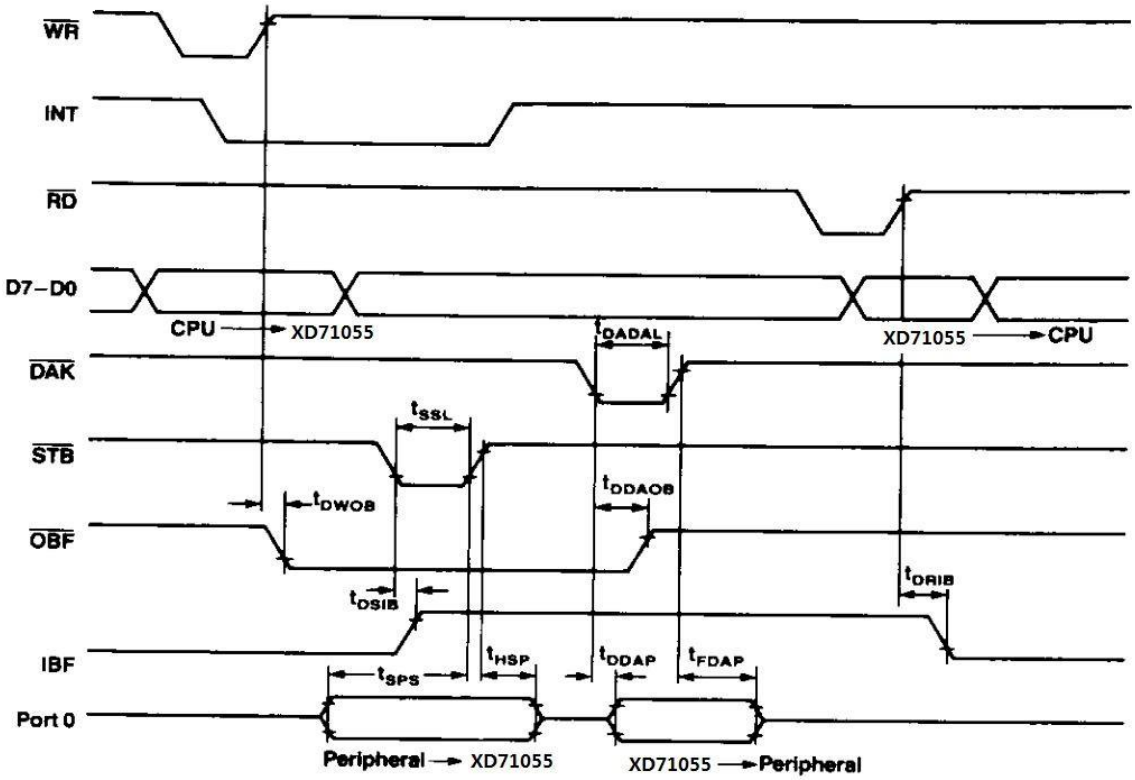


Figure 1.Mode Select Command Word

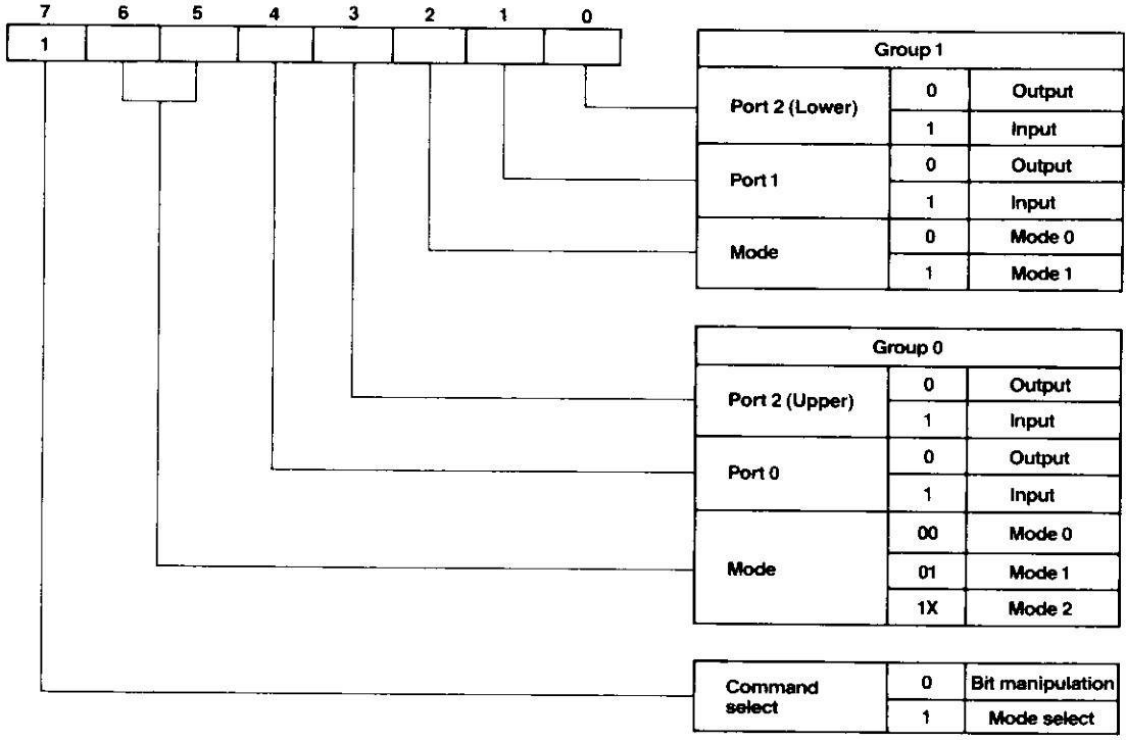


Figure 2.Bit Manipulation Command Word

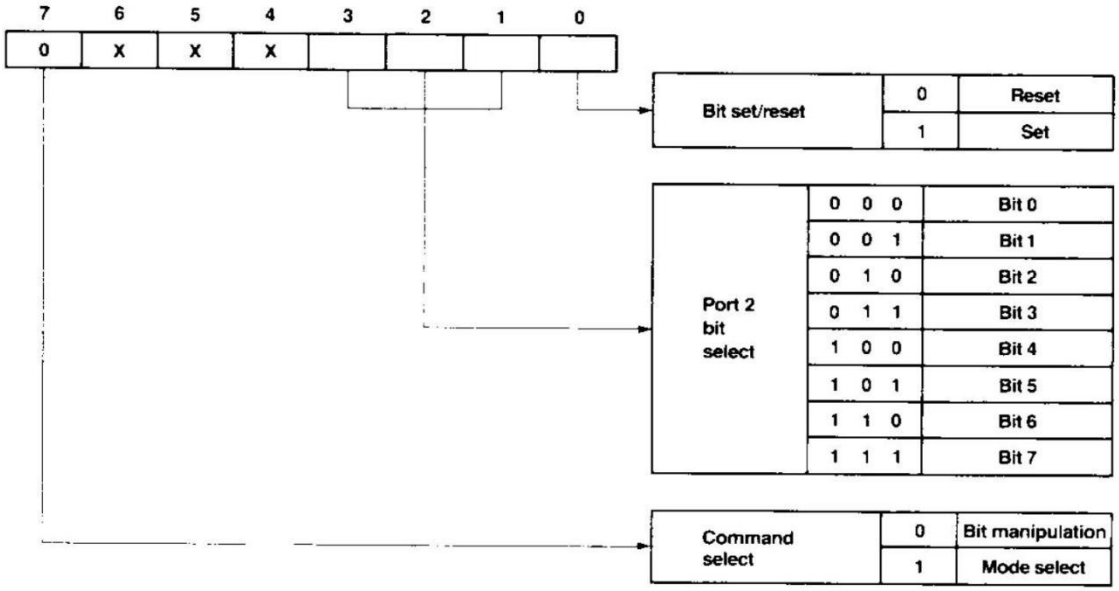


Figure 3.Bit Manipulation Command Word Example

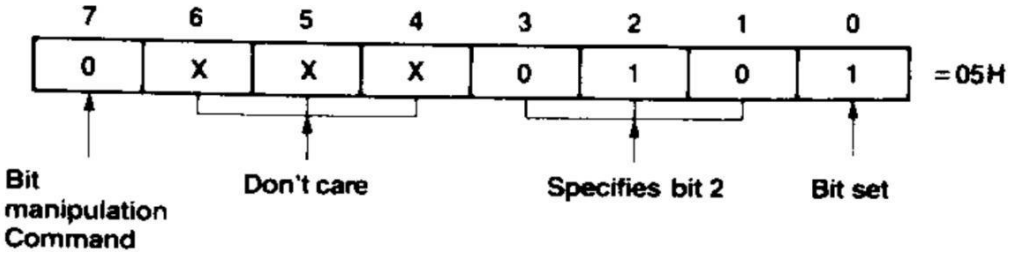


Figure 4.Mode 0

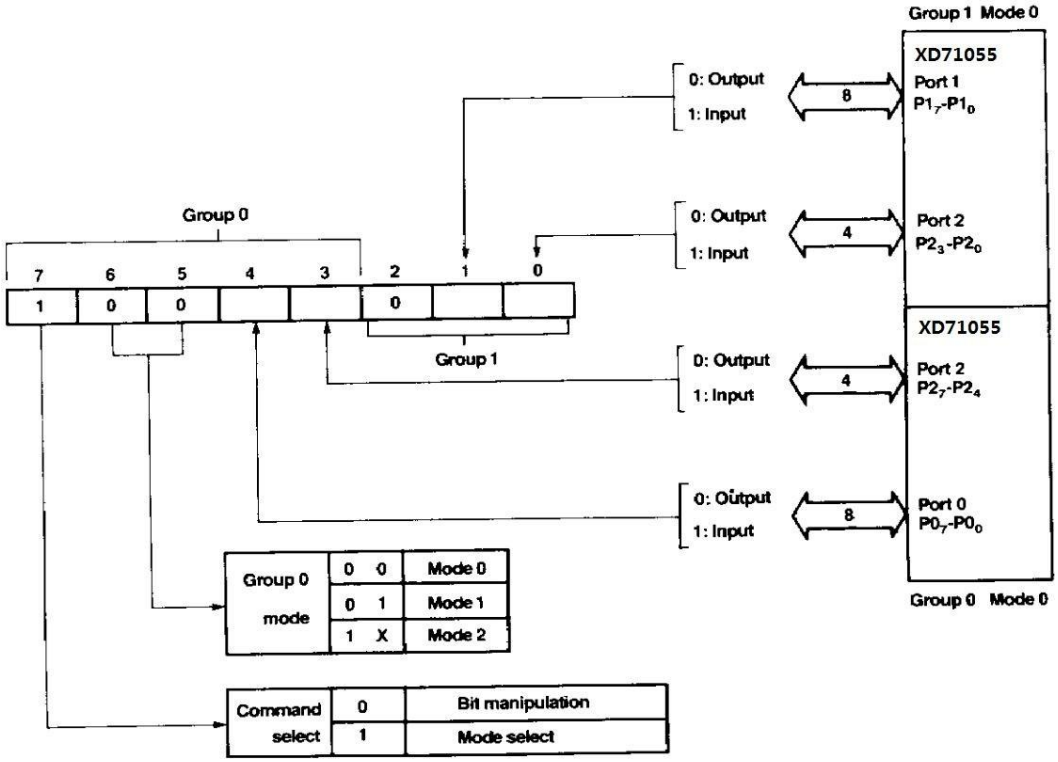


Figure 5.Mode 0 Input Timing

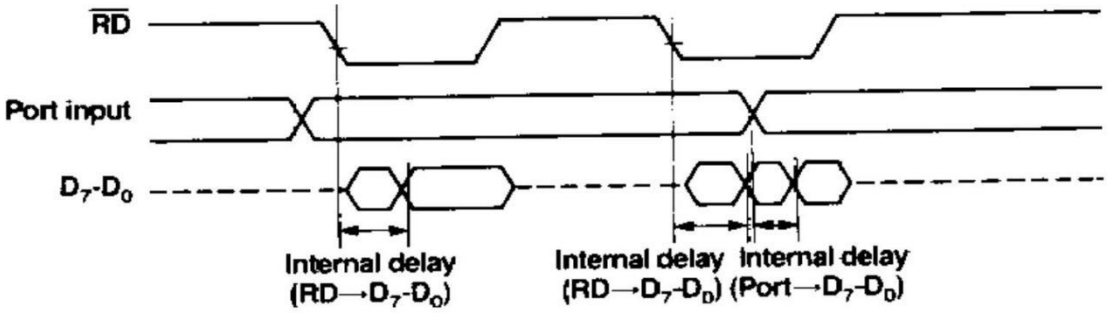


Figure 6.Mode 0 Output Timing

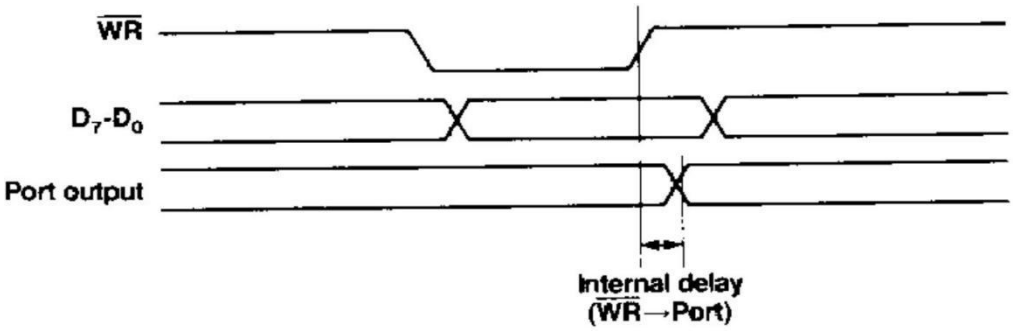


Figure 7.A/D Converter Connection Example

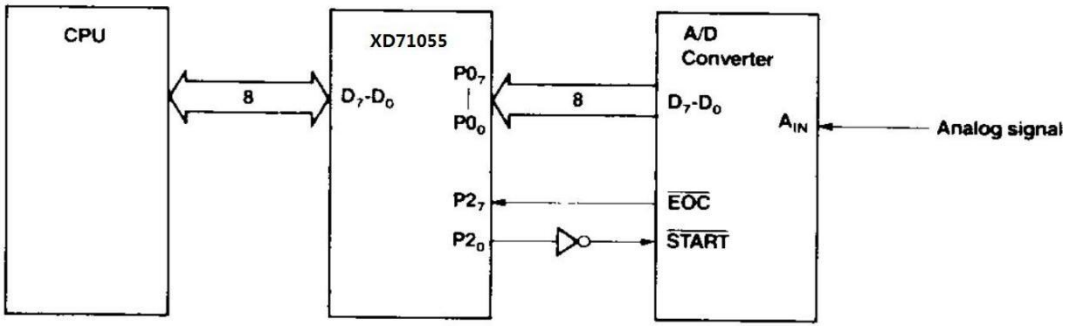
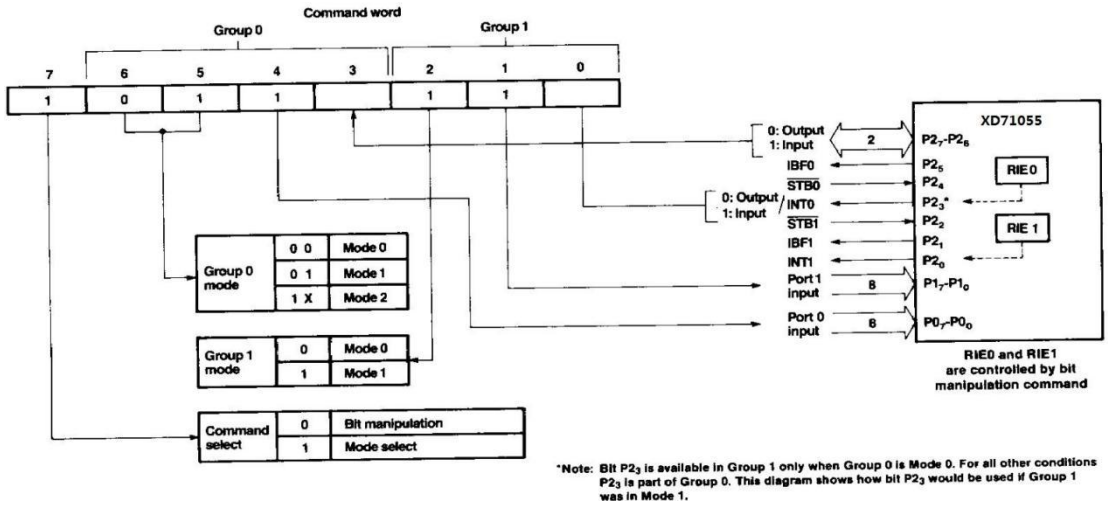


Figure 8.A/D Converter Example

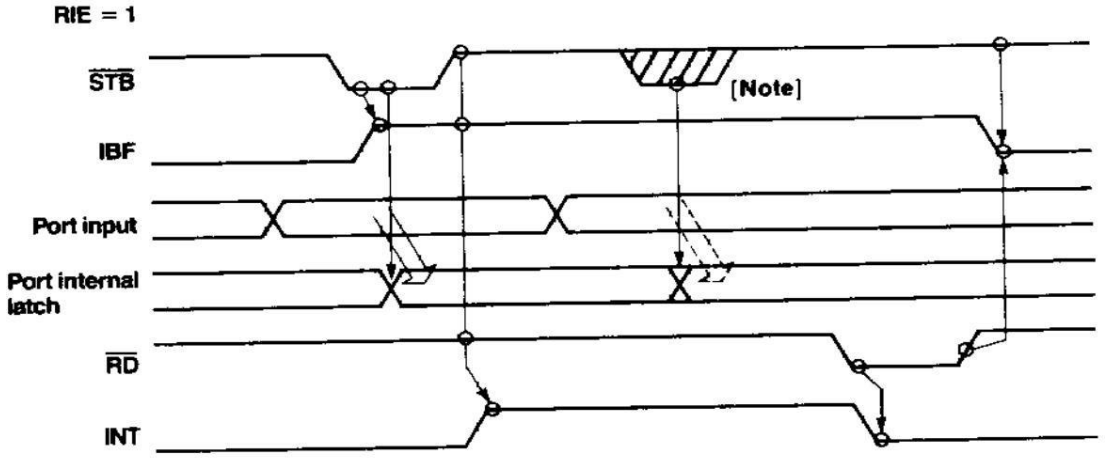
```
READ_A/D:   MOV     AL,10011000B    ; XD71055 Mode Setting:
            OUT     CTRLPORT,AL     ;Group 0, group 1 in mode 0
                                    ;Port 0 & port 2 (upper) are inputs
                                    ;Port 1 & port 2 (lower) are outputs
            MOV     AL,00000001B
            OUT     CTRLPORT,AL     ;Conversion starts by setting P2₀ high
WAIT_EOC:   IN      AL,PORT2        ;End of conversion wait loop
            TEST1   AL,7            ;Conversion ends when P2₇ = 0
            BNZ     WAIT_EOC
            IN      AL,PORT0        ;Read A/D converted values
            RET
```

Figure 9.Mode 1 Input



*Note: Bit $P2_3$ is available in Group 1 only when Group 0 is Mode 0. For all other conditions $P2_3$ is part of Group 0. This diagram shows how bit $P2_3$ would be used if Group 1 was in Mode 1.

Figure 10.Mode 1 Input Timing



Note: If STB goes low here before IBF goes low, original contents of port latch will change. STB must be kept high until IBF goes low to prevent loss of date.

Figure 11.Mode 1 Output

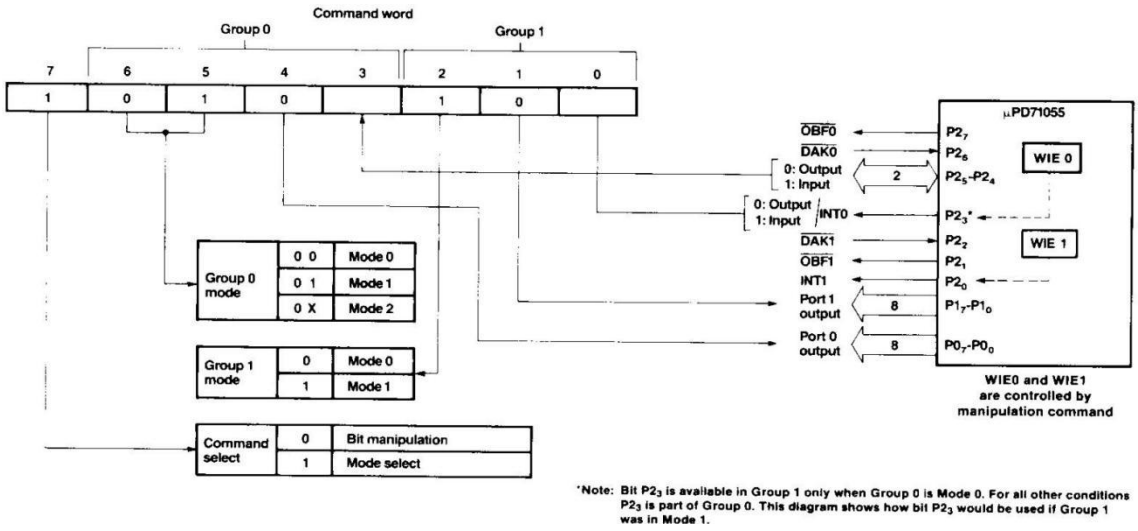
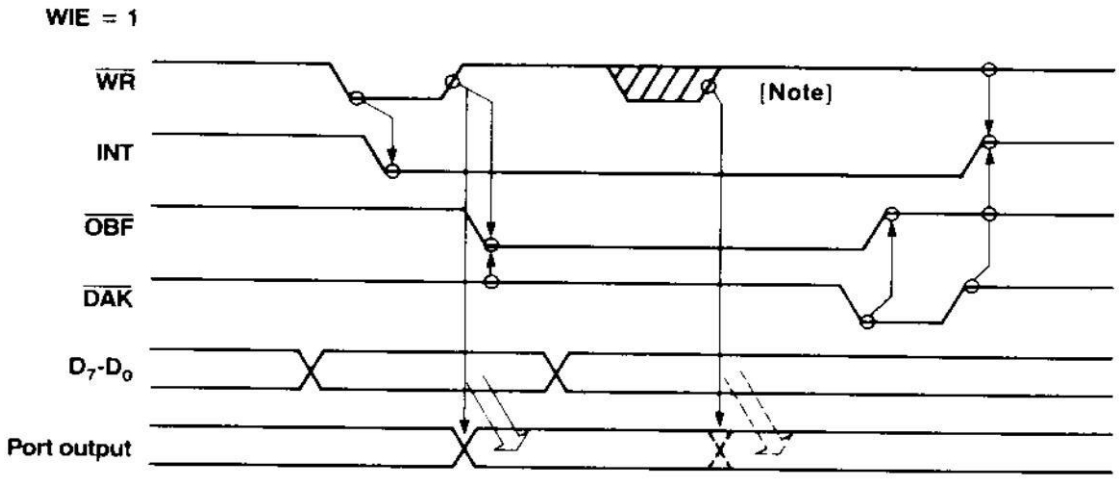


Figure 12.Mode 1 Output Timing



Note: If data is written to the μPD71055 before $\overline{OBF}$ goes high the original contents of the port latch will change. Data must not be written while $\overline{OBF}$ is low to prevent loss of data

Figure 13.Connection to Printer

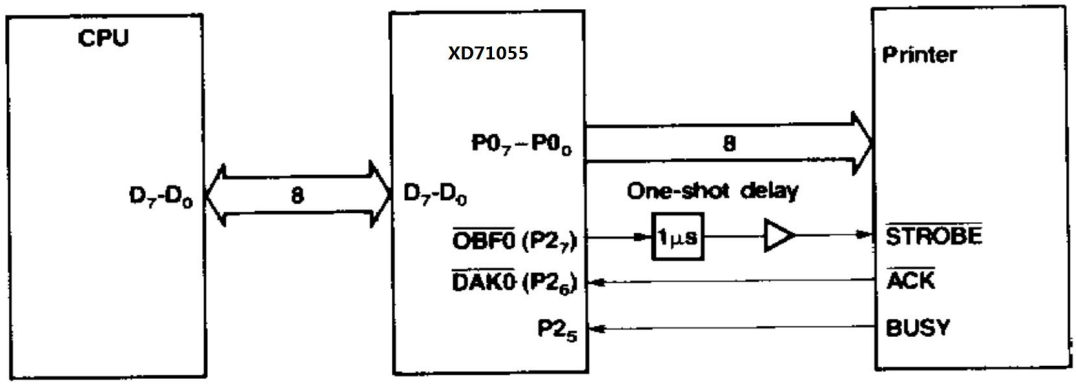


Figure 14.Printer Example Subroutine

```
;This subroutine sends character strings to the printer
INIT:       MOV     AL,10101000B    ; XD71055 Mode Setting:
                                    ;Group 0: mode 1 output
                                    ;Group 1: mode 0
            OUT     CTRLPORT,AL
            RET
SENDPRN:    MOV     BW,DATA         ;Output data address
PRNLOOP:    MOV     AL,[BW]
            CMP     AL,0FFH         ;End if data = 0FFH
            BNZ     WAIT
            RET
WAIT:       IN      AL,PORT2
            TEST1   AL,7            ;Wait until output buffer is empty
            BZ      WAIT
            TEST1   AL,5            ;Wait until printer can accept data
            BNZ     WAIT
            MOV     AL,[BW]         ;Send data to printer
            OUT     PORT0,AL
            INC     BW
            BR      PRNLOOP
```

Figure 15.Printer Example Subroutine

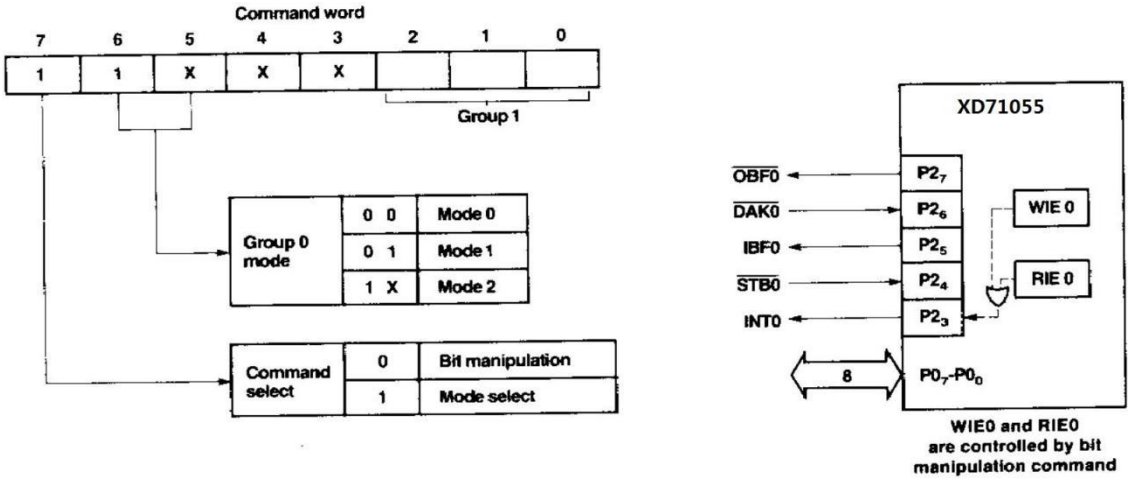
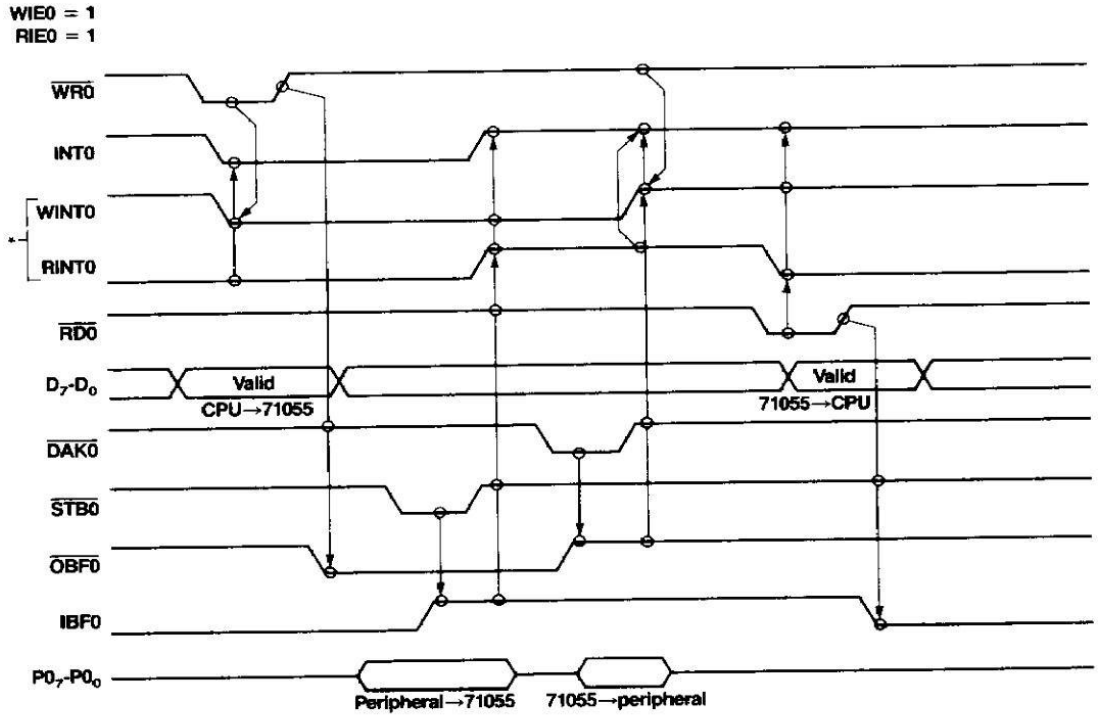


Figure 16.Mode 2 Timing



Note:
WINT0 and RINT0 are internal signals and are write and read interrupt request signals to the CPU, respectively.
WINT0 = $\overline{OBF0}$ (•) $\overline{WIE0}$ (•) $\overline{DAK0}$ (•) $\overline{WR0}$
RINT0 = IBF0 (•) RIE0 (•) $\overline{STB0}$ (•) $\overline{RD0}$
Also note that
INT0 = WINT0 (+) RINT0

Figure 17.Connecting Two CPUs

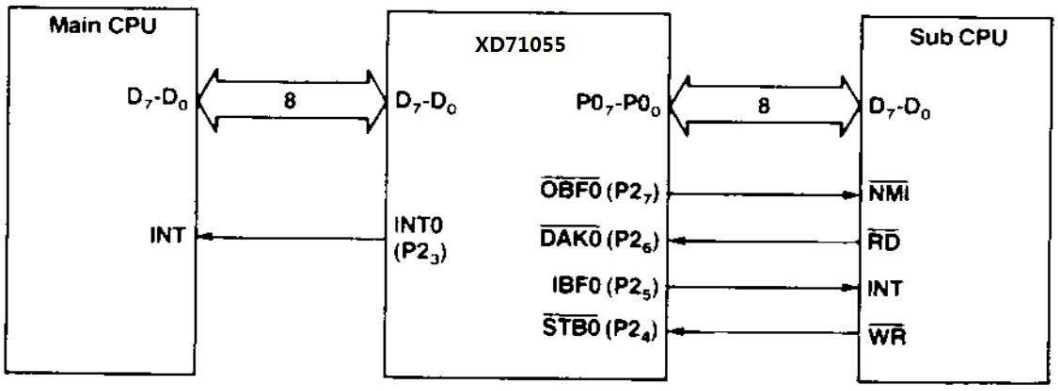


Figure 18.Main CPU Flowchart

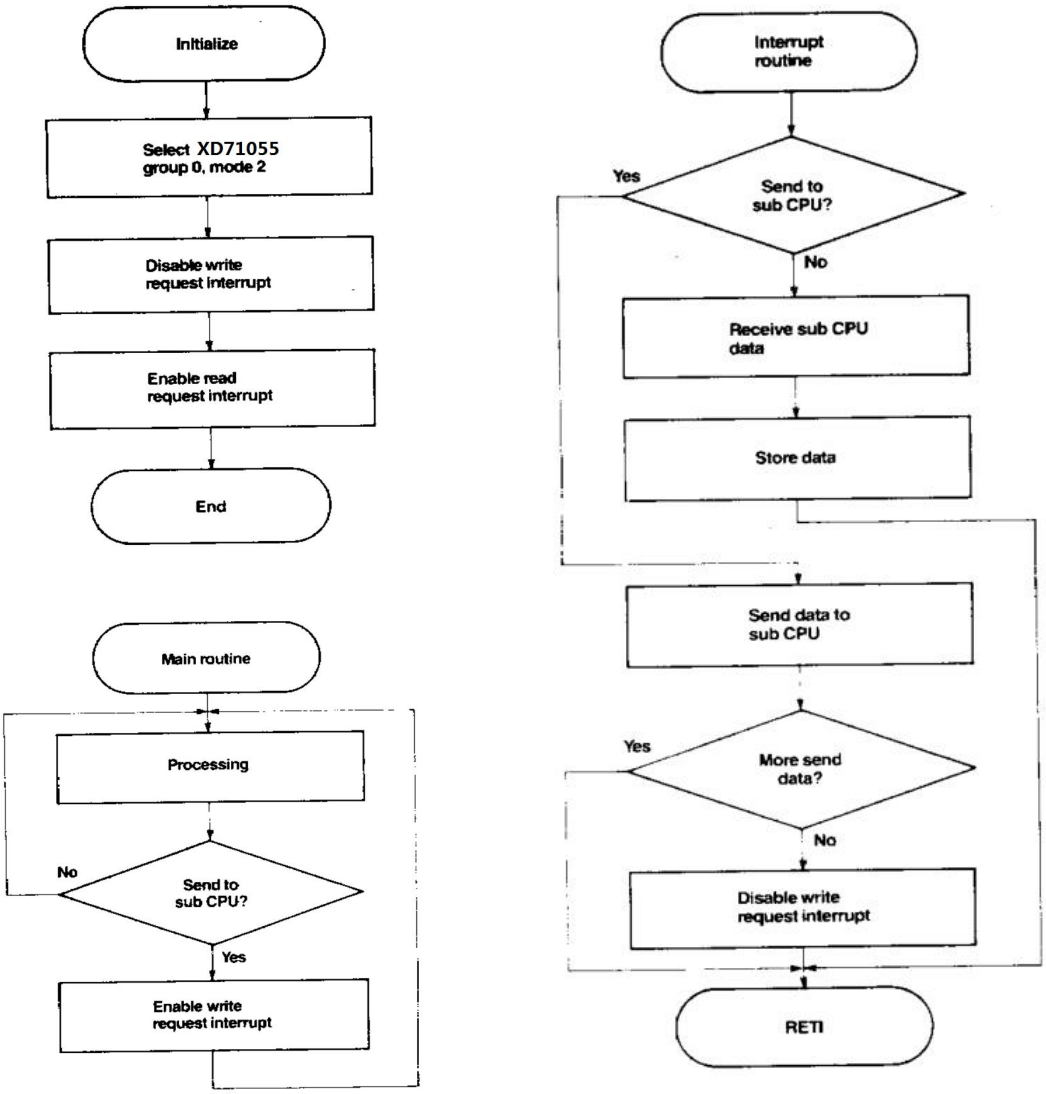
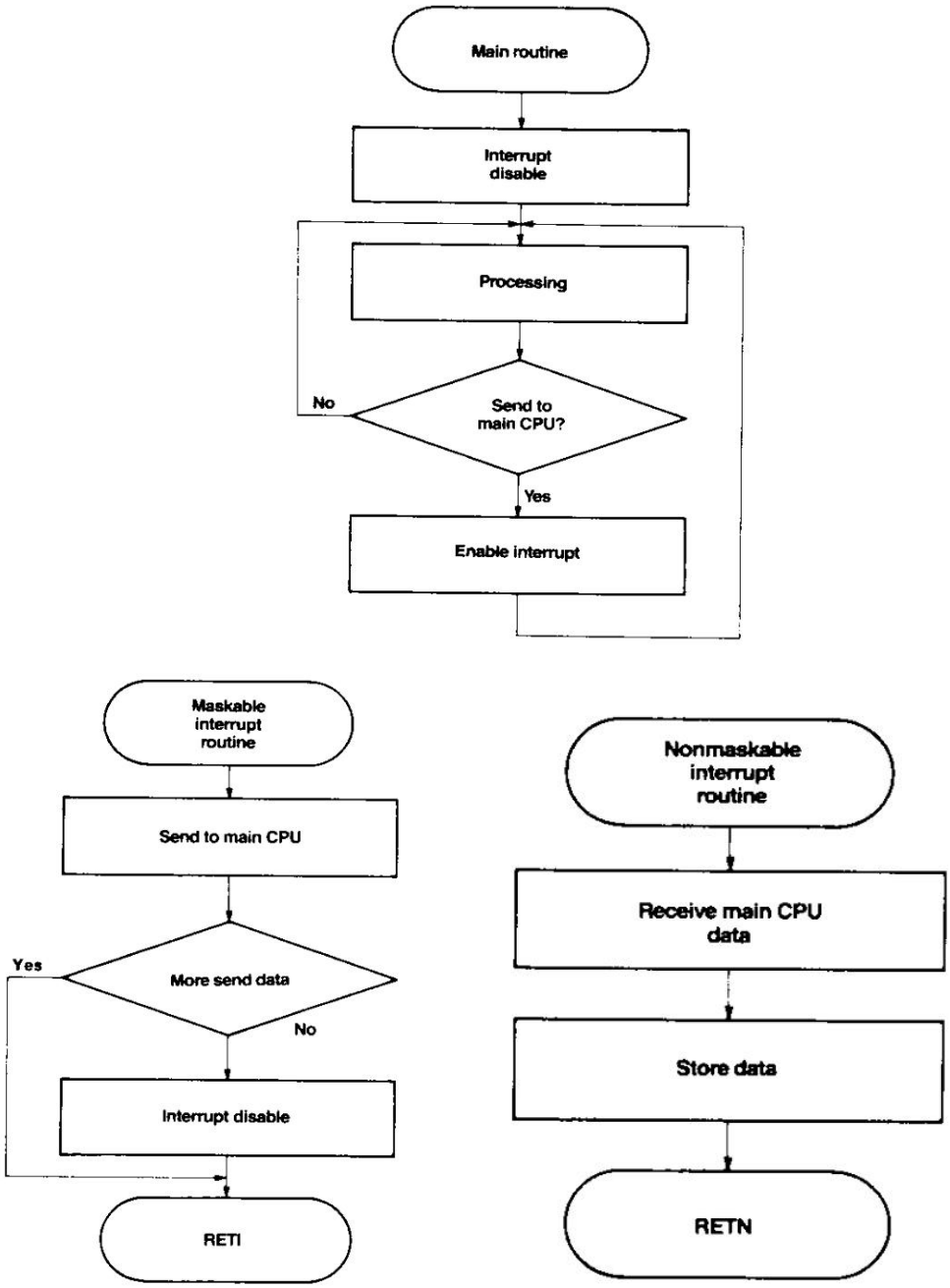


Figure 19.Sub CPU Flowchart



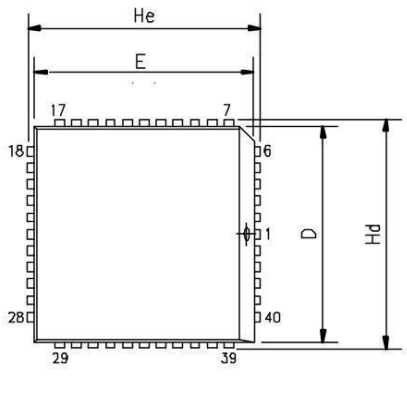
14. ORDERING INFORMATION

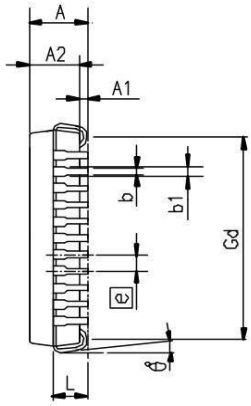
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD71055	XD71055	DIP40	52.32 * 13.80	-40 to +85	MSL3	Tube 9	180
XP71055	XP71055	PLCC44	16.58 * 16.58	-40 to +85	MSL3	T&R	500

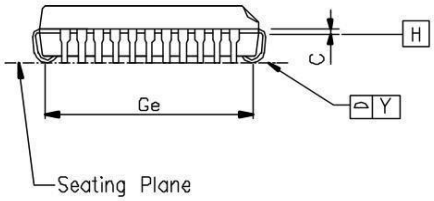
15. DIMENSIONAL DRAWINGS

PLCC44

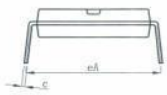




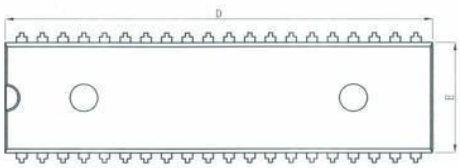
SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	4.191	–	4.572
A1	0.508	–	–
A2	3.734	–	4.013
b1	0.660	0.711	0.813
b	0.330	0.432	0.533
c	0.178	0.254	0.330
D	16.510	16.586	16.662
E	16.510	16.586	16.662
e	1.270 BSC		
Gd	14.986	15.494	16.002
Ge	14.986	15.494	16.002
Hd	17.399	17.526	17.653
He	17.399	17.526	17.653
L	2.540	–	2.845
Y	–	–	0.102

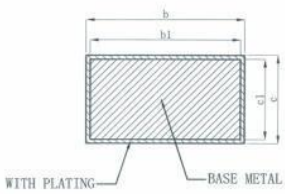


DIP40



symbol	millimeter		
	Min	Nom	Max
A	3.40	3.50	3.60
b	0.44	----	0.53
b1	0.43	0.46	0.49
c	0.25	----	0.30
c1	0.24	0.25	0.26
D	52.22	52.32	52.42
E	13.70	13.80	13.90
e	2.54BSC		
eA	15.24	----	17.21
L	3.00	----	----





SECTION A-A

[if you need help contactus. Xinluda reserves the right to change the above information without priornotice]