MPQ2735

Low-Voltage 0.45Ω Dual SPDT Analog Switches

AEC-Q100 Qualified

The Future of Analog IC Technology

GENERAL DESCRIPTION

The MPQ2735 are low voltage, low on-resistance, dual single-pole , double-throw (SPDT) monolithic CMOS analog switches designed for high performance switching of analog signals. Combining low-power, high speed, low on-resistance, and small package size, the MPQ2735 are ideal for portable and battery power applications.

The MPQ2735 have an operation range from 1.65V to 5.5V single supply. The MPQ2735 has two separate control pins and two separate SPDT switches.

The MPQ2735 are guaranteed 1.65V logic compatible for V+<3.3V, allowing the easy interface with low voltage DSP or MCU control logic and ideal for one cell Li-ion battery direct power.

The switch conducts signals within power rails equally well in both directions when on, and blocks up to the power supply level when off. Break-before-make is guaranteed.

The MPQ2735 are offered in a QFN10 package.

FEATURES

- Guaranteed Industrial/Automotive Temperature
- Low Voltage Operation (1.65V to 5.5V)
- Low On-Resistance - R_{ON}: 0.45Ω at 2.7V
- Fast Switching: T_{ON} = 29ns at 2.7V
- T_{OFF} = 23ns at 2.7V
- Latch-Up Current >300mA (JESD78)
- 2mm x 2mm QFN10 Package
- ESD Human-Body Model ±4000V
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Powered Systems
- Portable Media Player
- Handheld Test Instruments

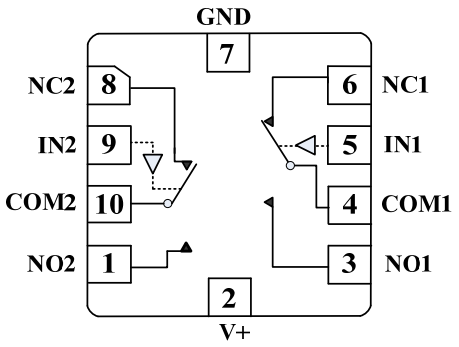
TRUTH TABLE

	IN1/2	NC1/2	NO1/2
MPQ2735	0	ON	OFF
	1	OFF	ON

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

FUNCTIONAL BLOCK DIAGRAM PIN CONFIGURATION



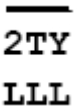
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ2735GG	QFN-10 (2mmx2mm)	*See Below*
MPQ2735GG-AEC1	QFN-10 (2mmx2mm)	*See Below*

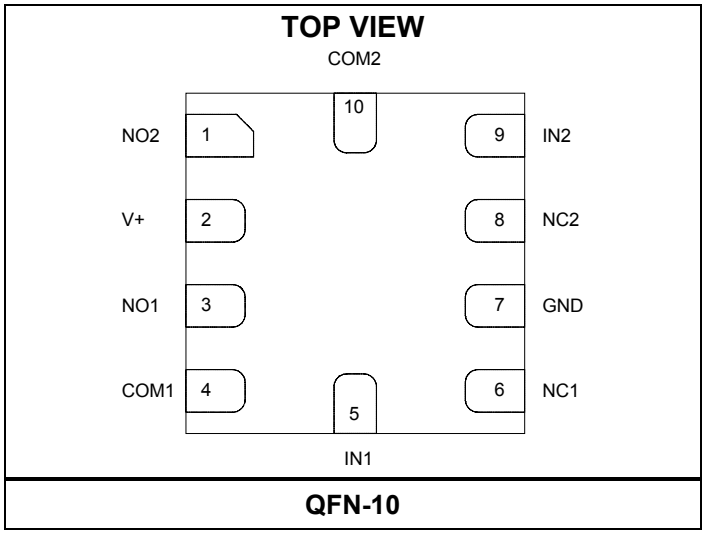
* For Tape & Reel, add suffix –Z (e.g. MPQ2735GG–Z);

TOP MARKING



2T: product code of MPQ2735GG&MPQ2735GG-AEC1;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS

V+ Supply Voltage .....-0.3V to +6V
IN/COM/NC/NO Voltage (1) ... -0.3V to V+ + 0.3V
Current
(Any terminal except NO, NC or COM) .....
..... 30mA
Continuous Current (NO, NC or COM) .....
..... ±250mA
Peak Current
(Pulsed at 1ms, 10% duty cycle) ..... ±500mA
Storage Temperature..... -65°C to +150°C
Power Dissipation (QFN10 (2)) (3) 208mW

Notes:

1) Signals on NC, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2) Derate 4.0mW/℃ above 70℃.
3) All leads welded or soldered to PC Board.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V+=3V, ±10%, V_{IN}=0.4 or 1.65V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Analog Switch							
Analog Signal Range	V_{analog}	$r_{DS(on)}$, T_A= -40°C to +125°C		0		V+	V
On-Resistance	$r_{DS(on)}$	V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V	T_A= +25°C		0.28	0.45	Ω
		V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=1.5V					
		V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V	T_A= -40°C to +125°C		0.30		
		V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=1.5V					
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=0.9V	T_A= +25°C		0.20	0.30	
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=2.5V			0.18		
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=0.9V	T_A= -40°C to +125°C		0.25		
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=2.5V					
r_{ON} Match	Δr_{on}	V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V/1.5V	T_A= +25°C		0.01	0.02	
		V+=5.5V, $I_{NO/NC}$=100mA, V_{COM}=0.9V/2.5V					
r_{ON} Flatness	r_{ON} Flatness	V+=2.7V, $I_{NO/NC}$=100mA, V_{COM}=0.5V/1.5V				0.15	
Switch Off Leakage Current	$I_{NO/NC(off)}$	V+=5.5V, $V_{NO/NC}$=0.3V/4.0V, V_{COM}=4.0V/0.3V	T_A= +25°C	-40		40	nA
			T_A= -40°C to +125°C	-1000		1000	
	$I_{COM(off)}$		T_A= +25°C	-40		40	
			T_A= -40°C to +125°C	-1000		1000	
Channel-On Leakage Current	$I_{COM(on)}$	V+=5.5V, $V_{NO/NC}$=V_{COM}=4.0V/0.3V	T_A= +25°C	-40		40	
			T_A= -40°C to +125°C	-1000		1000	
Digital Control							
Input High Voltage	V_{INH}		T_A= -40°C to +125°C	1.65			V
Input Low Voltage	V_{INL}					0.4	
Input Capacitance	C_{IN}				6		pF
Input Current	I_{INL} or I_{INH}	V_{IN}=0		-1		1	µA
		V_{IN}= V+			5.5		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V+=3V, ±10%, V_{IN}=0.4 or 1.65V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Dynamic Characteristics							
Break-Before-Make Time (4)	t_{BBM}	V+=3.6V, V_{NO}/V_{NC}=1.5V, R_L=50Ω, C_L=35pF	T_A= +25°C		10		ns
Turn-On Time (4)	t_{ON}		T_A= +25°C		24		
			T_A= -40°C to +125°C		40		
Turn-Off Time (4)	t_{OFF}		T_A= +25°C		20		
			T_A= -40°C to +125°C		35		
Off-Isolation(4)	OIRR	R_L=50Ω, C_L=5pF, f=100kHz	T_A= +25°C		-70		dB
Crosstalk(4)	XTALK				-70		dB
3dB Bandwidth (4)		R_L=50Ω, C_L=5pF			50		MHz
NO, NC Off Capacitance(4)	$C_{NO(off)}$	V_{IN}=0V, or V+, f=1MHz			55		pF
	$C_{NC(off)}$				55		
Channel On Capacitance(4)	$C_{NO(on)}$				130		
	$C_{NC(on)}$				130		
Power Supply							
Power Supply Range	V+			1.65		5.5	V
Power Supply Current	I+	V_{IN}=0 or V+	T_A= 25°C	-1		1	µA

Note:

4) Guarantee by design, not subjected to production test.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

PIN FUNCTIONS

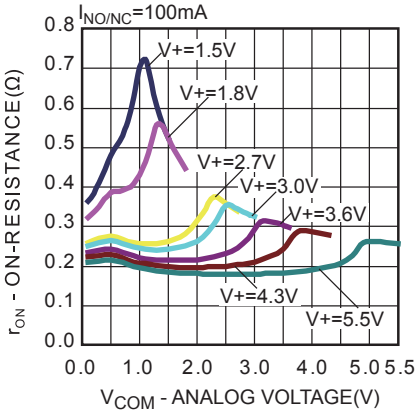
Pin #	Name	Description
1	NO2	Normally open I/O port of switch2
2	V+	Supply Voltage
3	NO1	Normally open I/O port of switch1
4	COM1	Commom I/O port for NC and NO channels of switch1
5	IN1	Channel select signal for switch1. IN1 high, NO1 channel is selected.
6	NC1	Normally closed I/O port of switch1
7	GND	Ground
8	NC2	Normally closed I/O port of switch2
9	IN2	Channel select signal for switch2. IN2 high, NO2 channel is selected.
10	COM2	Commom I/O port for NC and NO channels of switch2

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

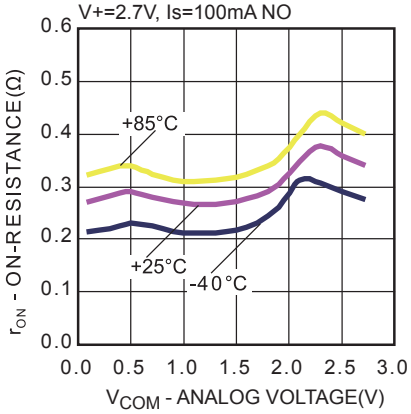
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, unless otherwise noted.

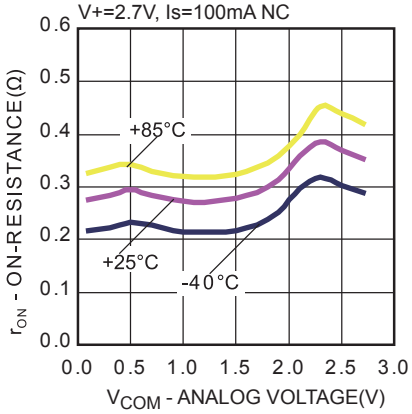
r_{ON} vs. V_{COM} and Supply Voltage



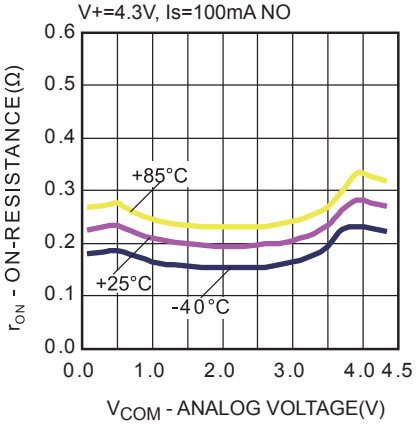
r_{ON} vs. V_{COM} and Temperature



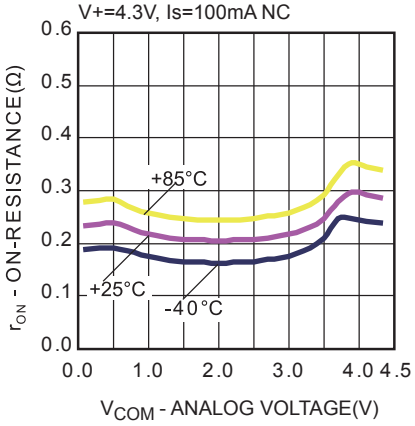
r_{ON} vs. V_{COM} and Temperature



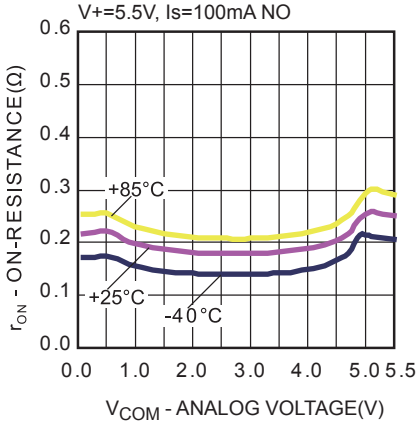
r_{ON} vs. V_{COM} and Temperature



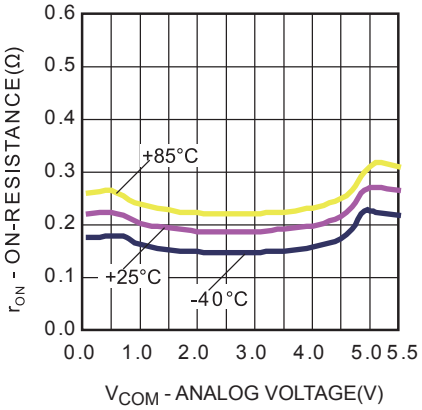
r_{ON} vs. V_{COM} and Temperature



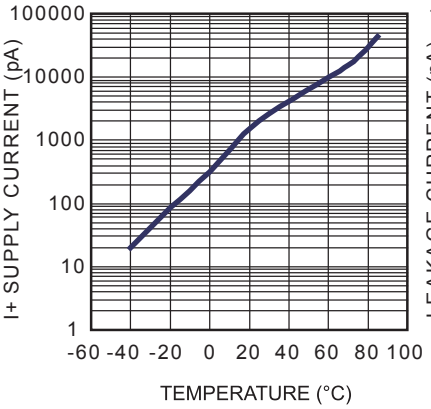
r_{ON} vs. V_{COM} and Temperature



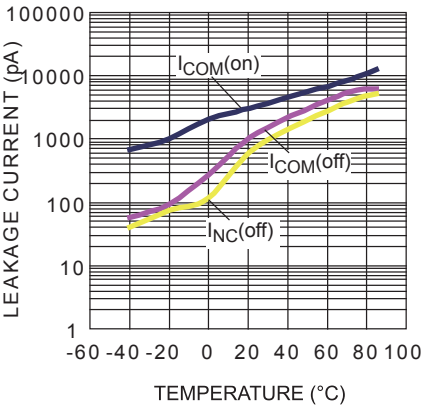
r_{ON} vs. V_{COM} and Temperature



Supply Current vs. Temperature



Leakage Current vs. Temperature

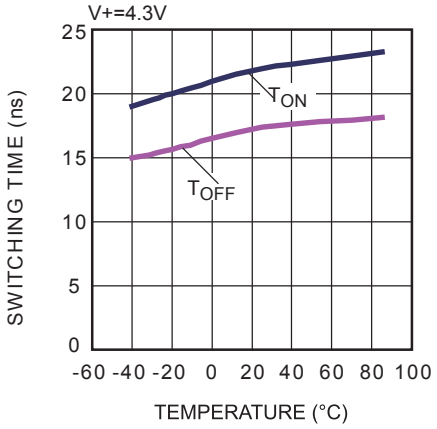


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

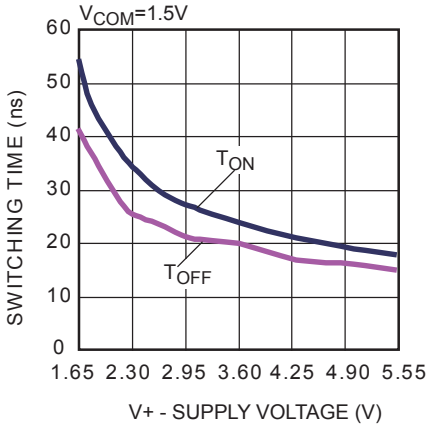
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

T_A = +25°C, unless otherwise noted.

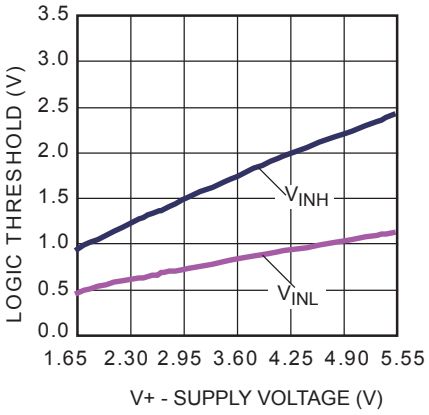
Switching Time vs. Temperature



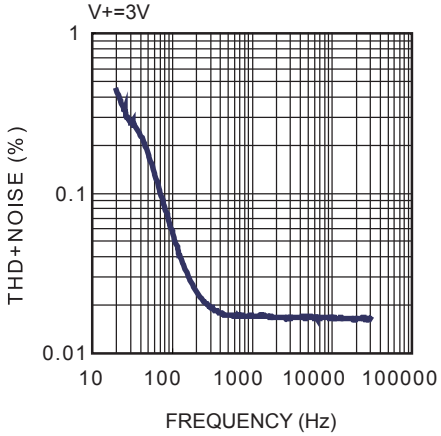
Switching Time vs. Supply Voltage



Logic Threshold vs. Supply Voltage

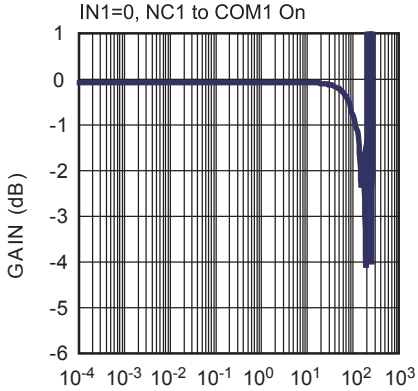


Total Harmonic Distortion vs. Frequency



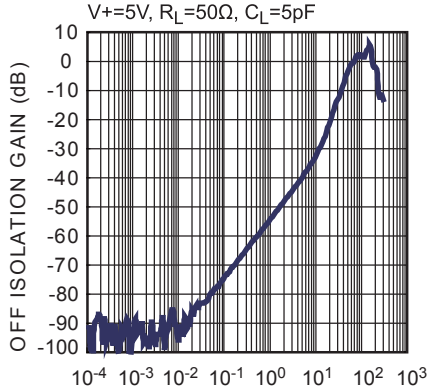
Bandwidth vs. Frequency

V+=5V, R_L=50Ω, C_L=5pF,
IN1=0, NC1 to COM1 On



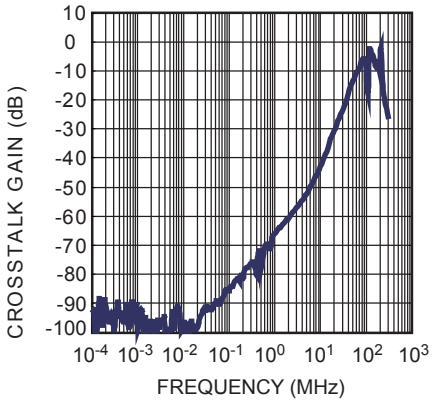
Off Isolation vs. Frequency

V+=5V, R_L=50Ω, C_L=5pF



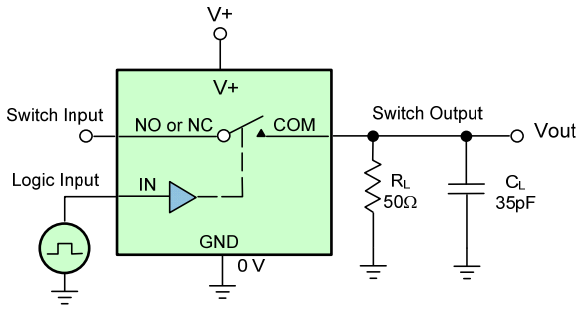
Crosstalk vs. Frequency

V+=5V, R_L=50Ω, C_L=5pF



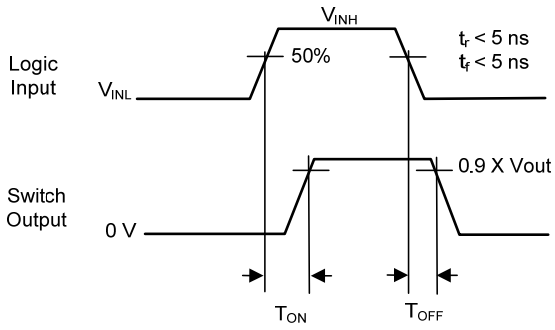
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

TEST CIRCUITS



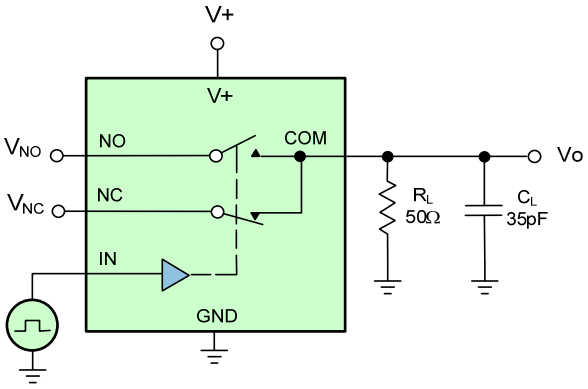
C_L (includes fixture and stray capacitance)

$$V_{out} = V_{COM}(\frac{R_L}{R_L + R_{ON}})$$



Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1 — Switching Time



C_L (includes fixture and stray capacitance)

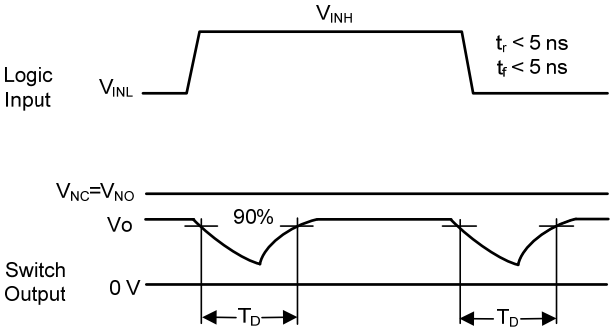
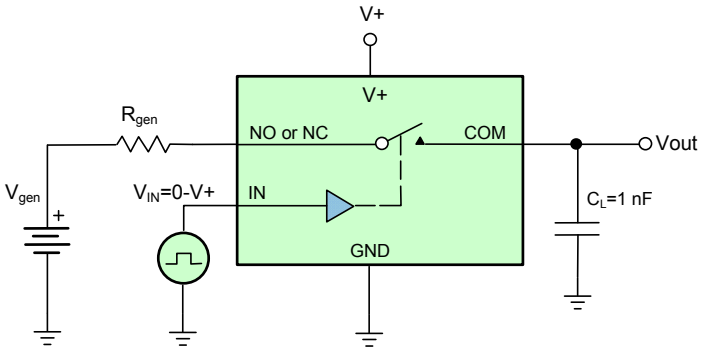
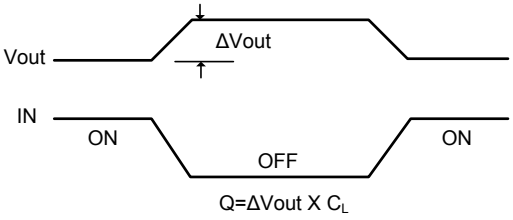


Figure 2 — Break-Before-Make Interval



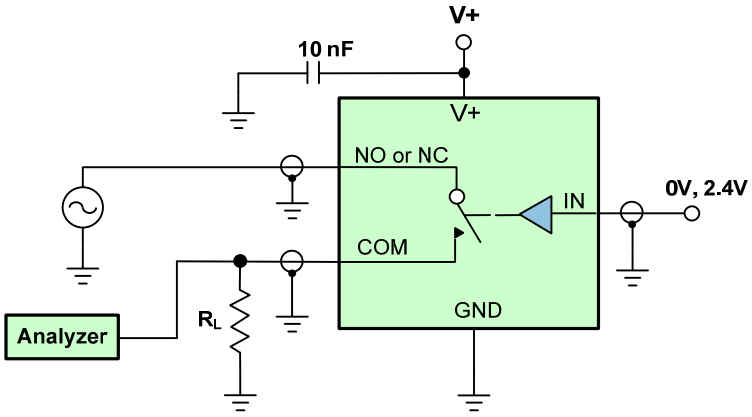


$Q = \Delta Vout \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3 — Charge Injection

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.



$$\text{Off Isolation} = 20 \log \frac{V_{COM}}{V_{NO/NC}}$$

Figure 4 — Off-Isolation

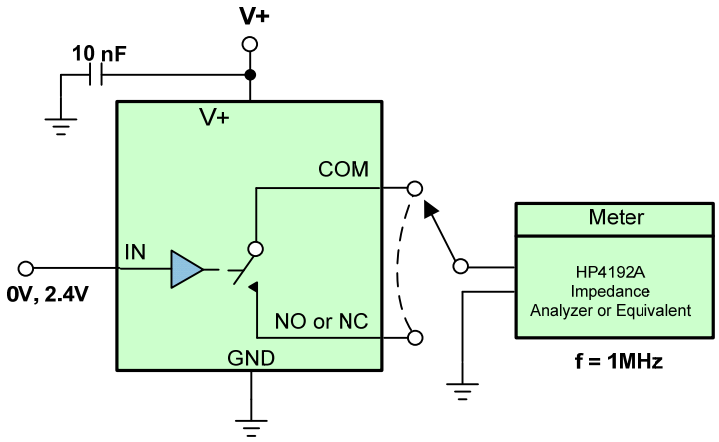
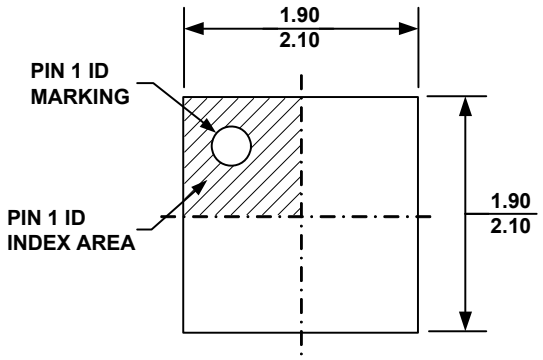


Figure 5 — Channel Off/On Capacitance

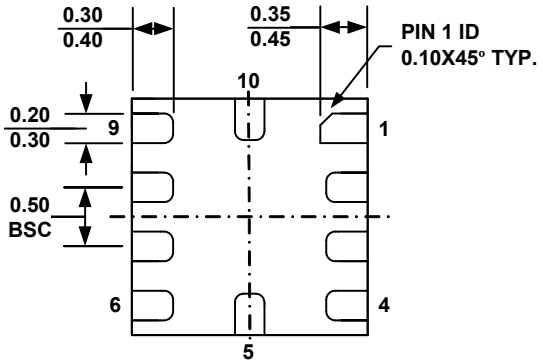
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

PACKAGE INFORMATION

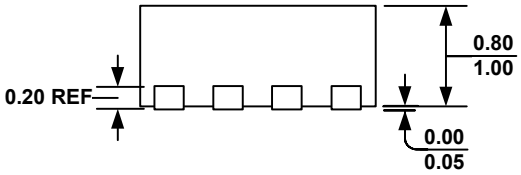
QFN-10 (2mmX2mm)



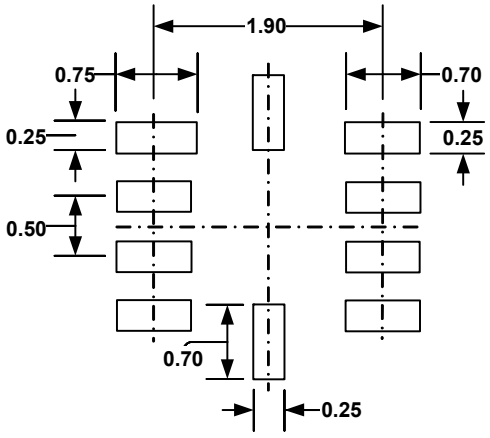
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.