

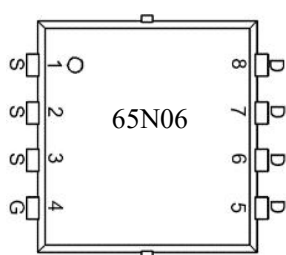
**Features**

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

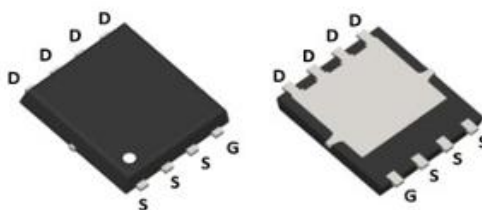
 B_{vds} **60V** **R_{dson}** **8mΩ** **I_D** **65A****Application**

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

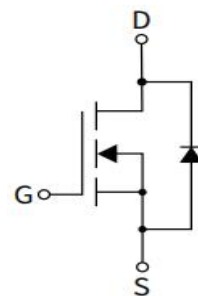
RoHS

Package

Marking and pin assignment



PDFN5*6-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
65N06	S65N06F	PDFN5*6-8L	5000

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	($T_C = 25^{\circ}\text{C}$)	I_D	65	A
Continuous Drain Current ¹	($T_C = 100^{\circ}\text{C}$)	I_D	49	A
Pulsed Drain Current ¹		I_{DM}	240	A
Single Pulsed Avalanche Energy ²		E_{AS}	56	mJ
Avalanche Current		I_{AS}	-	A
Power Dissipation@ $T_C = 25^{\circ}\text{C}$		P_D	89	W
Junction Temperature		T_J	$-55 \sim +175$	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	$-55 \sim +175$	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	--	2.5	$^{\circ}\text{C}/\text{W}$
Thermal Resistance,Junction-to-Ambient	$R_{\theta JA}$	--	--	$^{\circ}\text{C}/\text{W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS65N06F	PDFN5*6-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$	-	-	1	μA
Gate to Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	1.6	2.5	V
Static Drain-Source on-Resistance ³	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=20\text{A}$	-	8	11	m Ω
		$V_{GS}=4.5\text{V}, I_D=10\text{A}$	-	14	20	m Ω
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V},$ $f=1.0\text{MHz}$	-	930	-	pF
Output Capacitance	C_{oss}		-	370	-	
Reverse Transfer Capacitance	C_{rss}		-	20	-	
Total Gate Charge	Q_g	$V_{DS}=30\text{V}, I_D=20\text{A},$ $V_{GS}=10\text{V}$	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	4.8	-	
Gate-Drain(“Miller”) Charge	Q_{gd}		-	4.5	-	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30\text{V}, I_D=20\text{A},$ $R_G=1.6\Omega, V_{GS}=10\text{V}$	-	4.9	-	nS
Turn-on Rise Time	t_r		-	31	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	
Turn-Off Fall Time	t_f		-	8.7	-	
Maximum Continuous Drain to Source Diode Forward Current	I_S	--	-	-	65	A
Maximum Pulsed Drain to Source Diode Forward Current	I_{SM}	--	-	-	240	A
Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=30\text{A}$	-	-	1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F=20\text{A}, di/dt = 100\text{A}/\mu\text{s},$ $T_J=25^{\circ}\text{C}$	-	34	-	nS
Body Diode Reverse Recovery Charge	Q_{rr}		-	14	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: $T_J=25^{\circ}\text{C}$, $V_{DD}=30\text{V}, V_G=10\text{V}, R_G=25\Omega, L=0.5\text{mH}, I_{AS}=12\text{A}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$



Typical Performance Characteristics

Figure 1: Output Characteristics

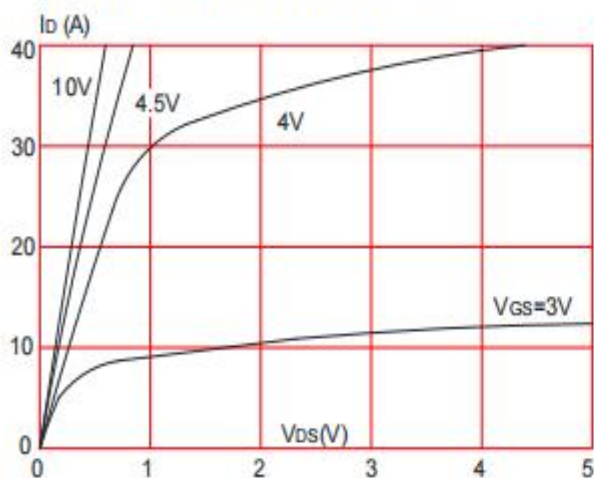


Figure 2: Typical Transfer Characteristics

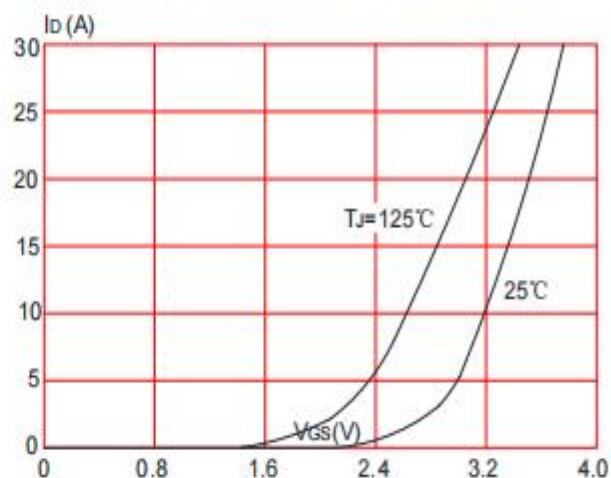


Figure 3: On-resistance vs. Drain Current

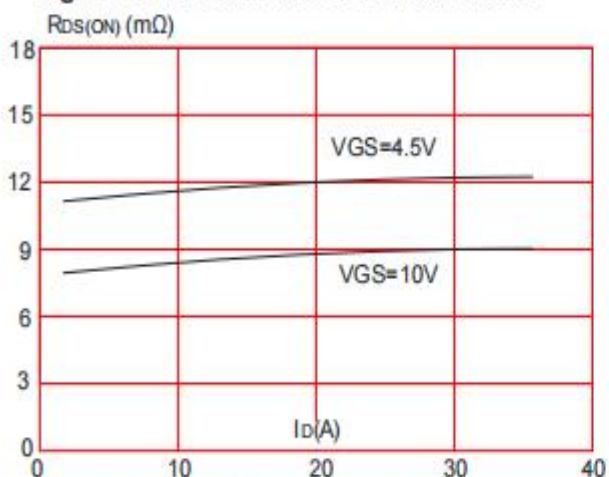


Figure 4: Body Diode Characteristics

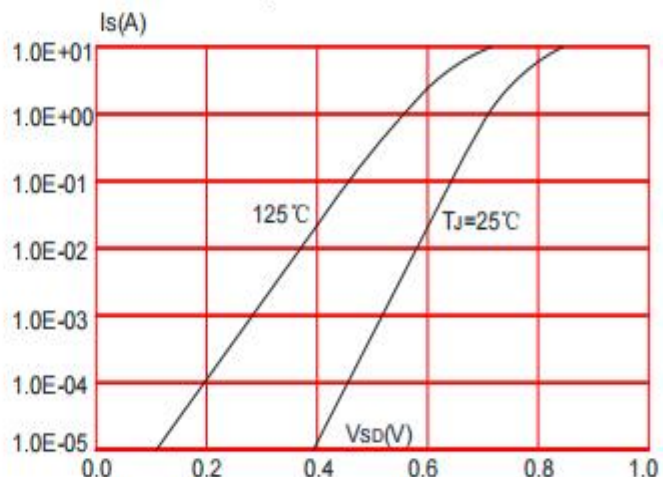


Figure 5: Gate Charge Characteristics

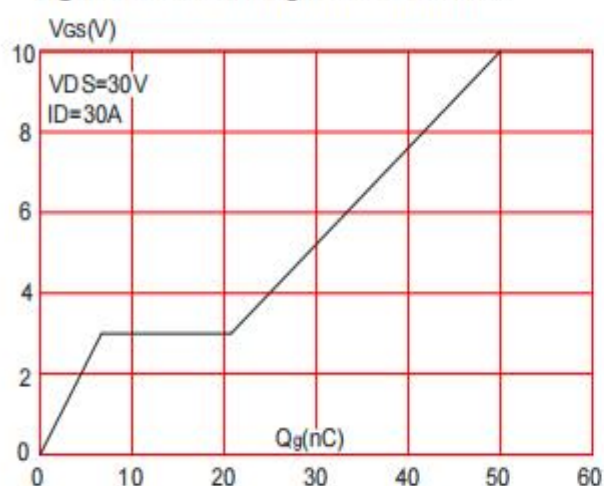


Figure 6: Capacitance Characteristics

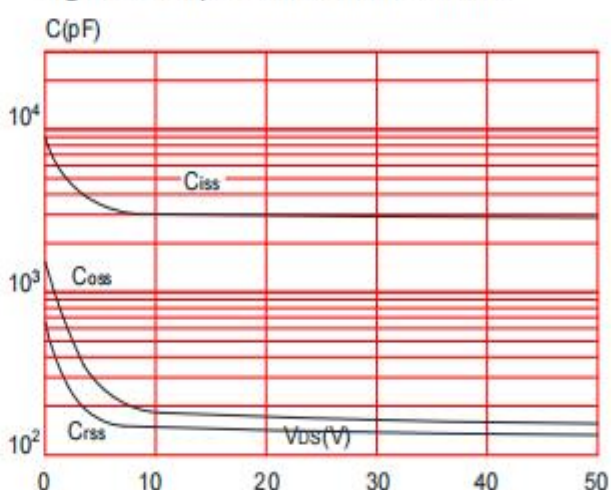


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

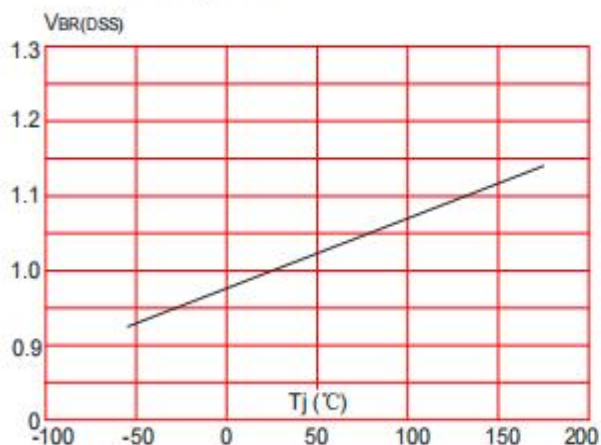


Figure 8: Normalized on Resistance vs. Junction Temperature

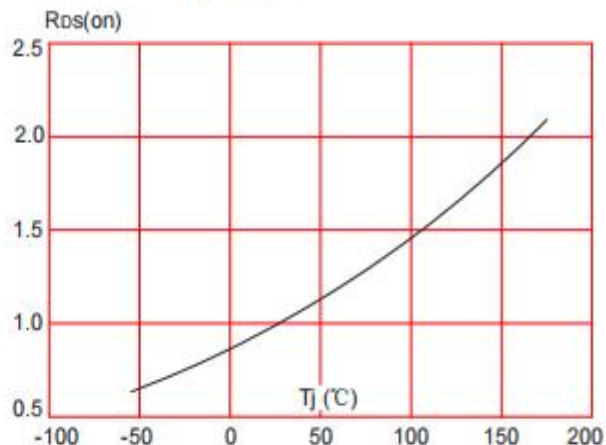


Figure 9: Maximum Safe Operating Area

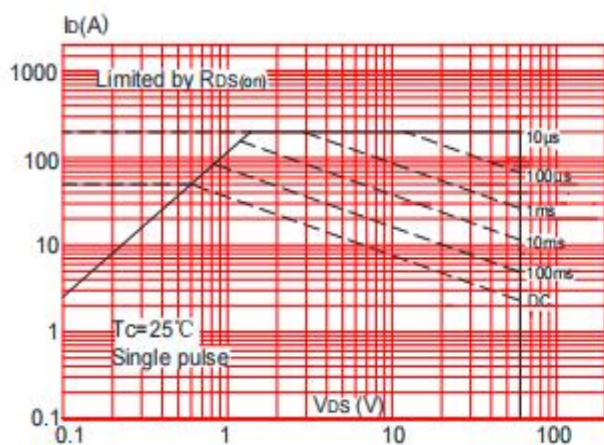


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

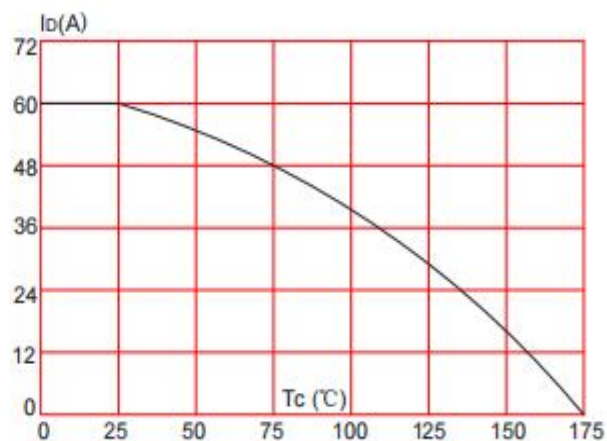
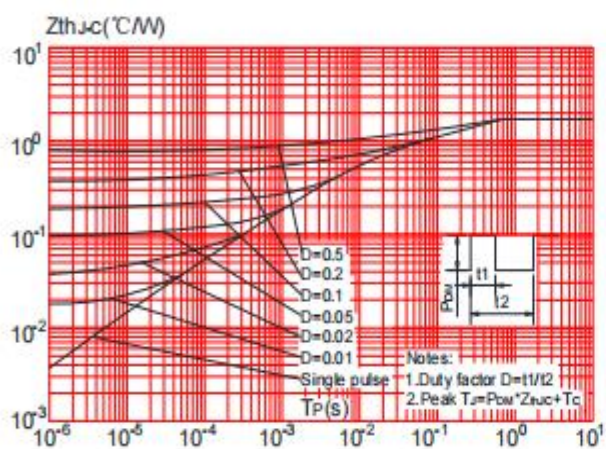
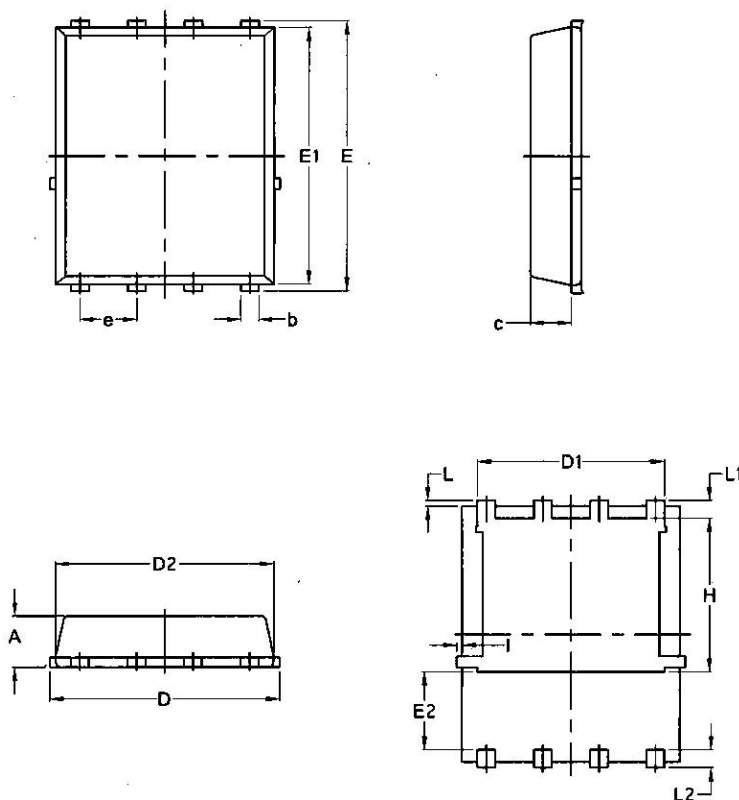


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Package Dimensions PDFN5x6-8L



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070



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