Ultra-low Power High Performance 2.4 GHz GFSK Transceiver

Key Features

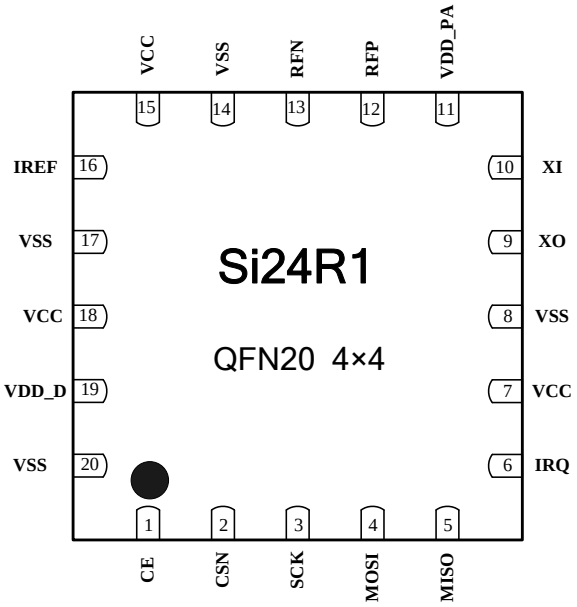
- Worldwide 2.4GHz ISM band operation
- Modulation：GFSK/FSK
- Air data rate：2Mbps/1Mbps/250Kbps
- Ultra low shutdown current：1uA
- Ultra low standby current：15uA
- Receiver sensitivity：-83dBm @2Mbps
- Maximum transmission power：7dBm
- RX supply current (2Mbps)：15mA
- TX supply current (2Mbps): 12mA (0dBm)
- Internal integrated high PSRR LDO
- Supply range：1.9-3.6V
- Digital I/O voltage range: 1.9-5.25V
- Max 130us start-up from standby mode
- Maximum rate 10MHz,4-wire interface SPI
- Embedded ARQ baseband protocol engine
- TX/RX Hardware interrupt output
- Support 1bit RSSI output
- Low cost crystal：16MHz±60ppm
- Minimal peripheral devices, reducing system application costs
- QFN20 package or COB package

Block diagram

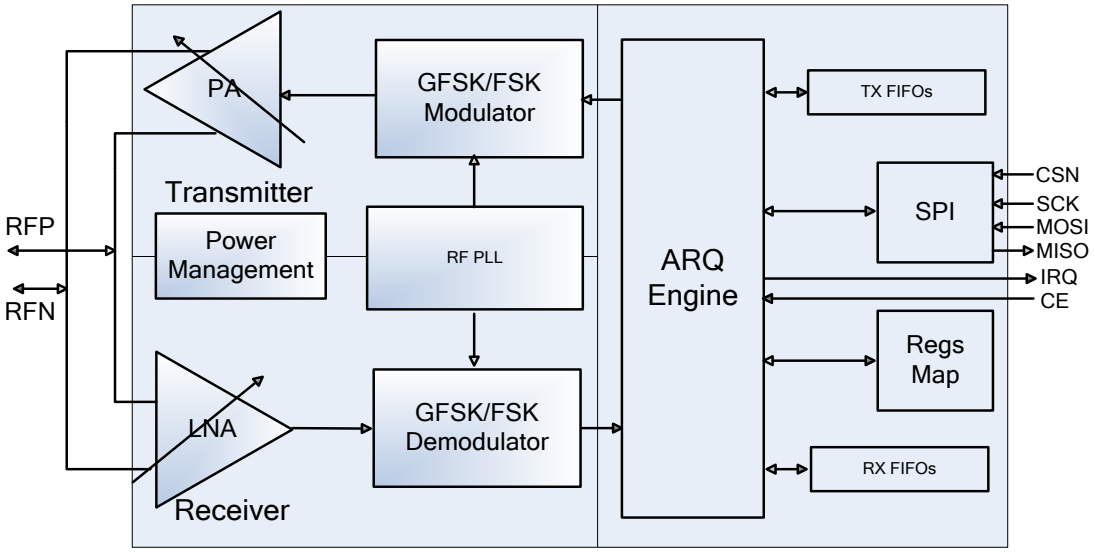
Applications

- Wireless mouse and keyboards
- Remote control、Somatosensory device
- Active RFID
- Smart Grid and Home automation
- Wireless audio
- Wireless data transceiver module
- Ultra low power wireless sensor networks

Pin Assignments



Rev 1.2 2024/04/03



Abbreviations

ARQ	Auto Repeat-reQuest
ART	Auto ReTransmission
ARD	Auto Retransmission Delay
BER	Bit Error Rate
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select
DPL	Dynamic Payload Length
GFSK	Gaussian Frequency Shift Keying
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
Mbps	Megabit per second
MCU	Micro Controller Unit
MHz	Mega Hertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
PA	Power Amplifier
PID	Packet Identity
PLD	Payload
RX	RX
TX	TX
PWR_DWN	Power Down
PWR_UP	Power UP
RF_CH	Radio Frequency Channel

RSSI	Received Signal Strength Indicator
RX	Receiver
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TX	Transmitter
TX_DS	Transmit Data Sent
XTAL	Crystal

Contents

1 Introduction

Si24R1 is a single chip transceiver with an embedded ARQ baseband protocol engine, suitable for ultra-low power wireless applications and is designed for operation in the 2.4GHz ISM frequency band at 2400MHz to 2525MHz.The operating frequency band is divided into 126 RF channels and the resolution of the RF channel frequency setting is 1MHz. Internal high PSRR LDO power ensures reliable work in a wide supply range from 1.9V to 3.6V.

Si24R1 uses GFSK/FSK digital modulation and demodulation. The air data rate is configurable and can be programmed to 2Mbps, 1Mbps and 250Kbps. The higher data rate contributes the lower power consumption because it takes less time to transmit or receive signals. The output power of Si24R1 can be adjusted and it can base on actual application to configure the appropriate output power, thus saving the power of system.

Si24R1 is especially optimized for low power wireless applications. All register values and FIFO values are maintained in Shutdown mode, and the shutdown supply current is 1uA. In Standby mode, the clock still works, and the standby supply current is 15uA. It takes less than 130us to start data transmitting and receiving.

Si24R1 is easy to use, and it can realize communication only by configuring several registers through the SPI with an MCU(microcontroller). The embedded ARQ baseband protocol engine is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system’s MCU. Enhanced ARQ baseband protocol engine reduces the system consumption of MCU by handling all high speed link layer operations.

Si24R1 has very low costs of system application. To design a radio system with the Si24R1, you simply need a microcontroller and a few external passive components. Digital I/O is compatible with several I/O voltage standards such as 2.5V/3.3V/5V, and it can be connected directly to various MCU I/O ports.

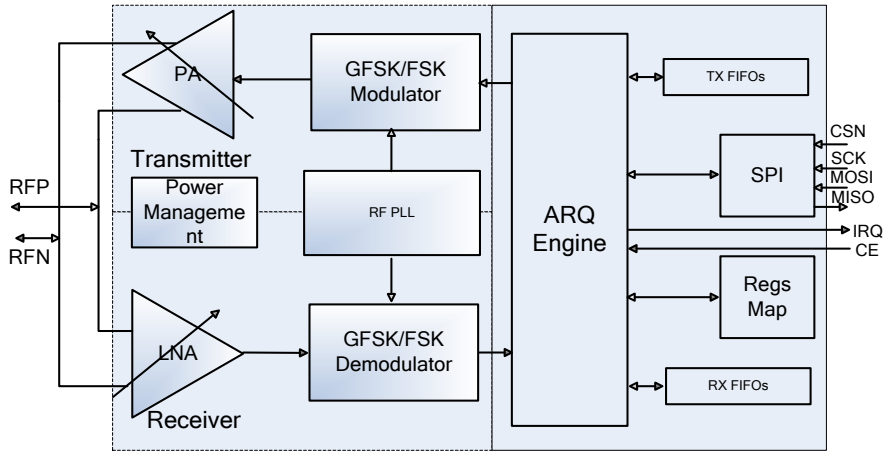


Figure 1-1 Si24R1 block diagram

2 Pin Information

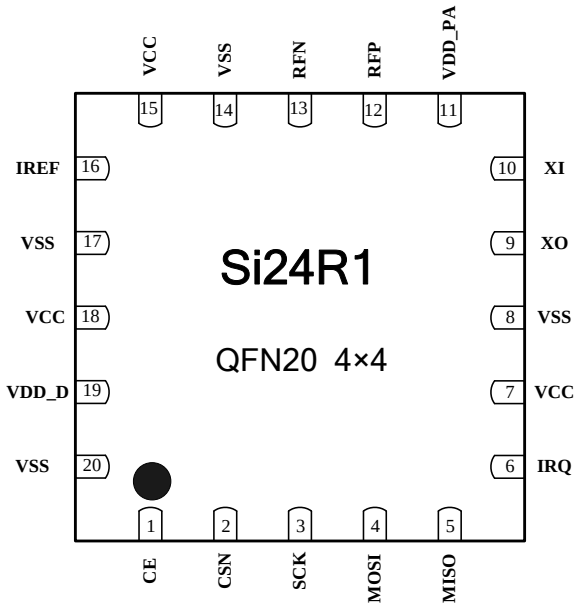


Figure 2-1 Si24R1 pin information（QFN20 4×4 package）

Table 2.1 pin function

Pin	Name	Type	Pin function
1	CE	DI	Chip Enable Activates RX or TX mode
2	CSN	DI	SPI Chip Select
3	SCK	DI	SPI Clock
4	MOSI	DI	SPI Slave Data Input
5	MISO	DO	SPI Slave Data Output
6	IRQ	DO	Maskable interrupt pin. Active low
7，15，18	VCC	Power	Power supply（+1.9～+3.6V，DC）
8，14，17，20	VSS	Power	Ground（0V）
9	XO	AO	Crystal oscillator output
10	XI	AI	Crystal oscillator input
11	VDD_PA	Power	1.8V power supply output for the internal Power Amplifier
12	RFP	RF	Antenna port 1
13	RFN	RF	Antenna port 2
16	IREF	AI	Reference current
19	VDD_D	PO	Internal digital supply output for de-coupling purposes
	Die exposed	Power	Ground（0V），connect die exposed to PCB ground

3 Operational modes

3.1 State Control Diagram

The Si24R1 has a built-in state machine that controls the transitions between the chip's different operating modes.

The state diagram in Figure3-1 shows the operating modes and how they function. There are five operating modes: Shutdown、Standby、Idle-TX、TX and RX.

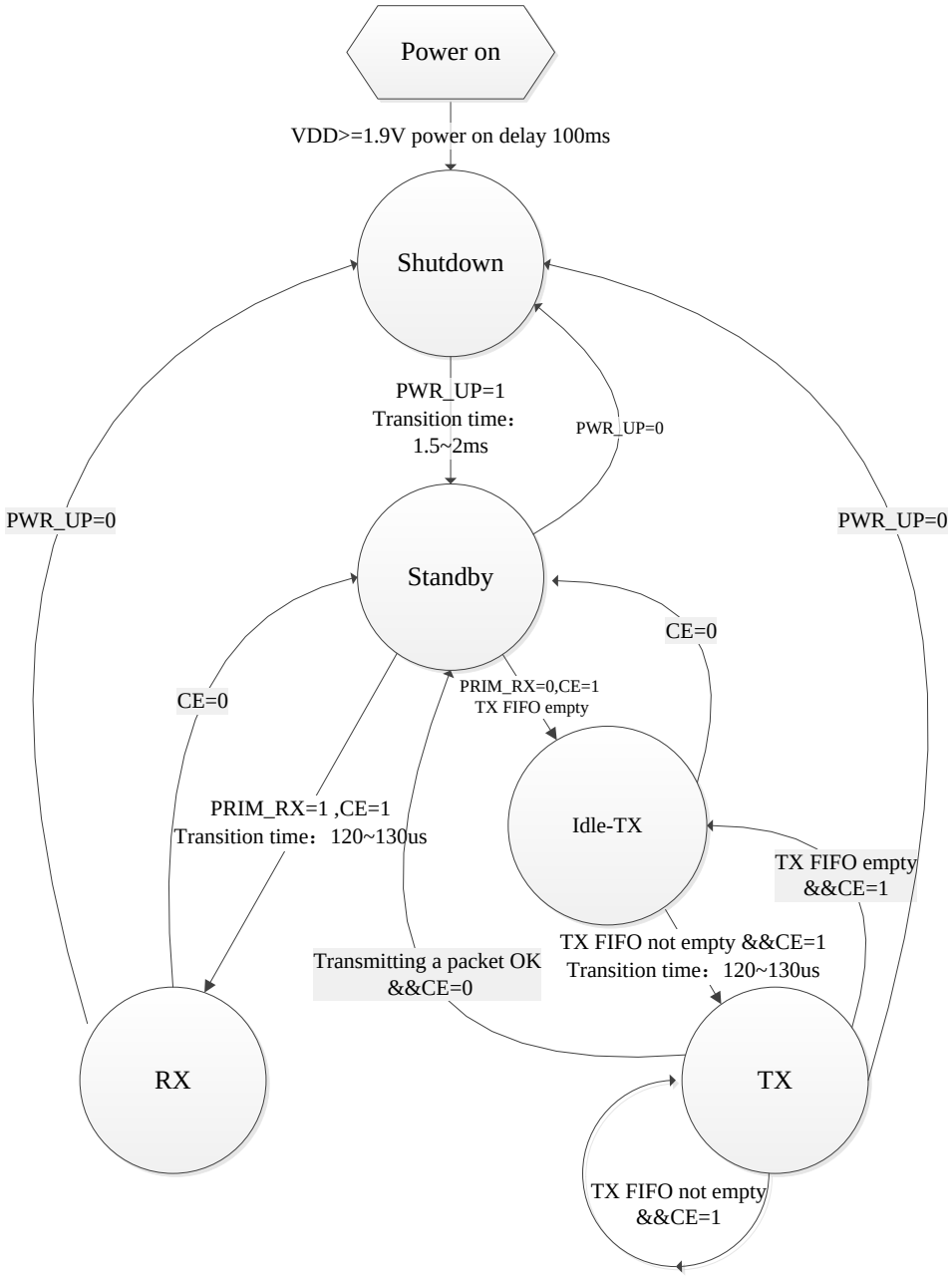


Figure 3-1 Si24R1 state control diagram

3.1.1 Shutdown Mode

In Shutdown mode Si24R1 is disabled using minimal current consumption, and the function of data transmitting and receiving is stopped. All register values available are maintained and can be written or read by SPI which is kept active. Shutdown mode is entered by setting the PWR_UP bit in the CONFIG register low.

3.1.2 Standby Mode

In Standby mode only part of the crystal oscillator is active. Standby mode is used to minimize average current consumption while maintaining short start-up times. Standby mode is entered after the crystal oscillator works stably by setting PWR_UP bit in the CONFIG register to 1. The crystal oscillator startup time is about 1.5~2ms, which is related to the performance of the crystal oscillator. The Si24R1 enters Idle-TX or RX mode by setting CE high. When CE pin is set low, Si24R1 returns to Standby mode from Idle-TX mode, TX or RX mode.

3.1.3 Idle-TX Mode

In Idle-TX mode, the crystal oscillator and clock buffers are active and more current is used compared to Standby mode. Si24R1 enters Idle-TX mode if CE is held high on a PTX device with an empty on TX FIFO. If a new packet is uploaded to the TX FIFO, the internal circuits will be active immediately, Si24R1 enters TX mode and the packet is transmitted.

Both in Standby and Idle-TX mode all register and FIFO values are maintained and can be written or read by SPI.

3.1.4 TX Mode

The TX mode is an active mode for transmitting packets. To enter this mode, Si24R1 must have PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and a high pulse on the CE pin for more than 10us.The transition time from Idle-TX mode to TX mode takes 120us~130us, but will not more than 130us. Si24R1 stays in TX mode until it finishes transmitting a packet. If CE = 1, the status of TX FIFO determines the next action. If the TX FIFO is not empty the Si24R1 remains in TX mode and transmits the next packet. If the TX FIFO is empty the Si24R1 goes into Idle-TX mode. If CE = 0, Si24R1 returns to Standby mode. The Si24R1 provides a TX interrupt after finishing transmitting a packet.

3.1.5 RX Mode

The RX mode is an active mode where Si24R1 is used as a receiver. To enter this mode, Si24R1 must have PWR_UP bit, PRIM_RX bit and the CE pin set high. The transition time from Standby mode to RX mode is 120us~130us. If a valid packet is found(by a matching address and a valid CRC)the payload of the packet is presented in a vacant slot in the RX FIFOs, and generate a data reception interrupt. Si24R1 can store 3 valid packets at most, if FIFOs are full, the received packet is discarded.

In RX mode the power of received signal is available by RSSI register. When a RF signal higher than -60dBm is detected inside the receiving frequency channel, the RSSI bit of RSSI register will be set high, otherwise RSSI bit set low. There are two methods for updating RSSI register. When a valid packet is received, then RSSI will be updated automatically. In addition, when chip enters Standby mode from RX mode, RSSI also will be updated. The value of RSSI varies with temperature, within ±5dbm.

4 Packet processing protocol

Si24R1 is based on packet communication and supports stop-and-wait ARQ protocol. Internal ARQ baseband protocol engine can realize automatic ACK and NO_ACK packet handling without the involvement of MCU. ARQ baseband supports the handling of 1 to 32 bytes dynamic payload length which is inside the packet. Besides, it supports static payload length which is set by registers. Baseband handling features automatic packet disassembly and assembly, automatic acknowledgement and retransmissions of packet. It also has 6 data pipes for 1:6 star networks.

4.1 ARQ packet format

A whole packet contains a preamble, address, packet control, payload and CRC field. Figure4-1 shows the packet format with MSB to the left.

Figure 4-1 A whole ARQ packet

The preamble is used to synchronize the receivers demodulator to the incoming bit stream. It is automatically attached when transmitting and added by transmitter and discarded by receiver, and shielded for users.

The address field stores the packet address values for the receiver. A packet will be received only when the address of the packet matches the address of the receiver. The address field width in the AW register can be configured to be 3, 4 or 5 bytes.

ATTENTION：The highest byte of the address shall not be set to 0xFF、0x00、0xA5、0x5A、0xAA、0x55, or it may lead to receiving failure.

Figure 4-2 shows the format of the 9 bit packet control field.

Figure 4-2 Format of packet control field

The 6 bit payload length specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

For example：000000 = 0 byte (no payload)

100000 = 32 byte (32 bytes of payload)

The PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once. The PID field is incremented at the TX side for each new packet received and write FIFO through the SPI. The PID and CRC fields are used by the PRX device to determine if a packet is retransmitted or new. If a packet has the same PID as the previous packet, Si24R1 compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

When NO_ACK bit is 1, it indicates telling the receiver that the packet is not to be auto acknowledged. For the transmitter, to set NO_ACK bit high must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit, and set the NO_ACK flag bit in the packet control field with this command: W_TX_PAYLOAD_NOACK. The PRX does not transmit an ACK packet when it receives this packet, even if it is working in ACK mode.

The payload is the user defined content of the transmitted packet. It can be up to 32 bytes.

The CRC field is the mandatory error detection mechanism in the packet. It is either 1 or 2 bytes, and the number of bytes is set by the CRCO bit in the CONFIG register.

4.2 ARQ communication mode

In the TX mode the PTX device assembles the preamble, address, packet control field, payload and CRC to make a complete packet first and then transmits the packet with RF module.

In the RX mode the receiver constantly searches for a valid packet by a matching address and a valid CRC. After the packet is validated, the receiver disassembles the packet and loads the payload into the RX FIFO and generates interrupt to assert the MCU. MCU can read data in the RX FIFO register through SPI at any time.

4.2.1 ACK mode

When write the data to the TX FITO using the W_TX_PAYLOAD command, the NO_ACK flag bit in the packet control field is reset after the data is packaged. After receiving a frame of valid data, the PRX asserts RX_DR interrupt and automatically send a frame of ACK signal. When receiving the ACK signal, the PTX automatically clears the TX FIFO and generates TX_DS transmission interrupt, then the communication is successful.

To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX

takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 and as the pipe address for the designated pipe.

If the PTX does not receive the ACK signal within ARD time, it will retransmit the last frame data. If the number of retransmissions exceeds the programmed maximum limit(ARC) and still not receive an ACK packet, the PTX will generate MAX_RT interrupt. No further packets can be transmitted before MAX_RT interrupt is cleared. All interrupts are cleared by writing to the STATUS register. The PLOS_CNT register is incremented at each MAX_RT interrupt, and is used to count the total number of transmissions since the last channel change. The ARC_CNT register counts the number of retransmissions for the current transaction, and can be reset by initiating a new transaction. The number of times it is allowed to retransmit and Auto Retransmit Delay can be set by the ARC bit and ARD bit in the SETUP_RETR register. The Auto Acknowledgement feature is enabled by setting the EN_AA register.

Figure 4-3 shows a complete communication in ACK mode.

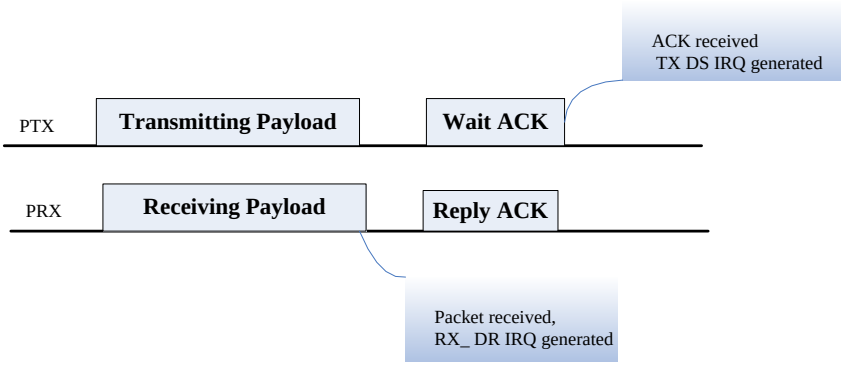


Figure 4-3 ACK mode

The PID field is incremented at the TX side for each new packet received, so the PIDs in the two adjacent data packets sent should be different from each other. If several data packets are lost on the link, the PID fields may become equal to the last received PID.

If the PRX detects a packet has the same PID as the previous packet, then compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded, and the ACK signal is replied again. Figure 4-4 shows the PTX device did not receive the ACK signal for the first data transmission. The ACK signal was received after retransmission, and the data communication was completed.

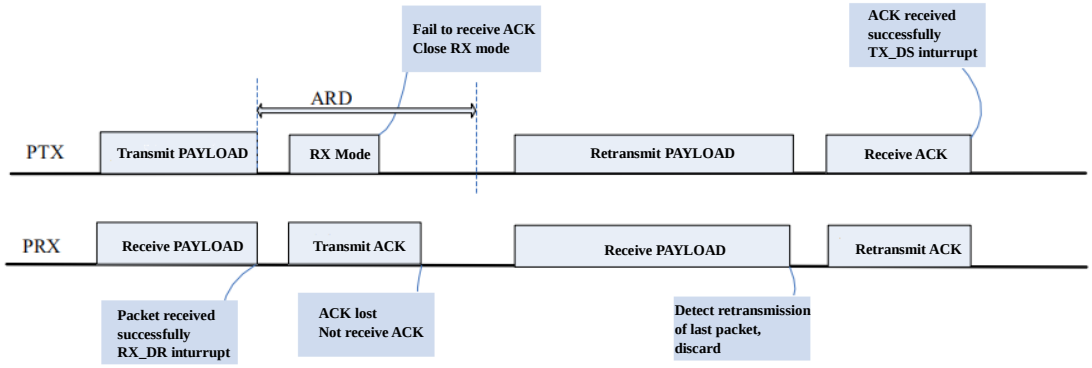


Figure 4-4 Communication mode of without ACKPAYLOAD

When PRX responds to the ACK signal, it can send an Auto Acknowledgement with payload data(ACKPLAYLOAD). In order to enable this function, the EN_ACK_PAY bit in the FETURE register must be set, and TX/RX must enable the dynamic payload length.

The PRX first uses W_ACK_PAYLOAD command to write the ACKPLAYLOAD corresponding to the receiving data pipe to the TX FIFO. When this pipe receives a new valid data, generates RX_DR interrupt and the ACK is automatically replied. The ACKPAYLOAD is automatically packaged and sent to the PTX. For the PTX both the TX_DS and RX_DR interrupt are asserts after receiving the ACK packet. When the PRX receives a packet of valid data sent by PTX again, it means the PTX has received ACKPLAYLOAD. Clear the data in the TX FIFO, and generate RX_DR and TX_DS interrupts at the same time. If the received data is a retransmission of the previous packet, repackage this ACKPAYLOAD and send it out as an ACK signal. Figure 4-5 shows the PTX device did not receive the ACK signal with ACKPAYLOAD after the first transmission and retransmitted. Then PRX packaged the ACKPLAYLOAD again, and the PRX sent the next packet after receiving it.

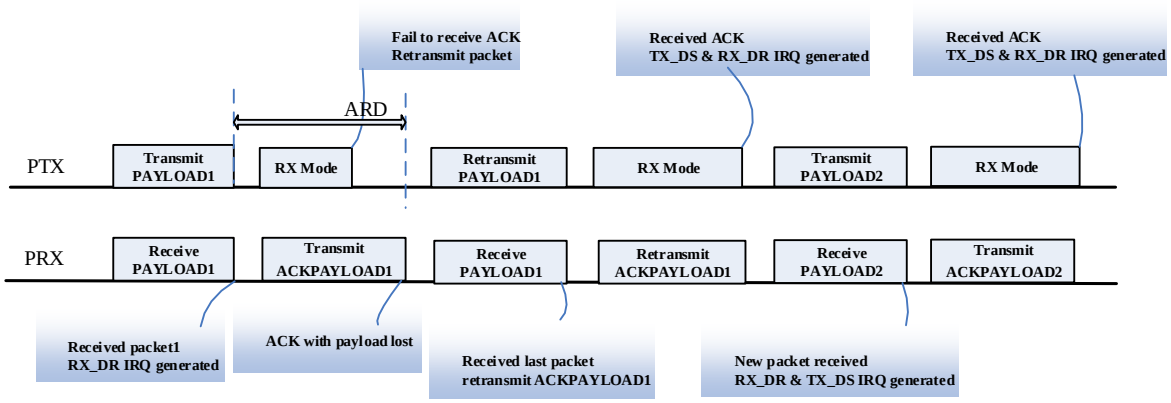


Figure 4-5 Communication mode of with ACKPAYLOAD

4.2.2 NOACK Mode

On the PTX you can set the NO_ACK flag bit in the Packet Control Field with this command: W_TX_PAYLOAD_NOACK. After sending a packet of data, generates TX_DS interrupt immediately, and start to prepare transmitting next packet of data. After receiving data, the PRX checks if the NO_ACK flag is set and the data is valid, then generates RX_DR interrupt. It is means that a frame of data communication is finished and the PRX does not need to transmit an ACK packet. Additionally, the EN_DYN_ACK bit in FEATURE register must be set before using W_TX_PATLOAD_NOACK command.

4.2.3 Dynamic payload length (DPL) and static payload length

A PTX device with DPL enabled must have the EN_DPL bit in FEATURE register and the DPL_P0 bit in DYNPD register set. The first 6 bits in the control field of the packaged data are the length of the data for sending.

The PRX set the EN_DPL bit in FEATURE register, and enable the pipe of DYNPD register. It will receive data according to the length control field. Thus, every time when receiving payload data, its length can be different. MCU can read out the payload length by using R_RX_PL_WID command. If it is static payload length by default, the payload length on the transmitter side must be the same every time, and must equal the value in the RX_PW_Px register on the receiver side.

4.2.4 Multi data pipes communication

Up to six Si24R1 configured as PTX can communicate with one Si24R1 configured as a PRX at the same time. At this time, PRX should enable data pipes with the bits in the EN_RXADDR register, and set data pipe address of PRX same as the TX address of the corresponding PTX. Data pipe 0 has a unique 5 bytes address, data pipes 1-5 share the four most significant address bytes.

If the PTX needs to receive ACK signal, the RX address for data pipe 0 (RX_ADDR_P0) must be equal to the TX address (TX_ADDR) in the PTX device

Figure 4-6 is an example of an address configuration for the PRX and PTX with Multi data pipes communication.

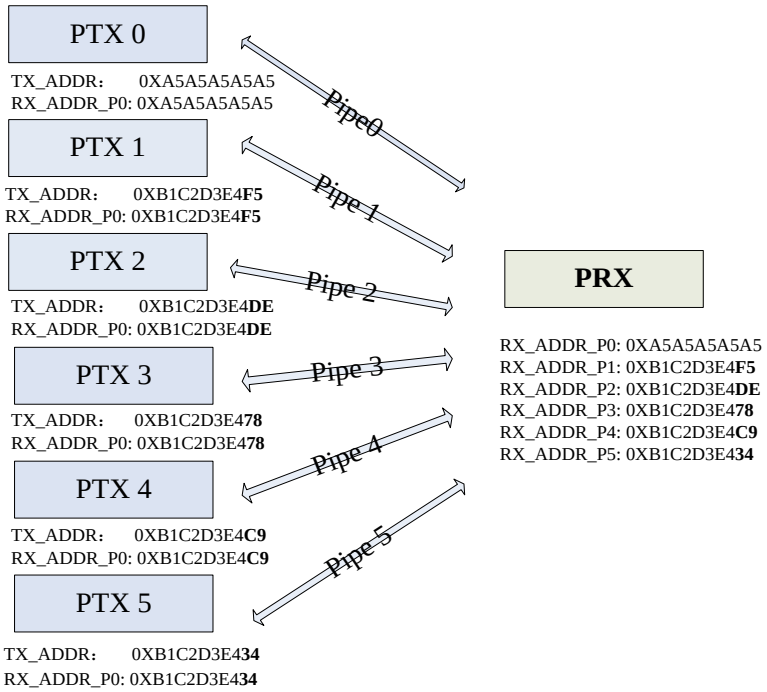


Figure 4-6 Multi pipes receiver example

The multi pipes operation can directly support 1:6 star networks at most.

5 SPI Interface

The SPI interface is a standard 4-wire SPI with a maximum data rate of 10Mbps.MCU can configure the Si24R1 through SPI interface, including R/W register、read and write FIFO、read the status of Si24R1 and clear the interrupts etc.

5.1 SPI Commands

Table 5-1 shows the SPI commands, and every new command must be started by a high to low transition on CSN pin. Every time a SPI operation, the first byte output by MISO is the value of the STATUS register, then the command determines whether to output the value or not (never output HRS value).

- <Command word: MSBit to LSBit > -- one byte
- <Data bytes: LSByte to MSByte, MSBbit in each byte first >

  See Figure 5-1 & Figure 5-2 for timing information.

Table 5-1 SPI Commands

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read register command. AAAAA= 5 bit Register address (refer to register table)
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write register command. AAAAA= 5 bit Register address (refer to register table) Executable in Shutdown、Standby or Idle-TX modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX payload:1- 32 bytes, used in RX mode.LSB is first read out.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX payload:1-32 bytes, used in TX mode. LSB is first write in.
FLUSH_TX	1110 0001	0	Flush TX FIFO , used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode. Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device. Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed.

R_RX_PL_WID	0110 0000	1	Read RX payload width of the top RX FIFO
W_ACK_ PAYLOAD	1010 1PPP	1 to 32 LSByte first	Used for PRX Write payload to be transmitted with ACK packet on pipe PPP. Allow 3 frames of data storage in FIFO at most
W_TX_PAYLOAD _NOACK	1011 0000	1 to 32 LSByte first	Used in TX mode. AUTOACK should be set 1 when using this command
NOP	1111 1111	0	No operation. Might be used to read the STATUS Register.

5.2 SPI Timing

SPI operation includes basic Read/Write operation and other command operation. Figure 5-1 and Figure 5-2 show the SPI timing.

ATTATION:Si24R1 must be in Shutdown/Standby/Idle-Tx mode before writing to the configuration registers.

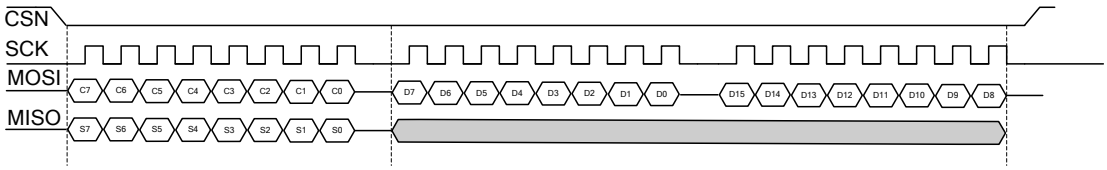


Figure 5-1 SPI write operation

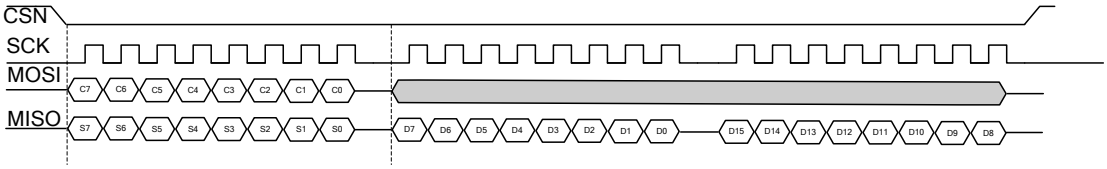


Figure 5-2 SPI read operation

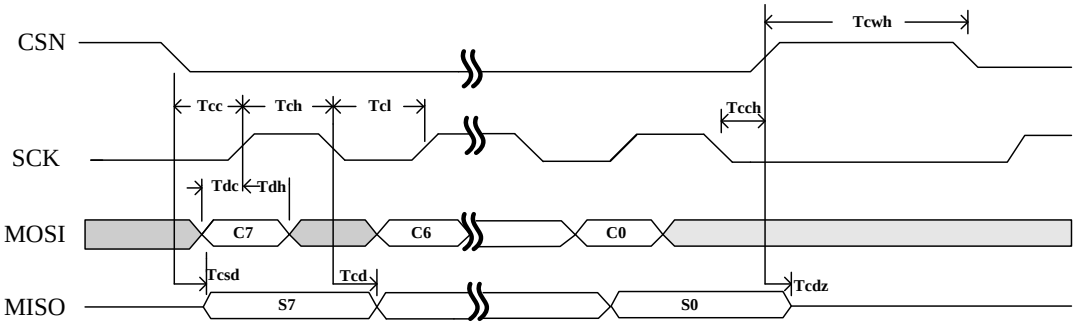


Figure 5-3 SPI typical timing

Table 5-2 shows SPI Interface typical timing parameter

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns

Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

6 Register Table

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only ‘0’ allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high 0: close CRC 1: open CRC
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' - 2 bytes
	PWR_UP	1	0	R/W	Power up/down control 1: POWER UP 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control, only be changed in Shutdown/ Standby mode 1: RX, 0: TX
01	EN_AA				Enable Auto Acknowledgment Function
	Reserved	7:6	00	R/W	Reserved, only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0

02	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Reserved, only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3
	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	1	R/W	Enable data pipe 1
	ERX_P0	0	1	R/W	Enable data pipe 0
03	SETUP_AW				Setup of Address Widths
	Reserved	7:2	000000	R/W	Reserved, only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width 00: illegal 01:3 bytes 10:4 bytes 11: 5 bytes
04	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmission Delay0 0000: Wait 250uS 0001: Wait 500uS 0010: Wait 750uS …… 1111: Wait 4000uS
	ARC	3:0	0011	R/W	Auto Retransmit Count 0000: Retransmit disabled 0001: Up to 1 Re-Transmission 0010: Up to 2 Re-Transmission …… 1111: Up to 15 Re-Transmission
05	RF_CH				RF Channel
	Reserved	7	0	R/W	Reserved, only ‘0’ allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel, corresponding to the 0~125th channel respectively Channel’s interval is 1MHz, by default, 02 means 2402MHz
06	RF_SETUP				RF Setup
	CONT_WAVE	7	0	R/W	1: Continuous carrier transmit, for test only
	Reserved	6	0	R/W	Reserved, only ‘0’allowed

	RF_DR_LOW	5	0	R/W	Set RF Data Rate. See RF_DR_HIGH for encoding
	PLL_LOCK	4	0	R/W	Reserved bit, only ‘0’allowed
	RF_DR_HIGH	3	1	R/W	Set RF Data Rate [RF_DR_LOW, RF_DR_HIGH]: 00: 1Mbps 01: 2Mbps 10: 250kbps 11: Reserved
	RF_PWR	2:0	110	R/W	Set RF output power in TX mode 111: 7dBm 110: 4dBm 101: 3dBm 100: 1dBm 011: 0dBm 010:-4dBm 001:-6dBm 000:-12dBm
07	STATUS				Status Register (In parallel to the SPI command word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin)
	Reserved	7	0	R/W	Reserved, only ‘0’ allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received Write 1 to clear bit
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt. Write 1 to clear bit
	RX_P_NO	3:1	111	R	Data pipe number for the payload available, it can be read through SPI 000-101: data pipe 0-5 110: unavailable 111: RX FIFO empty
	TX_FULL	0	0	R	TX FIFO full flag 1: TX FIFO full. 0: Available locations in TX FIFO
08	OBSERVE_TX				Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH

	ARC_CNT	3:0	0	R	Count retransmitted packet. The counter is reset when transmission of a new packet starts
09	RSSI				Received Power Detector
	Reserved	7:1	000000	R	
	RSSI	0	0	R	Received Power Detector： 0: Received Power is less than -60dbm
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2.Only LSB.MSB bytes are equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3, only LSB MSB bytes are equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4, only LSB MSB bytes are equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5, only LSB MSB bytes are equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSB byte is written first) Set RX_ADDR_P0 equal to this address and enable ARQ if PTX needs to receive ACK signal. ATTENTION：The highest byte of the address shall not be set to 0xFF、0x00、0xA5、0x5A、0xAA、0x55, or it may lead to receiving failure.
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Reserved, Only '00' allowed
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe0(1 to 32 bytes) 1: 1bytes …… 32: 32bytes
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Reserved, Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe

					1(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Reserved, Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Reserved, Only '00' allowed
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3(1 to 32 bytes) 0:not used 1: 1bytes …… 32: 32bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Reserved, Only '00' allowed
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4(1 to 32 bytes) 1: 1bytes …… 32: 32bytes
16	RX_PW_P5				
	Reserved	7:6	00	R/W	Reserved, Only '00' allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5(1 to 32 bytes) 1: 1bytes …… 32: 32bytes
17	FIFO_STATUS				FIFO Status
	Reserved	7	0	R/W	Reserved, only ‘0’ allowed

	TX_REUSE	6	0	R	Used for PTX, Reuse last transmitted data packet. TX_REUSE is set by the SPI command REUSE_TX_PL and is reset by SPI command W_TX_PAYLOAD or FLUSH_TX
	TX_FULL	5	0	R	TX FIFO full flag 1: TX FIFO full 0: TX FIFO not full
	TX_EMPTY	4	1	R	TX FIFO empty flag 1: TX FIFO empty 0: TX FIFO not empty
	Reserved	3:2	00	R/W	Reserved, only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag 1: RX FIFO full 0: RX FIFO not full
	RX_EMPTY	0	1	R	RX FIFO empty flag 1: RX FIFO empty 0: RX FIFO not empty
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Reserved, only '00' allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe5 (Requires EN_DPL & ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe4 (Requires EN_DPL & ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe3 (Requires EN_DPL & ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe2 (Requires EN_DPL & ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe1 (Requires EN_DPL & ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe0 (Requires EN_DPL & ENAA_P0)
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Reserved, only '00000' allowed
	EN_DPL	2	0	R/W	Enable dynamic payload length
	EN_ACK_PAY	1	0	R/W	Enable Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command

7 Electrical specification

7.1 Limitation parameter

Operating Condition	Min.	Max.	Unit
Supply Voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input Voltage			
VI	-0.3	5.25	V
Output Voltage			
VO	VSS to VDD	VSS to VDD	V
Power Dissipation			
		100	mW
Temperatures			
Operation Temperature	-40	+85	℃
Storage Temperature	-40	+125	℃
ESD Performance	HBM(Human Body Model): Class 1C		

7.2 Electrical specification

Conditions: VDD = 3V, VSS = 0V , TA = 27℃ , Crystal oscillator C_L=12pF

Symbol	parameter	Min.	Typ.	Max.	Unit	Comment
OP Parameters						
VDD	Supply voltage	1.9		3.6	V	
I_{SHD}	Supply current in Shutdown mode		1		μA	
I_{STB}	Supply current in Standby mode		15		μA	
I_{IDLE}	Supply current in Idle-Tx mode		380		μA	
I_{RX}@2MHZ	RX mode supply current @2Mbps		15		mA	
I_{RX}@1MHZ	RX mode supply current @1Mbps		14.5		mA	
I_{RX}@250kbps	RX mode supply current @250kbps		14		mA	
I_{TX}@7dBm	TX mode supply current @7dBm output power		25		mA	
I_{TX}@4dBm	TX mode supply current @4dBm output power		16		mA	

I_{TX}@0dBm	TX mode supply current @0dBm output power		12		mA	
I_{TX}@-6dBm	TX mode supply current @-6dBm output power		9.5		mA	
I_{TX}@-12dBm	TX mode supply current @-12dBm output power		8.5		mA	
RF Parameter						
F_{OP}	RF operation frequency	2400		2525	MHz	
F_{CH}	RF channel interval	1			MHz	2MHz at least when 2Mpbs
ΔF_{MOD}(2Mbps)	Frequency deviation		±330		KHz	
ΔF_{MOD}(1M/250Kbps)	Frequency deviation		±175		KHz	
R_{GFSK}	Data rate	250		2000	Kbps	
RX Parameter						
RX_{SENS}@2Mbps	Sensitivity@2Mbps		-83		dBm	BER=0.1%
RX_{SENS}@1Mbps	Sensitivity@1Mbps		-87		dBm	BER=0.1%
RX_{SENS}@250Kbps	Sensitivity@250kbps		-96		dBm	BER=0.1%
C/I_{CO}@2Mbps	C/I Co-channel 2Mbps		6		dB	
C/I_{1st}@2Mbps	1st ACS C/I 2MHz		0		dB	
C/I_{2ND}@2Mbps	2nd ACS C/I 4MHz		-20		dB	
C/I_{3RD}@2Mbps	3rd ACS C/I 6MHz		-26		dB	
C/I_{CO}@1Mbps	C/I Co-channel 1Mbps		7		dB	
C/I_{1st}@1Mbps	1st ACS C/I 2MHz		6		dB	
C/I_{2ND}@1Mbps	2nd ACS C/I 4MHz		-21		dB	
C/I_{3RD}@1Mbps	3rd ACS C/I 6MHz		-30		dB	
TX Parameter						
P_{RF}	RF Output Power	-30		7	dBm	
P_{BW}@2Mbps	Bandwidth for modulated carrier		2.1		MHz	
P_{BW}@1Mbps	Bandwidth for modulated carrier		1.1		MHz	
P_{BW}@250Kbps	Bandwidth for modulated carrier		0.9		MHz	
P_{RF1}	1stAdjacent Channel Transmit Power 2MHz			-20	dBm	
P_{RF2}	2ndAdjacent Channel Transmit Power 4MHz			-46	dBm	
Crystal Oscillator Parameter						
F_{XO}	Crystal frequency		16		MHz	
ΔF	Frequency tolerance		±60		ppm	
ESR	Equivalent Series Resistance		100		Ω	

8 Package

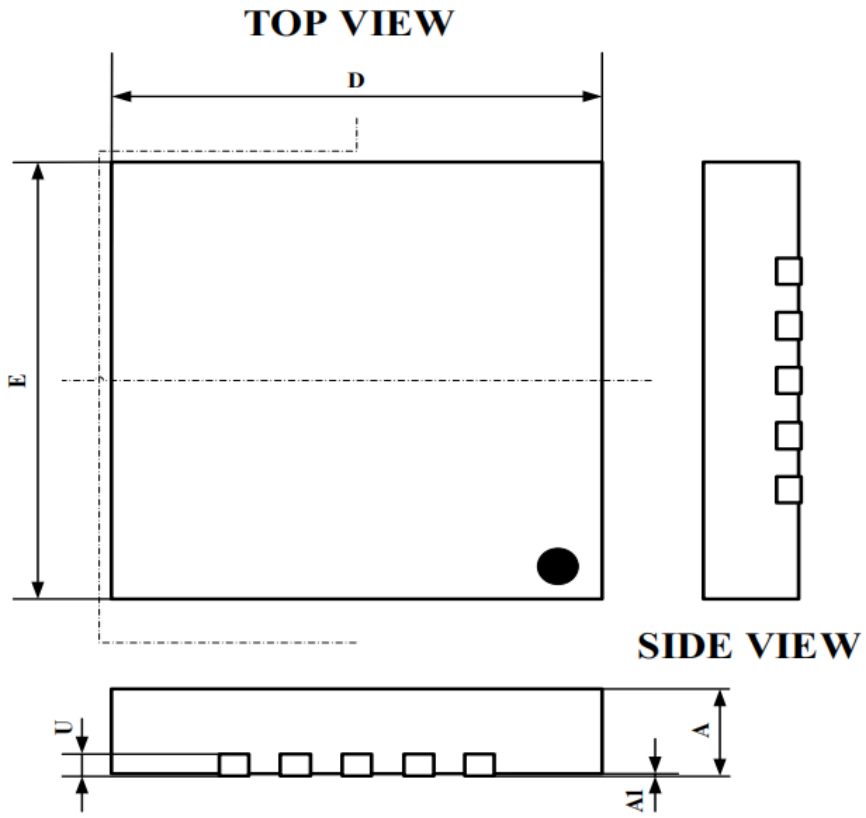


Figure 8-1 Top view

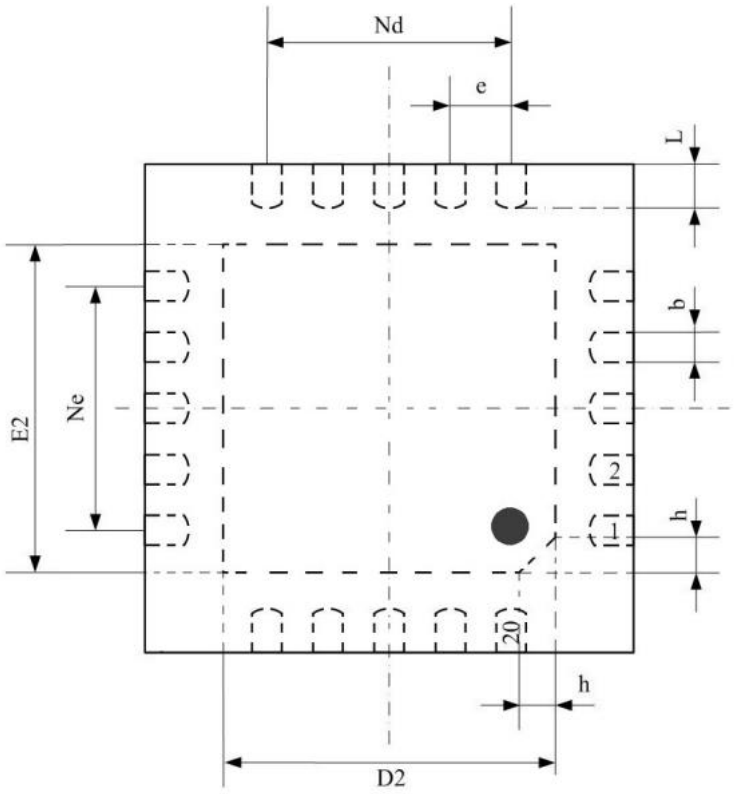


Figure 8-2 Package measurement (Top view)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
e	0.50BSC		
E2	2.55	2.65	2.75
E	3.90	4.00	4.10
Ne	2.00BSC		
Nd	2.00BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40
U	0.20 REF.		
L/F (mil)	114×114		

Table 8-2 Package measurement

9 Typical Application Schematic

9.1 Typical Application Schematic

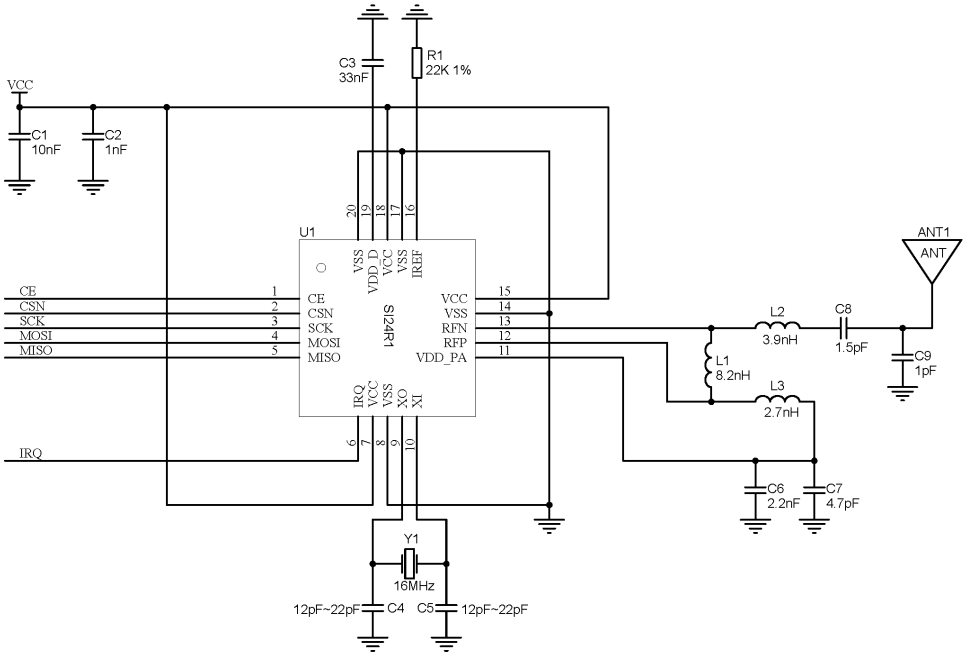


Figure 9-1 Typical application schematic

Designator	Part	Footprint	Description
C1	100uF	0402	X7R, +/- 10%
C2	1nF	0402	X7R, +/- 10%
C3	33nF	0402	X7R, +/- 10%
C4	12~22pF	0402	NPO, +/- 2%
C5	12~22pF	0402	NPO, +/- 2%
C6	2.2nF	0402	X7R, +/- 10%
C7	4.7pF	0402	NPO, +/- 0.25pF
C8	1.5pF	0402	NPO, +/- 0.1pF
C9	1.0pF	0402	NPO, +/- 0.1pF
L1	8.2nH	0402	chip inductor, +/- 5%
L2	3.9nH	0402	chip inductor, +/- 5%
L3	2.7nH	0402	chip inductor, +/- 5%
R1	22KΩ	0402	+/- 1%
R2	Not mounted	0402	
Y1	16MHz		+/-60ppm, CL=12pF
U1		QFN20 04×04	

Table 9-1 Recommended components (BOM)

* When the system cannot supply stable voltage, such as using button battery to power supply. It is recommended to use 100uF capacitor to stabilize the voltage. Meanwhile, the capacitor should not have a large leakage current.

Pin CE，CSN，SCK，MOSI，MISO，IRQ are the interface to MCU. When MCU does not operate Si24R1, output pin MISO and IRQ are floating, input pin CE，CSN，SCK，MOSI must connect the power or ground through MCU interface.

9.2 PCB layout

As shown in the figure below is the PCB layout example for the typical application schematic Figure 9-2. A double-sided FR-4 board is used. There is a copper clad surface on the top and bottom layers respectively, the copper clad surfaces of the top and bottom layers are connected by a large number of vias, and there is no copper clad surface under the antenna. The bottom layer of PCB is the ground plane. To ensure better RF performance, die exposed at the bottom of the IC is recommended to connect to PCB ground plane. It is strongly recommended to keep it connected.

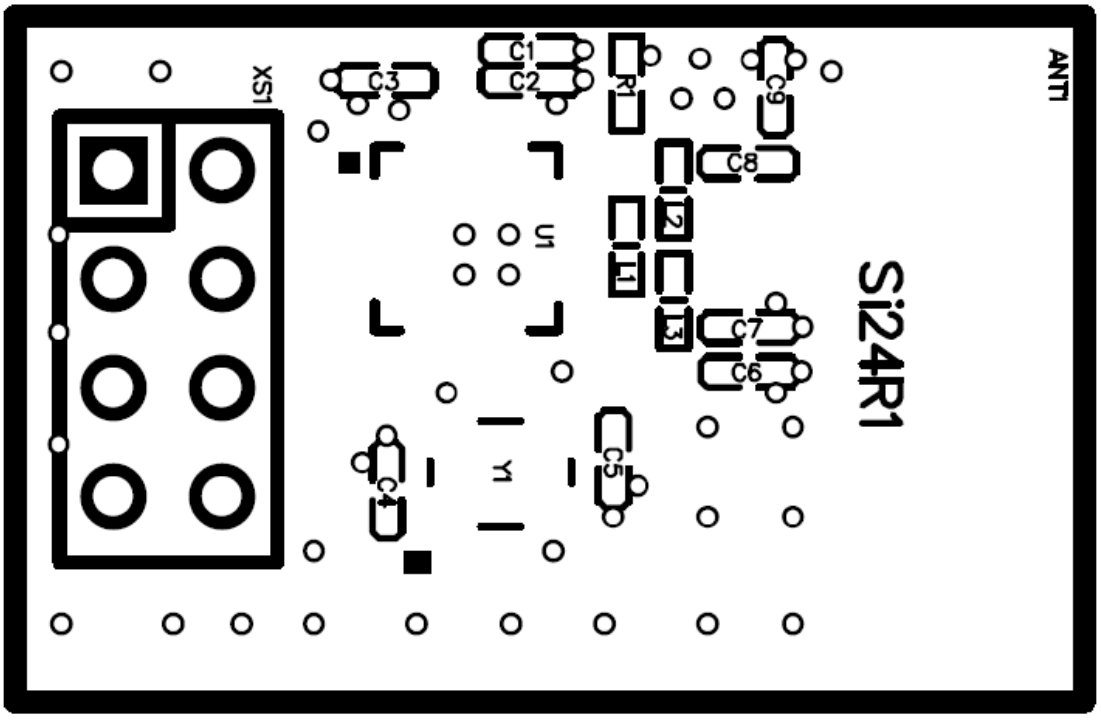


Figure 9-2 Top overlay（0402 size passive components）

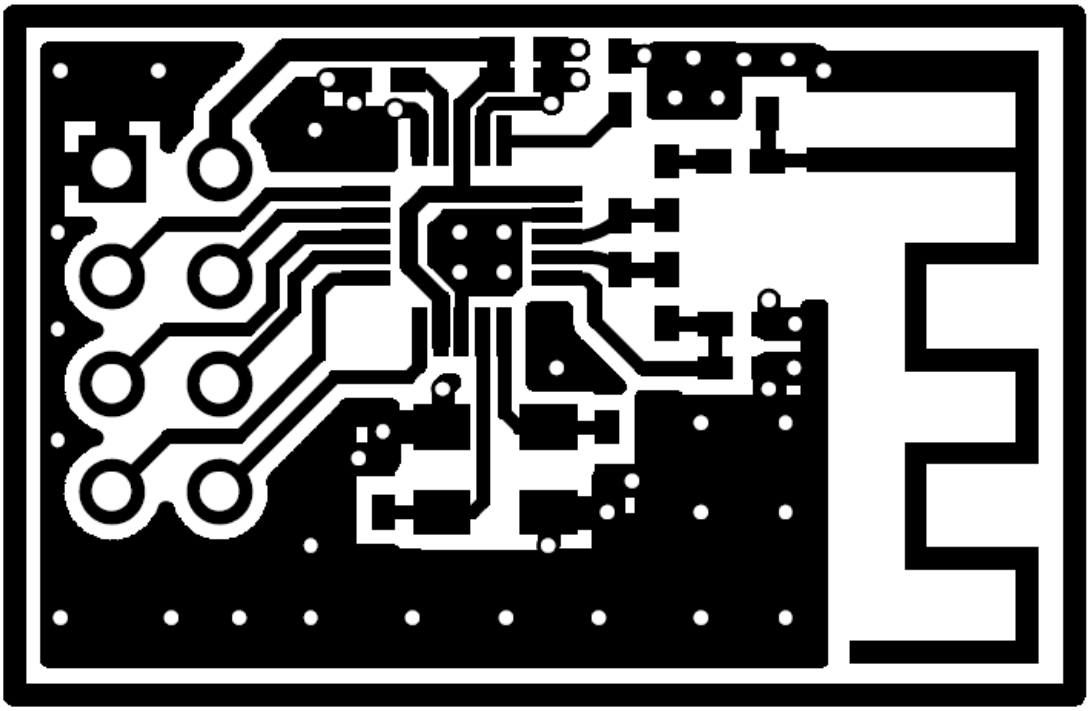


Figure 9-3 Top layer（0402 size passive components）

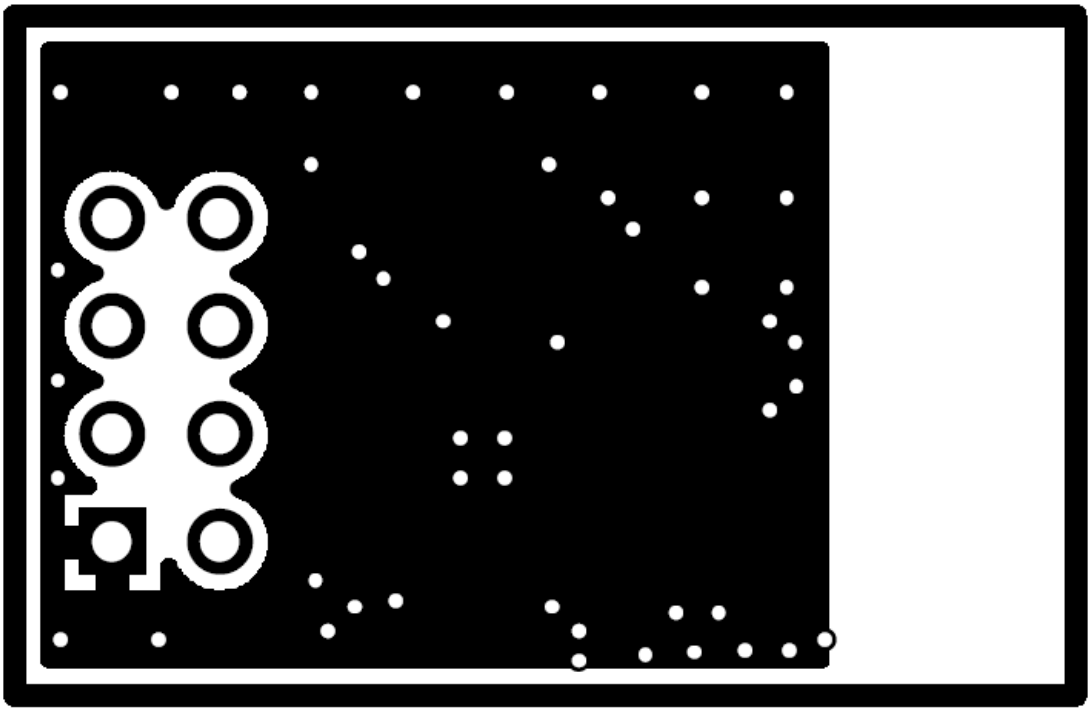


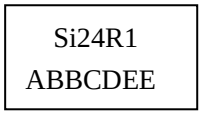
Figure 9-4 Bottom layer

10 Version Information

Version	Modified date	Modified content
V1.0	2023/11/13	First draft
V1.1	2024/03/19	Add description of address to ARQ packet format and register 0x10
V1.2	2024/04/03	Modify the description of PID in packet format

11 Order Information

Package marking



Si24R1: chip code

A: package date code, 5 represents year 2020

BB: week of sending out processing, 42 represents in the year A the 42th week

C: package factory code, A、HT、NJ or WA, can also abbreviated as A、H、N or W

D: test factory code, A、Z or H

EE: production batch code

order code	package	container	minimum
Si24R1-Sample	4×4mm 20-pin QFN	Box/Tube	5
Si24R1	4×4mm 20-pin QFN	Tape and reel	4K

Table 11-1 Si24R1 order example

12 Technical Support and Contact Information

Nanjing Zhongke Microelectronic Industry Technology Research Institute Co., Ltd
Technical Support Center
Phone: 025-68517780
Address: Room 201, Building B, Research Zone 3, Xuzhuang Software Park, Xuanwu District, Nanjing, Jiangsu, China
Website: http://www.csm-ic.com

Sales and Marketing
Phone: 13645157034, 13645157035
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Technical Support
Phone: 13645157034
Email: supports@csmic.ac.cn

Appendix A - Configuration and communication example

MODE 1: ACK MODE

PTX Configuration:

```
spi_rw_reg(SETUP_AW, 0x03);          // configure address width 5 bytes
spi_write_buf(TX_ADDR, TX_ADDRESS, 5);          // write in TX address, 5 bytes
spi_write_buf(RX_ADDR_P0, TX_ADDRESS, 5);    //address of pipe0 is the same with TX address
spi_write_buf(W_TX_PAYLOAD, buf, TX_PLOAD_WIDTH);       // write data in TX FIFO
spi_rw_reg(FEATURE, 0x04);      //Enable dynamic payload length
spi_rw_reg(DYNPD, 0x01);       //enable DPL_P0
spi_rw_reg(SETUP_RETR, 0x15);         //configure ARD=500us ,ARC=5
spi_rw_reg(RF_CH, 0x40);         // configure RF channel
spi_rw_reg(RF_SETUP, 0x0e);           // configure TX data rate=2Mbps and power
spi_rw_reg(CONFIG, 0x0e);          // set TX MODE, enable CRC and maskable interrupt
CE = 1;
```

PRX Configuration：

```
spi_write_buf(RX_ADDR_P0, TX_ADDRESS, 5);    // address of pipe0 is the same with RX address
spi_rw_reg(EN_RXADDR, 0x01);       //Enable data pipe 0 .
spi_rw_reg(RF_CH, 0x40);         // configure RF channel
spi_rw_reg(SETUP_AW, 0x03);    // configure address width:5 bytes
spi_rw_reg( FEATURE, 0x04);     //Enable dynamic payload length
spi_rw_reg(DYNPD, 0x01);     // enable DPL_P0
spi_rw_reg(RF_SETUP, 0x0e);     // configure TX data rate=2Mbps and power
spi_rw_reg(CONFIG, 0x0f);          // set RX MODE, enable CRC and maskable interrupt
CE = 1;
```

MODE 2 : NOACK MODE

PTX Configuration:

```
spi_write_buf( TX_ADDR, TX_ADDRESS, 5);          // write in TX address
spi_rw_reg( FEATURE, 0x01);     // Enable W_TX_PAYLOAD_NOACK
spi_write_buf(W_TX_PAYLOAD_NOACK, buf, TX_PLOAD_WIDTH);    // write data in TX FIFO
spi_rw_reg(SETUP_AW, 0x03);          // configure PTX address width 5 bytes
spi_rw_reg( RF_CH, 0x40);         // configure RF channel 0x40
spi_rw_reg(RF_SETUP, 0x08);        // configure TX data rate=2Mbps
spi_rw_reg( CONFIG, 0x0e);       // set TX MODE, enable CRC and CRC length is 2bytes
CE = 1;
```

PRX Configuration：

```
spi_write_buf( RX_ADDR_P0, TX_ADDRESS, 5);    // write in RX address
spi_rw_reg( EN_RXADDR, 0x01);       // Enable data pipe 0
spi_rw_reg( RF_CH, 0x40);           // configure RF channel
spi_rw_reg( RX_PW_P0, TX_PLOAD_WIDTH);       //configure pipe 0 payload length
spi_rw_reg( RF_SETUP, 0x08);       // configure TX data rate=2Mbps, TX power=-18dbm
spi_rw_reg( CONFIG, 0x0f);          // set RX MODE, enable CRC and CRC length is 2bytes
CE = 1;
```

MODE 3: PRX turn on multiple pipes

Dynamic length payload:

```
spi_rw_reg(FEATURE, 0x04);
spi_rw_reg(DYNPD, 0x3F) ;      //enable all pipes dynamic payload length
spi_rw_reg(EN_RXADDR, 0x3F);       // enable all pipes
spi_rw_reg(RF_CH, 0x40);          // configure RF channel 0x40
spi_rw_reg(SETUP_AW, 0x03);    // configure address width 5 bytes
spi_rw_reg(CONFIG, 0x0B);       // set RX MODE
CE = 1;
```

Static length payload:

```
spi_rw_reg(RX_PW_P0, 0x20);    //configure data length of pipe0
spi_rw_reg(RX_PW_P1, 0x20);
spi_rw_reg(RX_PW_P2, 0x20);
spi_rw_reg(RX_PW_P3, 0x20);
spi_rw_reg(RX_PW_P4, 0x20);
spi_rw_reg(RX_PW_P5, 0x20);

spi_rw_reg(EN_RXADDR, 0x3F);      // enable all pipes
spi_rw_reg(RF_CH, 0x40);           // configure RF channel 0x40
spi_rw_reg(SETUP_AW, 0x03);    // configure PRX address width 5
spi_rw_reg(CONFIG, 0x0F);       // set RX MODE
CE = 1;
```