Programmable Multi-Channel PMIC

Advanced Datasheet

P9180A

Features

- Single 3.15-5.25V supply input
- 3 x SVID IMVP8/VR12.1 compatible 5A synchronous step-down switching regulator with DPU interface to support up to four additional 6A phases
- 2 x step-down switching controller with DPU interface to support up to four 6A phases
- 2 x 2.3A synchronous step-down switching regulators
- Programmable mode selection:
  - Automatic PWM/PFM mode transition for high efficiency at light load or
  - PWM-only mode for low noise applications
- 6 x 50-400mA linear regulators, LDO0-2 with optional pass switch feature
- 1 x ±550mA Vtt linear regulator
- 10-bit ADC monitors internal and external voltages, currents and temperature
- Host interface and system management
  - Interrupt controller with mask-able interrupts
  - Reset function
  - Power control state machine
  - Programmable sequencing of output rails
  - High speed I^{2}C interface (3.4Mbit/s)
- Programmable enable outputs for external switches
- 15 x GPIOs
- -40°C to +85°C operating temperature range
- Two thermally-enhanced package options:
  100-ld, 8mm x 8mm x 0.7mm dual-row QFN
  100-ld, 9mm x 9mm x 0.8mm dual-row GQFN or

Applications

- Mobile (phones, tablets etc.)
- General Embedded Applications
- Print Imaging & Multi-Function Printers
- µServers
- Storage
- Industrial & Embedded Systems

Description

The P9180A is a highly programmable, multiple channel Power Management Integrated Circuit (PMIC) designed for the Intel™ ATOM® SoC to meet the high performance requirements as well as to provide a high level of integration to minimize system board area and BOM cost.

The PMIC includes sub-systems for voltage regulation, power sequencing management, A/D conversion, GPIOs, PWMs and others. The P9180A device is controlled and programmed via an I^{2}C interface that operates in conjunction with the SoC. There is also a SerialVID (SVID) interface between the SoC and PMIC for handling VCC, VNN & VDDQ voltage rails control supporting the VR12.1 specification.

The P9180A is capable of providing current levels sufficient for entry level platforms with its internal regulators and is scalable to higher current requirements by adding IDT's unique Distributed Power Units (DPUs) (P9147/P9148) to source additional current for those DCDC rails.

Also included are 7 LDOs which are programmable over a wide output voltage range and offer output currents up to 550mA. These LDOs are designed for low noise, high PSRR and excellent transient response.

The default output voltages of all regulators as well as device sequencing can be programmed by OTP (at the factory) to adjust to nonstandard configurations. Contact IDT marketing for specific requirements.

Table of Contents

ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Voltage

PIN NAME		MAXIMUM RATING
LDO_VIN, LDO5_VIN, VGPIO0, LDO0_VO, LDO1_VO, LDO2_VO, LDO3_VO, LDO4_VO, LDO5_VO, DCD[0:2]_FB, DCD3_DIF, DCD3_DIO, DCD4_DIF, DCD4_DIO, GPIO[8:0]		-0.3 to 2.2 V
GPIO[14:9]		-0.3 to 3.6 V
DCD0_LX, DCD1_LX, DCD2_LX, DCD5_LX, DCD6_LX	DC (T>500ns)	-0.3 to 6.0 V
DCD0_LX, DCD1_LX, DCD2_LX, DCD5_LX, DCD6_LX	AC (T<500ns)	-1.2 to 6.5 V
All other pins		-0.3 to 6.0 V
ESD Rating	(HBM) Human Body Model (all pins)	±1500 V
	(CDM) Charged Device Model (all pins)	± 500 V
Latch-up	GPIO pins, Grade II	40 mA
	All other pins, Grade II	100 mA

Table 2 - Package Thermal Information

SYMBOL	DESCRIPTION	RATING		UNITS
	Thermal Resistances	QFN (NQG)	GQFN (NHG)	
θ_{JA}	Thermal Resistance Junction to Ambient	24.4	24.0	°C/W
θ_{JC}	Thermal Resistance Junction to Top of Case	21.7	19.3	°C/W
θ_{JB}	Thermal Resistance Junction to Board (1mm from package)	1.0	0.7	°C/W
T_J	Junction Temperature	-40 to +125		°C
T_A	Ambient Operating Temperature	-40 to +85		°C
T_{STG}	Storage Temperature	-55 to +150		°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300		°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: The thermal rating is calculated based on a JEDEC standard 2S2P 4-layer board (114 mm x 101 mm in still air condition with 2 oz. internal planes) and 5x5 mm EPAD solder down and a 25 thermal via array to the internal plane.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SYS}	PMIC Input voltage		3.15		5.25	V
V_{PVIN}	DCD0,1, 2, 5 & 6 Power Stage Input voltage		2.8		5.25	V
V_{IN_LDO}	LDO0 – 4 Input voltage		1.0	1.8	2.0	V
V_{IN_LDO5}	LDO5 Input voltage		1.2	1.35	1.5	V

Table 4: Overview of the Power Supplies

REGULATOR	I_{OUT_MAX} (A)	I_{OUT_MAX} with DPUs (A) [1,2]	V_{IN} RANGE (V) [3]	V_O RANGE (V)	C_O/L [5]
DCD0	5.0	29	V_{SYS} = $V_{IN\_DCD0,1,2}$ = 3.15 – 5.25V	SVID: 0.25 – 1.3V Non-SVID: 1.1 – 1.9V	Factory-enabled loadline (DCD0,1 default): C_O= 6 x 47µF; L=0.47µH Factory-disabled loadline (DCD2 default): C_O= 3 x 47µF; L=0.47µH See DPU datasheet for additional C_O
DCD1	5.0	29		SVID: 0.25 – 1.3V Non-SVID: 1.1 – 1.9V	
DCD2	5.0	29		SVID: 0.25 – 1.3V Non-SVID: 1.1 – 1.9V	
DCD3_CTRL	-	24	V_{SYS}=3.15 – 5.25	0.525 – 3.6	C_O= 3 x 47µF per DPU; See DPU datasheet for L
DCD4_CTRL	-	24	V_{SYS}=3.15 – 5.25	0.525 – 3.6	C_O= 3 x 47µF per DPU; See DPU datasheet for L
DCD5	2.3	-	V_{SYS} = V_{IN_DCD5} = 3.15 – 5.25V	0.525 – 3.375	C_O= 2 x 47µF; L=1.0µH
DCD6	2.3	-	V_{SYS} = V_{IN_DCD6} = 3.15 – 5.25V	0.525 – 3.375	C_O= 2 x 47µF; L=1.0µH
LDO0[4]	0.400	-	V_{LDO_VIN}=1.0 – 2.0	1.0 - 1.65	C_O= 2.2µF
LDO1[4]	0.400	-		1.0 - 1.65	C_O= 2.2µF
LDO2[4]	0.400	-		1.0 - 1.65	C_O= 2.2µF
LDO3	0.05	-		1.0 - 1.65	C_O= 1.0µF
LDO4	0.05	-		1.0 - 1.65	C_O= 1.0µF
LDO5	0.550	-	V_{LDO5_VIN}=1.2 – 1.5	V_{IN_LDO5}/2	C_O= 22µF
LDO6	0.1	-	V_{SYS}=3.15 – 5.25	1.20 – 3.55	C_O= 1.0uF
LDO7	0.1	-	V_{SYS}=3.15 – 5.25	1.80	C_O= 1.0uF

Note 1: Ensure that DPU's PVIN voltage is above PVIN UVLO (V_{UV}) before V_{SYS} reaches V_{SYS_MIN}.
Note 2: PWRBTNIN_B (or PMIC_EN when used) should not be asserted until DPU is powered on.
Note 3: During power up ensure that the voltage seen by VSYS is monotonic, which can be achieved by adding appropriate RC filter.
Note 4: Can be configured as a pass switch
Note 5: The output capacitor recommendation is with X5R, 20%, 0805 minimum case size. Derating of ceramic capacitor due to operating conditions, such as bias voltage and temperature, should be considered as part of the component selection.

PIN CONFIGURATION & DESCRIPTION

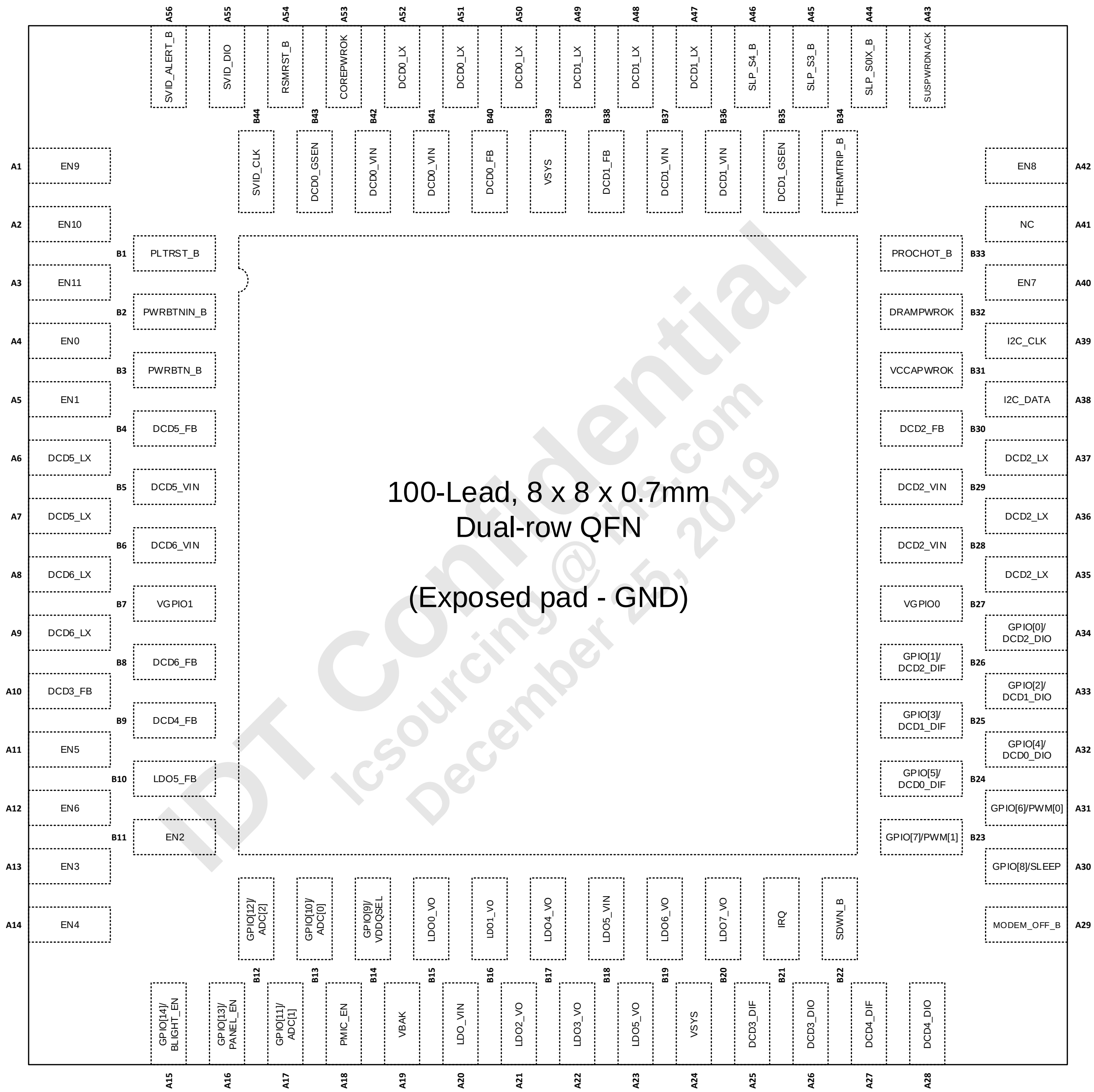


Figure 1: QFN (NQG) Package Pin Configuration (Top View)

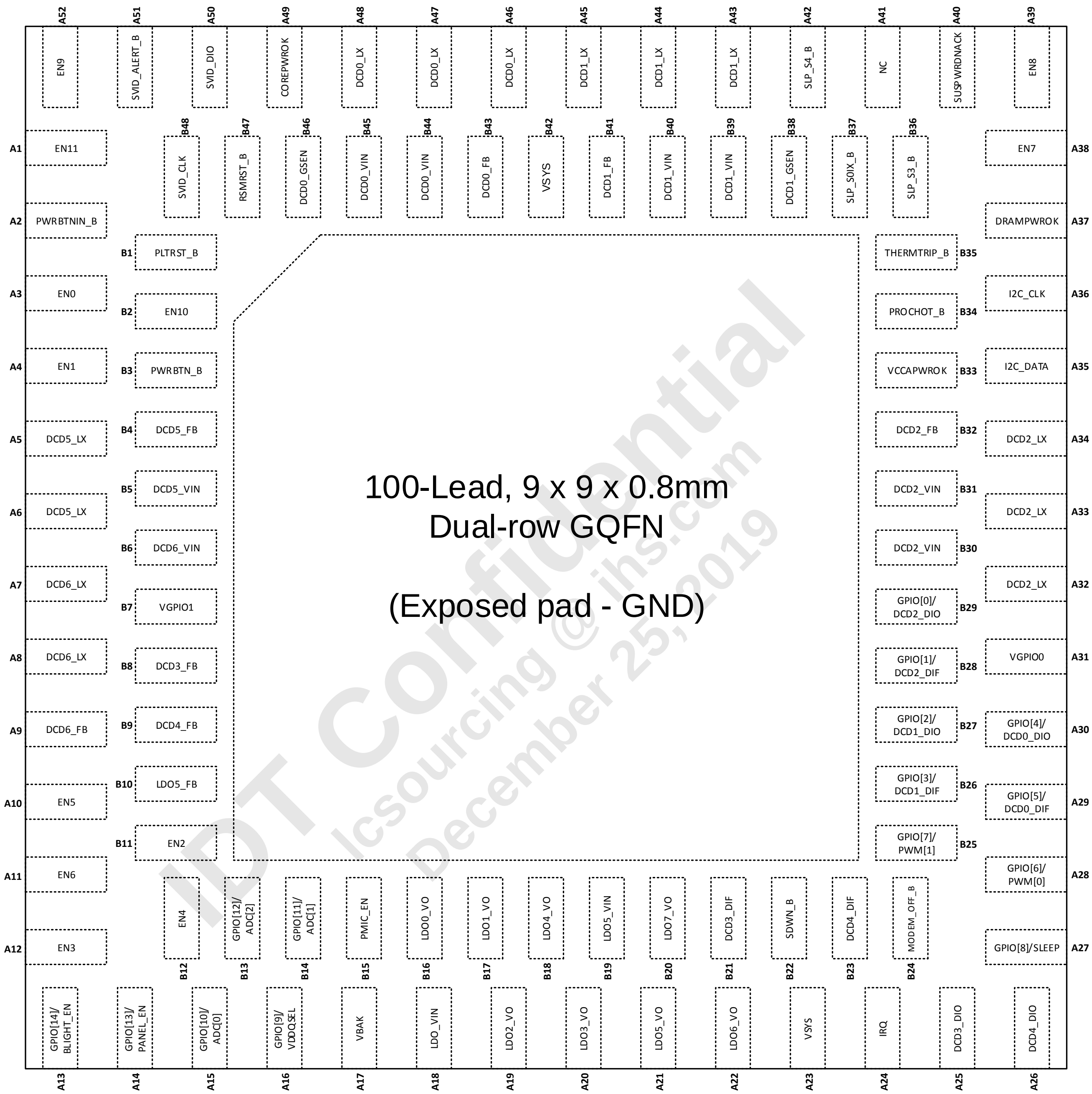


Figure 2: GQFN (NHG) Package Pin Configuration (Top View)

Table 5: Pin Descriptions

NQG(QFN)	NHG(GQFN)	LABEL	I/O	DESCRIPTION
A1	A52	EN9	O	Open drain output enable signal.
A2	B2	EN10	O	Open drain output enable signal.
A3	A1	EN11	O	Open drain output enable signal.
A4	A3	EN0	O	Open drain output enable signal.
A5	A4	EN1	O	Open drain output enable signal.
A6	A5	DCD5_LX	O	DCD5 switch node - this pin connects to the output inductor.
A7	A6	DCD5_LX	O	DCD5 switch node - this pin connects to the output inductor.
A8	A7	DCD6_LX	O	DCD6 switch node - this pin connects to the output inductor.
A9	A8	DCD6_LX	O	DCD6 switch node - this pin connects to the output inductor.
A10	B8	DCD3_FB	I	Feedback voltage for DCD3 controller. This pin must be connected to the output voltage of the P9180A.
A11	A10	EN5	O	Open drain output enable signal.
A12	A11	EN6	O	Open drain output enable signal.
A13	A12	EN3	O	Open drain output enable signal.
A14	B12	EN4	O	Open drain output enable signal.
A15	A13	GPIO[14]/BLIGHT_EN	I/O	General purpose input/output 14 or backlight enable output.
A16	A14	GPIO[13]/PANEL_EN	I/O	General purpose input/output 13 or LCD panel enable output.
A17	B14	GPIO[11]/ADC[1]	I/O	General purpose input/output 11 or ADC1 input.
A18	B15	PMIC_EN	I	PMIC enable input
A19	A17	VBAK	O	Coin cell backup battery connection.
A20	A18	LDO_VIN	I	Input supply voltage for LDOs 0, 1, 2, 3 and 4.
A21	A19	LDO2_VO	O	Linear regulator 2 output terminal.
A22	A20	LDO3_VO	O	Linear regulator 3 output terminal.
A23	A21	LDO5_VO	O	Source-sink regulator 5 output terminal.
A24	A23	VSYS	I	Input power supply powering the PMIC internal circuitry. Connect a 2.2µF capacitor from as close this pin to ground as possible.
A25	B21	DCD3_DIF	I/O	DCD3 switching regulator digital interface output signal. This pin must be connected to the DIF pin of the P9147/P9148.
A26	A25	DCD3_DIO	I/O	DCD3 regulator digital interface input/output signal. This pin must be connected to the DIO P9147/P9148.
A27	B23	DCD4_DIF	I/O	DCD4 regulator digital interface output signal. This pin must be connected to the DIF pin of the P9147/P9148.
A28	A26	DCD4_DIO	I/O	DCD4 regulator digital interface input/output signal. This pin must be connected to the DIO pin of the P9147/P9148.
A29	B24	MODEM_OFF_B	O	Active low Modem Hard Reset Signal.
A30	A27	GPIO[8]/SLEEP	I/O	General purpose input/output 8 or sleep mode control signal
A31	A28	GPIO[6]/PWM[0]	I/O	General purpose input/output 6 or PWM[0] output control signal.
A32	A30	GPIO[4]/DCD0_DIO	I/O	General purpose input/output 4 or DCD0 regulator digital interface input/output.
A33	B27	GPIO[2]/DCD1_DIO	I/O	General purpose input/output 2 or DCD1 regulator digital interface input/output.
A34	B29	GPIO[0]/DCD2_DIO	I/O	General purpose input/output 0 or DCD2 regulator digital interface input/output.
A35	A32	DCD2_LX	O	DCD2 switch node - this pin connects to the output inductor.
A36	A33	DCD2_LX	O	DCD2 switch node - this pin connects to the output inductor.

NQG(QFN)	NHG(GQFN)	LABEL	I/O	DESCRIPTION
A37	A34	DCD2_LX	O	DCD2 switch node - this pin connects to the output inductor.
A38	A35	I2C_DATA	I/O	I^2C data
A39	A36	I2C_CLK	I	I^2C clock
A40	A38	EN7	O	Open drain output enable signal.
A41	A41	N/C	-	No connect
A42	A39	EN8	O	Open drain output enable signal.
A43	A40	SUSPWRDNACK	I	Suspend power down acknowledgment.
A44	B37	SLP_S0IX_B	I	Active low input signal. When connected to logic high, all the “SX” power type rails are enabled. When pulled low, the regulators shutdown.
A45	B36	SLP_S3_B	I	Active low input signal. When connected to logic high, all the “S” power type rails are enabled. When pulled low, the regulators shutdown.
A46	A42	SLP_S4_B	I	Active low input signal. When connected to logic high, all the “U” power type rails are enabled. When pulled low, the regulators shutdown.
A47	A43	DCD1_LX	O	DCD1 switch node - this pin connects to the output inductor.
A48	A44	DCD1_LX	O	DCD1 switch node - this pin connects to the output inductor.
A49	A45	DCD1_LX	O	DCD1 switch node - this pin connects to the output inductor.
A50	A46	DCD0_LX	O	DCD0 switch node - this pin connects to the output inductor.
A51	A47	DCD0_LX	O	DCD0 switch node - this pin connects to the output inductor.
A52	A48	DCD0_LX	O	DCD0 switch node - this pin connects to the output inductor.
A53	A49	COREPWROK	O	Active high soft start done signal.
A54	B47	RSMRST_B	O	Resume reset pin is an active low soft start done signal.
A55	A50	SVID_DIO	I/O	SVID data input and open drain output.
A56	A51	SVID_ALERT_B	O	SVID interrupt from PMIC to SOC. Open drain output.
B1	B1	PLTRST_B	I	Platform reset is an active low reset input signal from SoC to PMIC.
B2	A2	PWRBTNIN_B	I	System power button input (active low). The button must be pressed for greater than 30ms to turn on all the A rails.
B3	B3	PWRBTN_B	O	Power button output signal. It is a level shifted copy of PWRBTNIN_B after the 30ms de-bouncing circuit.
B4	B4	DCD5_FB	I	Feedback voltage for DCD5. This pin must be connected to the output voltage of the DCD5.
B5	B5	DCD5_VIN	I	Input voltage for DCD5. Connect a bypass capacitor from this pin to ground.
B6	B6	DCD6_VIN	I	Input voltage for DCD6. Connect a bypass capacitor from this pin to ground.
B7	B7	VGPIO1	I	Supply voltage for GPIO [9] through GPIO [14]. This pin must be connected to 3.3V.
B8	A9	DCD6_FB	I	Feedback voltage for DCD6. This pin must be connected to the output voltage of the DCD6.
B9	B9	DCD4_FB	I	Feedback voltage for DCD4. This pin must be connected to the output voltage of the P9147/P9148.
B10	B10	LDO5_FB	I	Feedback voltage for LDO5. This pin must be connected to the output voltage of the LDO5. This pin is internally connected to LDO5_VO with 180 Ohm.
B11	B11	EN2	O	Open drain output enable signal.
B12	B13	GPIO[12]/ADC[2]	I	General purpose input/output 13 or ADC[2] input.
B13	A15	GPIO[10]/ADC[0]	I	General purpose input/output 11 or ADC[0] input.
B14	A16	GPIO[9]/VDDQSEL	I	General purpose input/output 9 or DCD2 output voltage select
B15	B16	LDO0_VO	O	Linear regulator 0 output terminal.
B16	B17	LDO1_VO	O	Linear regulator 1 output terminal.

NQG(QFN)	NHG(GQFN)	LABEL	I/O	DESCRIPTION
B17	B18	LDO4_VO	O	Linear regulator 4 output terminal.
B18	B19	LDO5_VIN	I	Input supply voltage for source-sink regulator LDO5.
B19	A22	LDO6_VO	O	Linear regulator 6 output terminal.
B20	B20	LDO7_VO	O	1.8V regulator output terminal for DPS control interface and internal biasing.
B21	A24	IRQ	O	Interrupt request output.
B22	B22	SDWN_B	O	Shutdown warning. In the event of system shutdown, PMIC issues a system shutdown warning to the modem.
B23	B25	GPIO[7]/PWM[1]	I	General purpose input/output 7 or PWM[1] output control signal
B24	A29	GPIO[5]/DCD0_DIF	O	General purpose input/output 5 or DCD0 regulator digital interface output.
B25	B26	GPIO[3]/DCD1_DIF	O	General purpose input/output 3 or DCD1 regulator digital interface output.
B26	B28	GPIO[1]/DCD2_DIF	O	General purpose input/output 1 or DCD2 regulator digital interface output.
B27	A31	VGPIO0	I	Input supply voltage for GPIO[0] to GPIO[8]. This pin must be connected to 1.8V voltage rail.
B28	B30	DCD2_VIN	I	Input voltage for DCD2. Connect two 10µF bypass capacitors from this pin to ground.
B29	B31	DCD2_VIN	I	Input voltage for DCD2. Connect two 10µF bypass capacitors from this pin to ground.
B30	B32	DCD2_ FB	I	Feedback voltage for DCD2. This pin must be connected to the output filter of the regulator.
B31	B33	VCCAPWROK	O	Active high open drain soft start done signal.
B32	A37	DRAMPWROK	O	Active high open drain soft start done signal.
B33	B34	PROCHOT_B	O	Active low open drain output signal.
B34	B35	THERMTRIP_B	I	Active low thermal trip input signal. Catastrophic thermal event indicator to PMIC to shut off all power rails.
B35	B38	DCD1_GSEN	I	DCD1 ground sense pin.
B36	B39	DCD1_VIN	I	Input voltage for DCD1. Connect two 10µF bypass capacitors from this pin to ground.
B37	B40	DCD1_VIN	I	Input voltage for DCD1. Connect two 10µF bypass capacitors from this pin to ground.
B38	B41	DCD1_FB	I	Feedback voltage for DCD1. This pin must be connected to the output filter of the DCD1.
B39	B42	VSYS	I	PMIC input supply voltage. Connect a 2.2µF capacitor from as close this pin to ground as possible.
B40	B43	DCD0_ FB	I	Feedback voltage for DCD0. This pin must be connected to the output filter of the DCD0.
B41	B44	DCD0_VIN	I	Input voltage for DCD0. Connect two 10µF bypass capacitors from this pin to ground.
B42	B45	DCD0_VIN	I	Input voltage for DCD0. Connect two 10µF bypass capacitors from this pin to ground.
B43	B46	DCD0_GSEN	I	DCD0 ground sense pin.
B44	B48	SVID_CLK	I	SVID clock input.
EXPOSED PAD	EXPOSED PAD	PGND	I	Ground. Exposed pad is the connection for current return path, and is also used for thermal dissipation. Connect to PCB ground with sufficient vias to support the returned current and thermal requirement.

FUNCTIONAL DIAGRAM

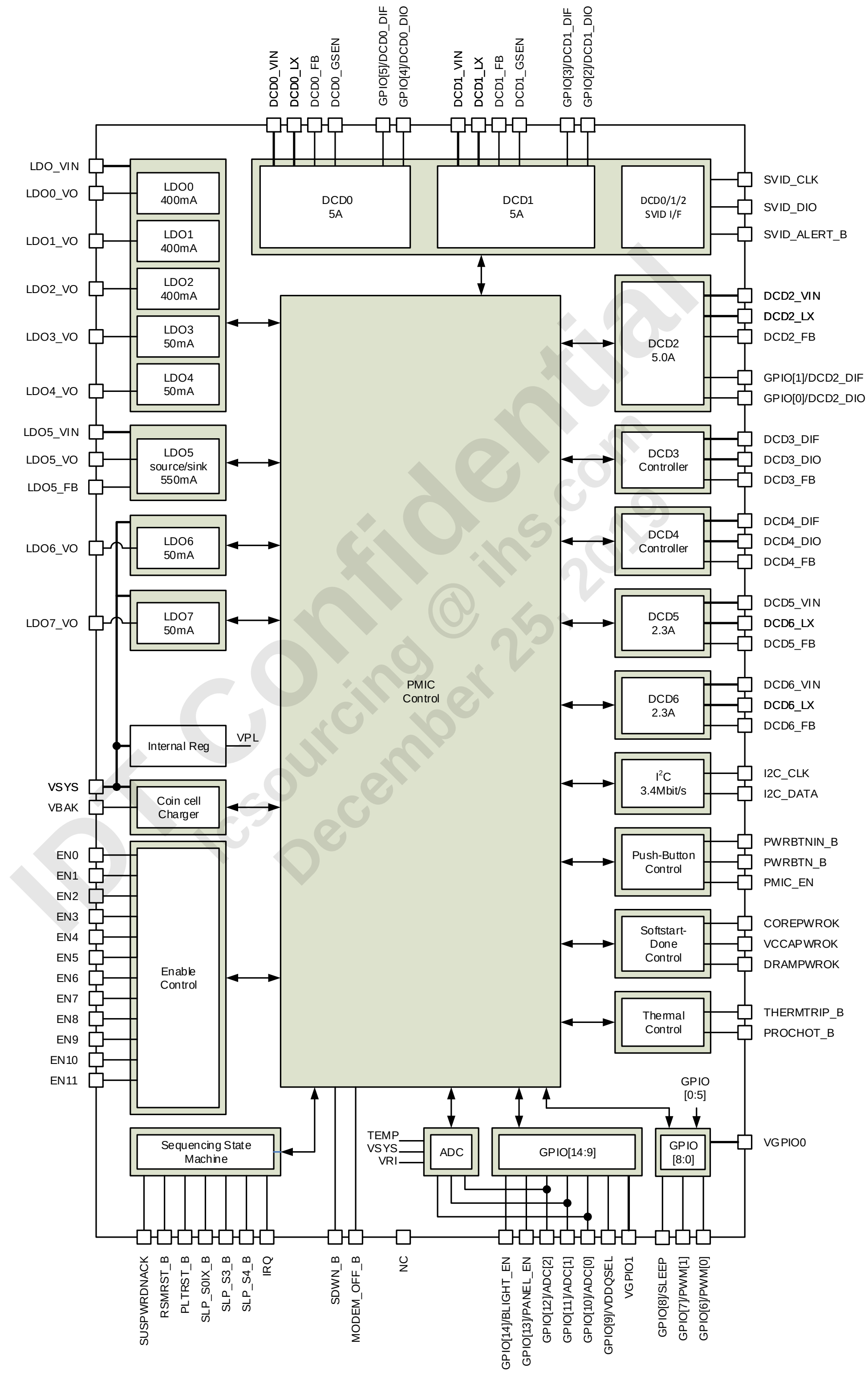


Figure 3: Functional Diagram

DESCRIPTIONS, SPECIFICATION TABLES & REGISTERS

General Specification

Table 6: Electrical Characteristics – PMIC VSYS, UVLO, thermal shutdown threshold

V_{SYS}= 5.0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SYS}	Input voltage range		3.15		5.25	V
$I_{Q(VSYS)}$	VSYS quiescent current	Device in G3 (OFF state)		7		µA
		Device in S4 state, all regulators powered-off		0.75	1.1	mA
$V_{SYS(UVLO)}$	UVLO threshold	VSYS rising ($VSYSREF_R$)		2.9		V
		VSYS falling ($VSYSREF_F$)		2.5		V
T_{SDN}	Thermal shutdown	Temperature increasing	125	132		°C

Linear Regulators LDO0, LDO1, LDO2

Table 7: Electrical Characteristics – LDO0, LDO1, LDO2

V_{SYS} = 5V, V_{IN_LDO} = 1.8V, V_{OUT} = 1.5V (default), C_{IN} = 10µF, C_O = 2.2µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN_LDO}	Input voltage range		1.0	1.8	2.0	V
V_O	Programmable output voltage		1.0	1.5	1.65	V
I_{SHDN}	Shutdown current			0.5		µA
I_Q	Quiescent current	No Load		22		µA
	Regulation voltage accuracy		-2.0		+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation			1.0		ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation			5.0		µV/mA
I_O	Maximum output current		300			mA
I_{LIM}	Current limit		400			mA
V_{DROP}	Dropout voltage	I_O = 300mA			150	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Power Supply Ripple Rejection	$V_{IN\_LDO} – V_O$ = 500mV, I_O = 30mA				dB
		<200Hz		>100		
		1kHz		100		
		10kHz		85		
		100kHz		55		
e_n	Output noise voltage	V_O = 1.5V, I_O = 100µA, BW = 10Hz to 100kHz		28		µVRMS
T_{SSR}	LDO soft-start ramp rate			30		mV/µs

Table 8: I²C Control Register – LDO0, LDO1, LDO2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO0_CTL	R/W	Reserved						LDO0_SEL	LDO0_EN	0x00	0x65
LDO1_CTL	R/W	Reserved						LDO1_SEL	LDO1_EN	0x00	0x61
LDO2_CTL	R/W	Reserved						LDO2_SEL	LDO2_EN	0x00	0x66

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	LDOx_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	LDOx_EN	Enable bit 0 = OFF 1 = ON	0

Table 9: ON/OFF Select Bit Truth Table – LDO0, LDO1, LDO2

D[1]	D[0]	Sequencer control	LDO
0	X	0	OFF
0	X	1	ON
1	0	X	OFF
1	1	X	ON

Table 10: I²C Output Voltage Setting – LDO0, LDO1, LDO2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO0_VOUT	R/W	Reserved			Output Voltage Setting (see Table 12)					OTP	0x12
LDO1_VOUT	R/W	Reserved			Output Voltage Setting (see Table 12)					OTP	0x13
LDO2_VOUT	R/W	Reserved			Output Voltage Setting (see Table 12)					OTP	0x14

Table 11: I²C Sequencing Control Register – LDO0, LDO1, LDO2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO0_GRP	R/W	Reserved		LDO0_TYPE		LDO0_GROUP				OTP	0xED
LDO1_GRP	R/W	Reserved		LDO1_TYPE		LDO1_GROUP				OTP	0xEE
LDO2_GRP	R/W	Reserved		LDO2_TYPE		LDO2_GROUP				OTP	0xEF

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	LDOX_TYPE	Rail Type Select Bit 00 = “A” rail type. 01 = “U” rail type. 10 = “S” rail type. 11 = “SX” rail type.	OTP
D[3:0]	LDOX_GROUP	Group Delay Bits 0000b = Group 0 0001b = Group 1 0010b = Group 2 0011b = Group 3 0100b = Group 4 0101b = Group 5 0110b = Group 6 0111b = Group 7 1000b = Group 8 1001b = Group 9 1010b = Group 10 1011b = Group 11 1100b = Group 12 1101b = Group 13 1110b = Group 14 1111b = Disabled	OTP

Table 12: LDO0, LDO1, LDO2 Output Voltage Setting

V_{OUT}	Decimal	Hex	Binary
1.000	0	00	00000
1.025	1	01	00001
1.050	2	02	00010
1.075	3	03	00011
1.100	4	04	00100
1.125	5	05	00101
1.150	6	06	00110
1.175	7	07	00111
1.200	8	08	01000
1.225	9	09	01001
1.250	10	0A	01010
1.275	11	0B	01011
1.300	12	0C	01100
1.325	13	0D	01101
1.350	14	0E	01110
1.375	15	0F	01111
1.400	16	10	10000
1.425	17	11	10001
1.450	18	12	10010
1.475	19	13	10011
1.500	20	14	10100
1.525	21	15	10101
1.550	22	16	10110
1.575	23	17	10111
1.600	24	18	11000
1.625	25	19	11001
1.650	26	1A	11010
Pass switch	≥27	≥1B	

Linear Regulators LDO3, LDO4

Table 13: Electrical Characteristics – LDO3, LDO4

V_{IN_LDO} = 1.8V, V_{OUT} = 1.2V (default), C_{IN} = 10µF, C_O = 1.0µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN_LDO}	Input voltage range		1.0	1.8	2.0	V
V_O	Output voltage range		1.0	1.2	1.65	V
I_{SHDN}	Shutdown current			0.5		µA
I_Q	Quiescent current	No Load		20		µA
	Regulation voltage accuracy		-2.0		+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation			1.0		ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation			19		µV/mA
I_O	Maximum output current		50			mA
I_{LIM}	Current limit		60			mA
V_{DROP}	Dropout voltage	I_O = 50mA			100	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Power Supply Ripple Rejection	V_{IN_LDO} – V_O = 500mV, I_O = 10mA				dB
		< 200Hz		>100		
		1kHz		100		
		10kHz		85		
		100kHz		55		
e_n	Output noise voltage	V_O =1.2V, I_O = 100µA, BW = 10Hz to 100kHz		28		µVRMS
T_{SSR}	LDO soft-start ramp rate			30		mV/µs

Table 14: I²C Control Register – LDO3, LDO4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO3_CTL	R/W	Reserved						LDO3_SEL	LDO3_EN	0x00	0x5E
LDO4_CTL	R/W	Reserved						LDO4_SEL	LDO4_EN	0x00	0x60

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	LDOx_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	LDOx_EN	Enable bit 0 = OFF 1 = ON	0

Table 15: Select Bit Truth Table – LDO3, LDO4

D[1]	D[0]	Sequencer control	LDO
0	X	0	ON
0	X	1	OFF
1	0	X	OFF
1	1	X	ON

Table 16: I²C Output Voltage Setting – LDO3, LDO4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO3_VOUT	R/W	Reserved			Output Voltage Setting (see Table 18)					OTP	0x16
LDO4_VOUT	R/W	Reserved			Output Voltage Setting (see Table 18)					OTP	0x17

Table 17: I²C Sequencing Control Register – LDO3, LDO4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO3_GRP	R/W	Reserved		LDO3_TYPE		LDO3_GROUP				OTP	0xF0
LDO4_GRP	R/W	Reserved		LDO4_TYPE		LDO4_GROUP				OTP	0xF1

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	LDOx_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.	OTP
D[3:0]	LDOx_GROUP	Group Delay Bits 0000b = Group 0 / 1000b = Group 8 0001b = Group 1 / 1001b = Group 9 0010b = Group 2 / 1010b = Group 10 0011b = Group 3 / 1011b = Group 11 0100b = Group 4 / 1100b = Group 12 0101b = Group 5 / 1101b = Group 13 0110b = Group 6 / 1110b = Group 14 0111b = Group 7 / 1111b = Disable	OTP

Table 18: LDO3, LDO4 Output Voltage Setting

V_{OUT}	Decimal	Hex	Binary
1.000	0	00	000000
1.025	1	01	000001
1.050	2	02	000010
1.075	3	03	000011
1.100	4	04	000100
1.125	5	05	000101
1.150	6	06	000110
1.175	7	07	000111

V_{OUT}	Decimal	Hex	Binary
1.200	8	08	001000
1.225	9	09	001001
1.250	10	0A	001010
1.275	11	0B	001011
1.300	12	0C	001100
1.325	13	0D	001101
1.350	14	0E	001110
1.375	15	0F	001111
1.400	16	10	010000
1.425	17	11	010001
1.450	18	12	010010
1.475	19	13	010011
1.500	20	14	010100
1.525	21	15	010101
1.550	22	16	010110
1.575	23	17	010111
1.600	24	18	011000
1.625	25	19	011001
1.650	26	1A	011010

Linear Regulator LDO5

LDO5 is a source-sink linear regulator capable of delivering load currents as high as ±550mA. The output voltage is designed to regulate at $V_{IN\_LDO5}/2$. The regulator is controlled either through the sequencing state machine or by I²C.

Table 19: Electrical Characteristics – LDO5

V_{IN_LDO5} = 1.24V, V_{OUT} = 0.620V (default), C_{IN} = 22µF, C_O = 22µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN_LDO5}	Input voltage range		1.20	1.24	1.50	V
V_{O_LDO5}	Output voltage			$V_{IN\_LDO5}/2$		V
I_{SHDN}	Shutdown current			1		µA
I_Q	Quiescent current	No Load		60	95	µA
	Regulation voltage accuracy	$-550mA \le I_{LOAD} \le +550mA$	-5		+5	%
$I_{(source)}$	Maximum source output current		550			mA
$I_{(sink)}$	Maximum sink output current		550			mA
R_{DIS}	Output discharge resistance			80		Ω

Table 20: I²C Control Register – LDO5

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO5_CTL	R/W	Reserved						LDO5_SEL	LDO5_EN	0x00	0x58

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	LDO5_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	LDO5_EN	Enable bit 0 = OFF 1 = ON	0

Table 21: Select Bit Truth Table – LDO5

D[1]	D[0]	Sequencer control	LDO5
0	X	0	OFF
0	X	1	ON
1	0	X	OFF
1	1	X	ON

Table 22: I²C Sequencing Control – LDO5

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO5_GRP	R/W	Reserved		LDO5_TYPE		LDO5_GROUP				OTP	0xF2

BIT	Name	Function		Default
D[7:6]	Reserved	Reserved		0
D[5:4]	LDO5_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.		OTP
D[3:0]	LDO5_GROUP	Group Delay Bits 0000b = Group 0 0001b = Group 1 0010b = Group 2 0011b = Group 3 0100b = Group 4 0101b = Group 5 0110b = Group 6 0111b = Group 7	1000b = Group 8 1001b = Group 9 1010b = Group 10 1011b = Group 11 1100b = Group 12 1101b = Group 13 1110b = Group 14 1111b = Disable	OTP

Linear Regulator LDO6

Table 23: Electrical Characteristics – LDO6

V_{SYS}= 5.0V, V_{OUT} = 3.3V, C_O = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SYS}	Input voltage range		3.15	5.0	5.25	V
V_O	Output voltage range		1.0	3.3	3.55	V
I_{SHDN}	Shutdown current			0.5		µA
I_Q	Quiescent current	No Load		20		µA
	Regulation voltage accuracy		-2		+2	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation			1		ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation			40		µV/mA
I_O	Maximum output current		100			mA
I_{LIM}	Current limit		120			mA
V_{DROP}	Dropout voltage	I_O = 50mA			125	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Power Supply Ripple Rejection[1]	V_{SYS} – V_O=1V, I_O = 30mA				dB
		< 200Hz		> 120		
		1kHz		120		
		10kHz		95		
		100kHz		57		
e_n	Output noise voltage[1]	V_O= 3.3V, I_O = 100µA, BW = 10Hz to 100kHz		28		µVRMS
T_{SSR}	LDO soft-start ramp rate			32		mV/µs

Table 24: I²C Control Register – LDO6

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO6_CTL	R/W	Reserved						LDO6_SEL	LDO6_EN	0x00	0x6A

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	LDO6_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	LDO6_EN	Control bit 0 = OFF 1 = ON	0

Table 25: Select Bit Truth Table – LDO6

D[1]	D[0]	Sequencer control	LDO6
0	X	0	ON
0	X	1	OFF
1	0	X	OFF
1	1	X	ON

Table 26: I²C Output Voltage Setting – LDO6

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO6_VOUT	R/W	Reserved		Output Voltage Setting (see Table 28)						0x00	0x18

Table 27: I²C Sequencing Control – LDO6

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDO6_GRP	R/W	Reserved		LDO6_TYPE		LDO6_GROUP				OTP	0xF3

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	LDO6_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.	OTP
D[3:0]	LDO6_GROUP	Group Delay Bits 0000b = Group 0 1000b = Group 8 0001b = Group 1 1001b = Group 9 0010b = Group 2 1010b = Group 10 0011b = Group 3 1011b = Group 11 0100b = Group 4 1100b = Group 12 0101b = Group 5 1101b = Group 13 0110b = Group 6 1110b = Group 14 0111b = Group 7 1111b = Disable	OTP

Table 28: LDO6 Output Voltage Setting

V_{OUT}	Decimal	Hex	Binary
1.00	0	00	000000
1.05	1	01	000001
1.10	2	02	000010
1.15	3	03	000011
1.20	4	04	000100
1.25	5	05	000101
1.30	6	06	000110
1.35	7	07	000111
1.40	8	08	001000

V_{OUT}	Decimal	Hex	Binary
1.45	9	09	001001
1.50	10	0A	001010
1.55	11	0B	001011
1.60	12	0C	001100
1.65	13	0D	001101
1.70	14	0E	001110
1.75	15	0F	001111
1.80	16	10	010000
1.85	17	11	010001
1.90	18	12	010010
1.95	19	13	010011
2.00	20	14	010100
2.05	21	15	010101
2.10	22	16	010110
2.15	23	17	010111
2.20	24	18	011000
2.25	25	19	011001
2.30	26	1A	011010
2.35	27	1B	011011
2.40	28	1C	011100
2.45	29	1D	011101
2.50	30	1E	011110
2.55	31	1F	011111
2.60	32	20	100000
2.65	33	21	100001
2.70	34	22	100010
2.75	35	23	100011
2.80	36	24	100100
2.85	37	25	100101
2.90	38	26	100110
2.95	39	27	100111
3.00	40	28	101000
3.05	41	29	101001
3.10	42	2A	101010
3.15	43	2B	101011
3.20	44	2C	101100
3.25	45	2D	101101
3.30	46	2E	101110
3.35	47	2F	101111
3.40	48	30	110000
3.45	49	31	110001
3.50	50	32	110010
3.55	51	33	110011
3.60	52	34	110100
3.65	53	35	110101
3.70	54	36	110110
3.75	55	37	110111

Linear Regulator LDO7

LDO7 is an always-on LDO, mainly for supplying the 1.8V rated GPIO[8:0] through the VGPIO0 input. LDO7 also supplies the DIF/DIO interfaces for DCD3 and DCD4, MODEM_OFF_B, SDWN_B, PWRBTN_B, and IRQ output buffers. The LDO can also be used for general purposes, as long as the total output current is limited below 100mA.

LDO is enabled once the PMIC enters S4 state und remains enabled until the PMIC powers down to G3 state.

Table 29: Electrical Characteristics – LDO7
V_{SYS}= 5.0V, V_{OUT} = 1.8V, C_O = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_O	Output voltage range			1.8		V
I_{SHDN}	Shutdown current			0.5		µA
I_Q	Quiescent current	No Load		20		µA
	Regulation voltage accuracy		-2		+2	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation			1		ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation			40		µV/mA
I_O	Maximum output current		100			mA
I_{LIM}	Current limit		120			mA
V_{DROP}	Dropout voltage	I_O = 50mA			125	mV
R_{DIS}	Output discharge resistance			10		kΩ
PSRR	Power Supply Ripple Rejection[1]	V_{SYS} – V_O=1V, I_O = 30mA				dB
		< 200Hz		> 120		
		1kHz		120		
		10kHz		95		
		100kHz		57		
e_n	Output noise voltage[1]	V_O= 1.8V, I_O = 100µA, BW = 10Hz to 100kHz		28		µVRMS
T_{SSR}	LDO soft-start ramp rate			32		mV/µs

LDO Current Limit Flags

Each linear regulator has a non-latching over-current flag. Once the regulator reaches current limit, the flag asserts for the duration of the over current condition and will de-assert when the current falls below the current limit threshold.

Table 30: LDO Current Limit Flags

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
LDOF1	R	LDO7_SC	LDO6_SC	LDO5_SC	LDO4_SC	LDO3_SC	LDO2_SC	LDO1_SC	LDO0_SC	0x00	0x9D

Switching Regulators for SoC Core, Graphics and Memory Rails

DCD0, DCD1, and DCD2 are high efficiency, synchronous step-down switching regulators capable of delivering up to 5A of peak current.

The output voltage (or boot voltage) can be individually set by OTP. It can be changed from the default setting either through I²C or SVID. The regulators support "Dynamic Voltage Scaling" (DVS) allowing on-the-fly, slew-rate controlled changes to the output voltage.

The regulators operate with a fixed 2MHz oscillator frequency allowing the use of small external components, minimizing cost and real estate. To maximize efficiency under varying load conditions the regulators offer selectable modes of operation through I²C. Available modes are forced PWM (FPWM) and auto-mode (PWM/PFM). Auto-mode is selected by default and allows the regulator to switch automatically between PWM and PFM mode, depending on the load condition. During heavy load the regulator operates in PWM mode at a fixed frequency. As the load decreases and the inductor valley current reaches zero, it automatically transitions into PFM mode maintaining high efficiency under light load conditions. For noise sensitive applications, the regulator can be forced into PWM mode by disabling the power-saving PFM mode.

The on/off control of the regulators can be accessed either through I²C or by toggling the appropriate SLP_Sx_B pins. Other features of the regulators include over-voltage protection, soft-start, and soft start done flags.

The regulators include an active discharge circuitry to discharge the output capacitor and hold the output voltage at ground after the regulator turned off.

SVID is the default interface for changing the output voltage setting. For applications not requiring SVID, the SVID interface can be disabled by OTP or thru I²C.

The regulators are capable of supporting load currents greater than 5A by connecting additional phases (P9147/P9148) to the DIF interface. Each individual P9147/P9148 can deliver peak currents of up to 5A with up to four phases in parallel. The communication link between the converter and P9147/P9148 is established by connecting DCDx_DIF and DCDx_DIO pins to the corresponding pins of the P9147/P9148. The DIF and DIO interface is running IDT's proprietary communication protocol and controls the attached devices. If additional phases are not required, the DIO and DIF pins can be used as regular GPIO pins or can be left floating. (Consult P9147/P9148 datasheet for electrical characteristics and product description.)

The power sequencing of each regulator can be changed by OTP trim. Contact factory to change the timing and the power rail type.

Switching Regulator DCD0, DCD1

Table 31: Electrical Characteristics – DCD0, DCD1

V_{IN_DCD} = 5.0V, V_O = 1.0V (default), L= 0.47µH, C_{IN_DCD} =10µF, C_O = 282µF; no DPU (P9147/P9148). T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN_DCD}	Input voltage range		2.7	5.0	5.25	V
V_O	Output voltage range	SVID enabled	0.250	1.000	1.295	V
		SVID disabled	1.100		1.890	
	Regulation voltage accuracy (Set point accuracy)	For factory programmed V_O	-2.0		+2.0	%
$R_{LL(DC)}$	DC Load Line			6		mΩ
$R_{LL(AC)}$	AC Load Line			10		mΩ
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN_DCD} = 2.75V – 5.25V		0.03		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5A – 4A, PWM mode, Load line disabled		0.3		mV/A
V_{OFFSET}	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)} + V_{OFFSET}$	PFM mode		15		mV
I_O	Continuous operating DC current	T_J < 115°C, GBD	4.0			A
I_{PULSE}	Pulsed Load Current	t_{Load} < 1ms.		5.0		A
$I_{SHD(VIN\_DCD)}$	Shutdown current	Regulator disabled		1.0		µA
I_{VIN_DCD}	Power Stage Supply Current	Forced PWM mode, no load		300		µA
		Forced PFM mode, no switching		200		µA
$R_{(DSON)}$	High side switch on resistance	$V_{SYS} = V_{IN\_DCD}$ = 5V, I_{OUT} = 500mA		50	80	mΩ
	Low side switch on resistance	$V_{SYS} = V_{IN\_DCD}$ = 5V, I_{OUT} = 500mA		28	80	mΩ
R_{DIS}	Output discharge resistance			280	450	Ω
F_{SW}	Switching frequency	PWM mode, GBD	1.8	2.0	2.2	MHz
$T_{ON(MIN)}$	Minimum On-Time			70		ns
T_{DCDSSR}	DCD soft-start ramp rate	15% – 90% of V_O		3.5		mV/µs
ΔG_{SEN}	GSEN pin diff. voltage range			250		mV
Z_{SEN}	GSEN pin input impedance			1		MΩ
I_{FB}	FB input bias current				10	µA
V_{OVP}	Overvoltage protection threshold	SVID enabled SVID disabled		1.8 2.4		V
	Overvoltage protection threshold tolerance	GBD	-5.0		+5.0	%

Table 32: VBOOT Register – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_VBOOT	R/W	VBOOT[7:1]							VBOOT[0]	OTP	0xBC
DCD1_VBOOT	R/W	VBOOT[7:1]							VBOOT[0]	OTP	0xCC

NOTE: If VBOOT[7:1] = 0x00, then VBOOT[0] = 0, otherwise VBOOT[0] = 1.

BIT	Name	Function	Default
D[7:0]	DCDx_VBOOT	VBOOT (refer to Table 46: Output Voltage Settings – DCD0/DCD1/DCD2)	OTP

Table 33: VID Register – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_VID	R/W	VID[7:0]								0x00	0xBE
DCD1_VID	R/W	VID[7:0]								0x00	0xCE

BIT	Name	Function	Default
D[7:0]	VID CODE	VID (refer to Table 46: Output Voltage Settings – DCD0/DCD1/DCD2)	0x97

Table 34: I²C Control Register – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_CTL	R/W	Reserved			SVID	Reserved	Reserved	DCD0_SEL	DCD0_EN	0x10	0x53
DCD1_CTL	R/W	Reserved			SVID	Reserved	Reserved	DCD1_SEL	DCD1_EN	0x10	0x54

BIT	Name	Function	Default
D[7:5]	Reserved	Reserved	0
D[4]	SVID	SVID ON/OFF select bit 0 = SVID disabled. 1 = SVID enabled.	OTP
D[3:2]	Reserved	Reserved	0
D[1]	DCDx_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	DCDx_EN	Enable bit 0 = OFF 1 = ON	0

Table 35: On/Off Select Bit Table – DCD0, DCD1

D[1]	D[0]	Sequencer control	DCD0
0	X	0	OFF
0	X	1	ON
1	0	X	OFF
1	1	X	ON

Table 36: I²C Output Voltage Register – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_SLEW	R/W	Reserved		Fast_Rate		Reserved			Slow_Rate	0x00	0xA8
DCD1_SLEW	R/W	Reserved		Fast_Rate		Reserved			Slow_Rate	0x00	0xA9

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	Fast_Rate	SetVID fast output voltage slew rate 00 = 10mV/µs 10 = 40mV/µs 01 = 20mV/µs 11 = Reserved	00
D[3:1]	Reserved	Reserved	0
D[0]	Slow_Rate	SetVID slow output voltage slew rate 0 = 2.5mV/µs 1 = 5mV/µs	0

Table 37: I²C Sequencing Control – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD0_GRP	R/W	Reserved		DCD0_TYPE		DCD0_GROUP				OTP	0xE6
DCD1_GRP	R/W	Reserved		DCD1_TYPE		DCD1_GROUP				OTP	0xE7

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	DCDx_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.	OTP
D[3:0]	DCDx_GROUP	Group Delay Bit 0000b = Group 0 1000b = Group 8 0001b = Group 1 1001b = Group 9 0010b = Group 2 1010b = Group 10 0011b = Group 3 1011b = Group 11 0100b = Group 4 1100b = Group 12 0101b = Group 5 1101b = Group 13 0110b = Group 6 1110b = Group 14 0111b = Group 7 1111b = Disable	OTP

Table 38: I²C Core-Type Exit Control – DCD0, DCD1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
CORE_TYPE_EXIT	R/W	Reserved						DCD1_TYPE_EXIT	DCD0_TYPE_EXIT	0x00	0x10

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	DCD1_TYPE_EXIT	0 = Exit sequence disabled. 1 = Exit sequence enabled.	0
D[0]	DCD0_TYPE_EXIT	0 = Exit sequence disabled. 1 = Exit sequence enabled.	0

When Exit Sequencing is disabled, DCD[1:0] follows I²C Sequencing Control for DCD0, DCD1 in registers 0xE6, 0xE7 respectively.

When Exit Sequencing is enabled

- The respective DCD1 and/or DCD0 will be powered on as “A” rail type (Type 00b) with the group delay set by DCDx_GRP[3:0].
- DCD[1:0] maintain an “A” Type (Type 00b) until RSMRST_B and PLTRST_B are both simultaneously asserted.
- Once assertion of both signals is detected the DCD_TYPE is changed to DCDx_TYPE[5:4] – which are programmable via OTP. DCDx_TYPE[5:4] are then used for enabling and disabling of DCD[1:0] until the system is reset.

Switching Regulator DCD2

Table 39: Electrical Characteristics – DCD2

V_{IN_DCD}= 5.0V, V_O =1.2V (default), L=0.47µH, C_{IN_DCD} =10µF, C_O =282µF; no DPU (P9147/P9148). T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN_DCD}	Input voltage range		2.7	5.0	5.25	V
V_O	Output voltage range	SVID enabled	0.250	1.000	1.295	V
		SVID disabled	1.100		1.890	
	Regulation voltage accuracy (Set point accuracy)	For factory programmed V_O	-2.0		+2.0	%
$R_{LL(DC)}$	DC Load Line			6		mΩ
$R_{LL(AC)}$	AC Load Line			10		mΩ
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN_DCD} = 2.75V – 5.25V		0.03		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5A – 4A, PWM mode, Load line disabled		0.3		mV/A
V_{OFFSET}	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)}+V_{OFFSET}$	PFM mode		15		mV
I_O	Continuous operating DC current	T_J < 115°C, GBD	4.0			A
I_{PULSE}	Pulsed Load Current	t_{Load} < 1ms.		5.0		A
$I_{SHD(VIN\_DCD)}$	Shutdown current	Regulator disabled		1.0		µA
I_{VIN_DCD}	Power Stage Supply Current	Forced PWM mode, no load		300		µA
		Forced PFM mode, no switching		200		µA
$R_{(DSON)}$	High side switch on resistance	$V_{SYS} = V_{IN\_DCD}$ = 5V, I_{OUT} = 500mA		50	80	mΩ
	Low side switch on resistance	$V_{SYS} = V_{IN\_DCD}$ = 5V, I_{OUT} = 500mA		28	80	mΩ
R_{DIS}	Output discharge resistance			280	450	Ω
F_{SW}	Switching frequency	PWM mode, GBD	1.8	2.0	2.2	MHz
$T_{ON(MIN)}$	Minimum On-Time			70		ns
T_{DCDSSR}	DCD soft-start ramp rate	15% – 90% of V_O		3.5		mV/µs
I_{FB}	FB input bias current				10	µA

Table 40: VBOOT Register – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_VBOOT	R/W	VBOOT[7:1]							VBOOT[0]	OTP	0xDC

BIT	Name	Function	Default
D[7:0]	DCD2_VBOOT	VBOOT (refer to Table 46: Output Voltage Settings – DCD0/DCD1/DCD2)	OTP

NOTE: If VBOOT[7:1] = 0x00, then VBOOT[0] = 0, otherwise VBOOT[0] = 1.

Table 41: VID Register – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_VID	R/W	VID[7:0]								0x00	0xDE

BIT	Name	Function	Default
D[7:0]	DCD2_VID	VID (refer to Table 46: Output Voltage Settings – DCD0/DCD1/DCD2)	0xDD

Table 42: I²C Control Register – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_CTL	R/W	Reserved			SVID	Reserved		DCD2_SEL	DCD2_EN	0x00	0x5F

BIT	Name	Function	Default
D[7:5]	Reserved	Reserved	0
D[4]	SVID	SVID ON/OFF select bit 0 = SVID disabled. 1 = SVID enabled.	0
D[3:2]	Reserved	Reserved	0
D[1]	DCD2_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	DCD2_EN	Enable bit 0 = OFF 1 = ON	0

Table 43: On/Off Select Bit Table – DCD2

D[1]	D[0]	Sequencer control	DCD2
0	X	0	OFF
0	X	1	ON
1	0	X	OFF
1	1	X	ON

Table 44: I²C Output Voltage Register – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_SLEW	R/W	Reserved		Fast_Rate		Reserved			Slow_Rate	0x00	0xAA

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	Fast_Rate	Fast Output Voltage Slew Rate 00 = 10mV/µs 10 = 40mV/µs 01 = 20mV/µs 11 = Reserved	01
D[3:1]	Reserved	Reserved	0
D[0]	Slow_Rate	Slow Output Voltage Slew Rate 0 = 2.5mV/µs 1 = 5mV/µs	0

Table 45: I²C Sequencing Control – DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD2_GRP	R/W	Reserved		DCD2_TYPE		DCD2_GROUP[1]				OTP	0xE8

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	DCD2_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.	OTP
D[3:0]	DCD2_GROUP	Group Delay Bit 0000b = Group 0 1000b = Group 8 0001b = Group 1 1001b = Group 9 0010b = Group 2 1010b = Group 10 0011b = Group 3 1011b = Group 11 0100b = Group 4 1100b = Group 12 0101b = Group 5 1101b = Group 13 0110b = Group 6 1110b = Group 14 0111b = Group 7 1111b = Disable	OTP

Table 46: Output Voltage Settings – DCD0/DCD1/DCD2

SVID enabled

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex	Voltage
0	0	0	0	0	0	0	0	0x00	OFF / 0.250 [2]
0	0	0	0	0	0	0	1	0x01	0.250
0	0	0	0	0	0	1	0	0x02	0.255
0	0	0	0	0	0	1	1	0x03	0.260
					. . .				
1	1	0	1	0	0	0	0	0xD0	1.285
1	1	0	1	0	0	0	1	0xD1	1.290
1	1	0	1	0	0	1	0	0xD2	1.295[1]
1	1	0	1	0	0	1	1	0xD3	1.300

SVID disabled

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex	Voltage
0	0	1	1	0	0	1	1	0x33	1.100
0	0	1	1	0	1	0	0	0x34	1.105
0	0	1	1	0	1	0	1	0x35	1.110
					. . .				
1	1	0	1	0	0	0	0	0xD0	1.885
1	1	0	1	0	0	0	1	0xD1	1.890
1	1	0	1	0	0	1	0	0xD2	1.895
1	1	0	1	0	0	1	1	0xD3	1.900

[1] Max default = 1.295V. To allow VID code 0xD3 (1.30V) the VOUTMAX register has to be adjusted accordingly (Table 99: Serial Voltage Identification (SVID) Register Set)

[2] OFF when register 0x7B.Bit[1] = 1, and 0.250V when register 0x7B.Bit[1] = 0. Register 0x7B (VSLEEP) is OTP-able.

Controllers DCD3, DCD4

DCD3 and DCD4 are step-down controllers and require at least one DPU (P9147 or P9148) connected to the DIF bus. The regulators have no power stage in the PMIC. The PMIC provides only the control and analog circuitry for the regulators and relies on the external DPU to provide power to the load.

The output voltage is factory set to a default value but it can be changed from the default setting through I^2C. (See Table 52 for available voltages).

The regulators operate with a fixed 2MHz oscillator frequency allowing the use of small external components, minimizing cost and real estate. The mode of operation supported by DCD3/4 is forced PWM (FPWM) with a maximum output voltage of 3.6V. If power saving is needed, it is recommended to configure the rails for sleep mode (SLP_) or disabling. The on/off control of DCD3 and DCD4 can be accessed either through I^2C or it will be managed be the programmed sequence.

The controllers must be used in conjunction with P9147/P9148s. The communication link between P9180A and P9147/P9148 is established by connecting DCD3_DIF/DCD4_DIF and DCD3_DIO/DCD4_DIO pins to the corresponding pins of the P9147/P9148. For each additional phase, the P9147/P9148 can deliver peak currents of 5A supporting up to four phases connected in parallel. If the regulators are not used, the DIO and DIF pins can be left floating. (Consult P9147/P9148 datasheet for electrical characteristics and product description.)

Table 47: Electrical Characteristics – DCD3, DCD4

V_{SYS}= 5.0V, V_O = 3.3V_{DCD3}, 1.8V_{DCD4} (default), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_O	Output voltage range		0.525		3.6	V
	Regulation voltage accuracy (Set point accuracy)	For factory programmed V_O, test mode	-2.0		+2.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN_P9148} = 4.5V – 8.4V		0.03		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5A – 4A, PWM mode		0.3		mV/A
V_{OFFSET}	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)}+V_{OFFSET}$	PFM mode		15		mV
I_{SHD}	Shutdown current			1.0		µA
F_{SW}	Switching frequency	PWM mode, GBD	1.8	2.0	2.2	MHz
T_{DCDSSR}	DCD soft-start ramp rate	15% – 90% of V_O		3.5		mV/µs
I_{FB}	Feedback input bias current				10	µA

NOTES:

1. DCD3, DCD4 must be used in conjunction with P9147/P9148.

Table 48: I^2C Control Register – DCD3, DCD4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD3_CTL	R/W	Reserved						DCD3_SEL	DCD3_EN	0x00	0x67
DCD4_CTL	R/W	Reserved						DCD4_SEL	DCD4_EN	0x00	0x5A

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	DCDx_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0

BIT	Name	Function	Default
D[0]	DCDx_EN	Enable bit 0 = OFF 1 = ON	0

Table 49: On/Off Select Bit Table – DCD[3/4]

D[1]	D[0]	Sequencer control	DCD[3/4]
0	X	0	ON
0	X	1	OFF
1	0	X	OFF
1	1	X	ON

Table 50: I²C Output Voltage Setting – DCD3, DCD4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD3_VOUT	R/W	DCD3_RNG		DCD3_VOUT						OTP	0xA4
DCD4_VOUT	R/W	DCD4_RNG		DCD4_VOUT						OTP	0xA5

BIT	Name	Function	Default
D[5:0]	DCDx_VOUT	DCD3, DCD4 Output Voltage Setting (see Table 52: Output Voltage Setting - DCD3, DCD4)	OTP
D[7:6]	DCDx_RNG[1]	Output Voltage Range select bit 00 = 0.5250 – 1.3125 increment of 12.5mV. 01 = 1.2875 – 2.0750 increment of 12.5mV. 10 = 2.0500 – 2.8375 increment of 12.5mV. 11 = 2.8125 – 3.6000 increment of 12.5mV.	OTP

Table 51: I²C Sequencing Control – DCD3, DCD4

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD3_GRP	R/W	Reserved		DCD3_TYPE		DCD3_GROUP[1]				OTP	0xE9
DCD4_GRP	R/W	Reserved		DCD4_TYPE		DCD4_GROUP[1]				OTP	0xEA

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	DCDx_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.	OTP
D[3:0]	DCDx_GROUP	Group Delay Bit 0000b = Group 0 1000b = Group 8 0001b = Group 1 1001b = Group 9 0010b = Group 2 1010b = Group 10 0011b = Group 3 1011b = Group 11 0100b = Group 4 1100b = Group 12 0101b = Group 5 1101b = Group 13 0110b = Group 6 1110b = Group 14 0111b = Group 7 1111b = Disable	OTP

Table 52: Output Voltage Setting - DCD3, DCD4

Range [00]	Range [01]	Range [10]	Range [11]	Decimal	Hex	Binary
0.5250	1.2875	2.0500	2.8125	0	00	000000
0.5375	1.3000	2.0625	2.8250	1	01	000001
0.5500	1.3125	2.0750	2.8375	2	02	000010
.						
.						
.						
1.2875	2.0500	2.8125	3.5750	61	3D	111101
1.3000	2.0625	2.8250	3.5875	62	3E	111110
1.3125	2.0750	2.8375	3.6000	63	3F	111111

Switching Regulator DCD5, DCD6

DCD5 and DCD6 are high efficiency, synchronous step-down switching regulators capable of delivering up to 2.3A of current.

The regulators operate with a fixed 2MHz oscillator frequency allowing the use of small external components, minimizing cost and real estate. To maximize efficiency under varying load conditions the converter offers selectable modes of operation through I²C. Available modes are forced PWM (FPWM) and auto-mode (PWM/PFM). When auto-mode is selected, the regulator switches automatically between PWM and PFM mode, depending on the load condition. During heavy load the regulator operates in PWM mode at a fixed frequency. As the load decreases and the inductor valley current reaches zero, it automatically transitions into PFM mode maintaining high efficiency under light load conditions. For noise sensitive applications, the regulator can be forced into PWM mode by disabling the power-saving PFM mode. The default mode is set to auto-mode.

The on/off control of DCD5 and DCD6 can be accessed either through I²C or it will be managed be the programmed sequence.

The regulator includes an active discharge circuitry to discharge the output capacitor and hold the output voltage at ground after the regulator powers off.

Table 53: Electrical Characteristics – DCD5, DCD6

Conditions unless otherwise specified: V_{IN_DCD}= 5.0V, V_O =1.05V (default), L=1.0µH, C_{IN_DCD} = 10µF, C_O =94µF. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN_DCD}	Input voltage range	V_O < 1.8V for V_{IN_DCD} < 3.0V V_O > 0.6V for V_{IN_DCD} > 5.0V	2.7	5.0	5.25	V
V_O	Output voltage range		0.525	1.05	3.3375	V
	Regulation voltage accuracy	For factory programmed V_O	-2.0		+2.0	%
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation	V_{IN_DCD} = 2.75 – 5V		0.03		%/V
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.5 – 2A, PWM mode		0.3		mV/A
	Offset voltage in PFM mode $V_{O(PFM)} = V_{O(PWM)}+V_{offset}$	PFM mode		15		mV
I_O	Maximum output current		2.0			A
I_{PULSE}	Pulsed load current	t_{Load} < 1ms		2.3		A
I_{SHD}	Shutdown current			1.0		µA
I_{VIN_DCD}	Power stage supply current	Forced PWM mode, no load		150		µA
		Forced PFM mode, no switching		65		µA
$R_{(DSON)}$	High side switch	V_{SYS}=V_{IN_DCD}=5V; I_{OUT}= 100mA		110	160	mΩ
	Low side switch	V_{SYS}=V_{IN_DCD}=5V; I_{OUT}= 100mA		57	85	mΩ
R_{DIS}	Output discharge resistance			850	1100	Ω
F_{SW}	Switching frequency	PWM mode, GBD	1.8	2.0	2.2	MHz
$T_{ON(MIN)}$	Minimum On-Time			70		ns
T_{DCDSSR}	DCD soft-start ramp rate	15% – 90% of V_O		6		mV/µs
I_{FB}	FB5 input bias current			10.0		µA

Table 54: DCD5, DCD6 Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD5_CTL	R/W	-	-	-	-	-	-	DCD5_SEL	DCD5_EN	0x00	0x59
DCD6_CTL	R/W	-	-	-	-	-	-	DCD6_SEL	DCD6_EN	0x00	0x55

BIT	Name	Function	Default
D[7:2]	Reserved	Reserved	0
D[1]	DCDx_SEL	ON/OFF select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] register.	0
D[0]	DCDx_EN	Enable bit 0 = OFF 1 = ON	0

Table 55: On/Off Select Bit Table

D[1]	D[0]	Sequencer control	DCDx
0	X	0	OFF
0	X	1	ON
1	0	X	OFF
1	1	X	ON

Table 56: I²C Output Voltage Setting

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD5_VOUT	R/W	DCD5_RNG		DCD5_VOUT						OTP	0xA6
DCD6_VOUT	R/W	DCD6_RNG		DCD6_VOUT						OTP	0xA7

BIT	Name	Function	Default
D[5:0]	DCDx_VOUT	Output Voltage Setting (see Table 57: Output Voltage Setting – DCD5, DCD6)	OTP
D[7:6]	DCDx_RNG	Output Voltage Range select bit 00 = 0.5250 – 1.3125 increment of 12.5mV. [Default] 01 = 1.2000 – 1.9875 increment of 12.5mV. 10 = 1.8750 – 2.6625 increment of 12.5mV. 11 = 2.5500 – 3.3375 increment of 12.5mV.	OTP

Table 57: Output Voltage Setting – DCD5, DCD6

Range [00]	Range [01]	Range [10]	Range [11]	Decimal	Hex	Binary
0.5250	1.2000	1.8750	2.5500	0	00	000000
0.5375	1.2125	1.8875	2.5625	1	01	000001
0.5500	1.2250	1.9000	2.5750	2	02	000010
			. . .			
1.2875	1.9625	2.6375	3.3125	61	3D	111101
1.3000	1.9750	2.6500	3.3250	62	3E	111110
1.3125	1.9875	2.6625	3.3375	63	3F	111111

Table 58: I²C Sequencing Control – DCD5, DCD6

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD5_GRP	R/W	Reserved		DCD5_TYPE		DCD5_GROUP				OTP	0xEB
DCD6_GRP	R/W	Reserved		DCD6_TYPE		DCD6_GROUP				OTP	0xEC

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	DCDx_TYPE	Rail Type Select Bit 00 = "A" rail type. 01 = "U" rail type. 10 = "S" rail type. 11 = "SX" rail type.	OTP
D[3:0]	DCDx_GROUP	Group Delay Bit 0000b = Group 0 0001b = Group 1 0010b = Group 2 0011b = Group 3 0100b = Group 4 0101b = Group 5 0110b = Group 6 0111b = Group 7 1000b = Group 8 1001b = Group 9 1010b = Group 10 1011b = Group 11 1100b = Group 12 1101b = Group 13 1110b = Group 14 1111b = Disable	OTP

DCDs' General Registers

Forcing PWM Mode for DCDx

DCDs regulators and controllers can be independently forced into PWM mode by setting the corresponding bit of FPWM register (0xAD) to 1 through I²C communication as shown below. Note that through OTP, setting associated with D[3] sets both DCD3 and DCD4 to forced PWM mode, and that associated with D[5] sets both DCD5 and DCD6. OTP setting of DCD0, 1, 2 can be configured independently.

Table 59: Forced PWM Register – DCD0-6

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
FPWM	R/W	-	DCD6_FPWM	DCD5_FPWM	DCD4_FPWM	DCD3_FPWM	DCD2_FPWM	DCD1_FPWM	DCD0_FPWM	0x00	0xAD

BIT	Name	Function	Default
D[7]	Reserved	Reserved	0
D[6] – D[0]	DCD[X]_FPWM	0 = Auto PFM/PWM. 1 = FPWM.	OTP

DC Load-line Control

Table 60: DC Load-line Control

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCLL_CTL	R/W	Reserved					DCLL_2	DCLL_1	DCLL_0	0x03	0x1F

BIT	Name	Function	Default
D[7:3]	Reserved	Reserved	0
D[2] – D[0]	DCLL_[X]	0 = Disable DC Loadline for DCD[X] 1 = Enable DC Loadline for DCD[X]	011

AC Load-line Control

Table 61: AC Load-line Control

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
ACLL_CTL	R/W	Reserved					ACLL_DCD2	ACLL_DCD1	ACLL_DCD0	0x03	0x25

BIT	Name	Function	Default
D[7:3]	Reserved	Reserved	0
D[2] – D[0]	ACLL_[X]	0 = Disable AC Loadline for DCD[X] 1 = Enable AC Loadline for DCD[X]	011

Active DPU and DPU Count Status

Table 62: PMSTATUS

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS0_PMSTATUS	R	DPS0_PMSTATUS[7:0]								0x00	0x07
DPS1_PMSTATUS	R	DPS1_PMSTATUS[7:0]								0x00	0x0A
DPS2_PMSTATUS	R	DPS2_PMSTATUS[7:0]								0x00	0x1C
DPS3_PMSTATUS	R	DPS3_PMSTATUS[7:0]								0x00	0x1E
DPS4_PMSTATUS	R	DPS4_PMSTATUS[7:0]								0x00	0x24

BIT	Name	Function	Default
D[7:0]	DPSx_PMSTATUS[7:0]	PMSTATUS has two modes. MODE1: If the rail is off the PMSTATUS will report in hexadecimal how many DPUs are available to that rail. Each bit represents a DPU. So: • 0x1=0b0001=1 DPU available to the rail • 0x3=0x0011=2 DPUs available to the rail • 0x7=0b0111=3 DPUs available to the rail • 0xF=0x1111=4 DPUs available to the rail MODE2: If the rail is active the PMSTATUS will report in decimal how many DPUs are active at that moment: • 0d1=1 DPU active (even if ≥ 2 DPUs are available) • 0d2=2 DPUs active • 0d3=3 DPUs active • 0d4=4 DPUs active	0

DCD Rail Select for DRAMPWROK Monitor

Table 63: DCD Rail Select for DRAMPWROK Monitor

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DRAMPWROK	R/W	Reserved					DCD_SEL[2:0]			0x02	0x7C

BIT	Name	Function	Default
D[7:3]	Reserved	Reserved	0
D[2:0]	DCD_SEL[2:0]	Select DCD rail that DRAMPWROK monitor the voltage 000 = DCD0 001 = DCD1 010 = DCD2 011 = DCD3 100 = DCD4 101 = DCD5 110 = DCD6 111 = OFF. DRAMPWROK always stays low	010

DCDx Internal Soft-start Complete Status

Table 64: DCD Internal Soft-start Complete Status

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD_PG	R	RSVD	DCD6_PG	DCD5_PG	DCD4_PG	DCD3_PG	DCD2_PG	DCD1_PG	DCD0_PG	0x00	0x8F

BIT	Name	Function	Default
D[7]	Reserved		0
D[6] – D[0]	DCD[X]_PG	0 = Internal soft-start of DCD[x] has not been complete or DCD[x] is disabled 1 = Internal soft-start of DCD[x] is complete	0

DCDx Current Limit Status

Table 65: DCD Current Limit Status

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DCD_OC	R/W	RSVD	DCD6_ OC	DCD5_ OC	Reserved		DCD2_ OC	DCD1_ OC	DCD0_ OC	0x00	0xAE

BIT	Name	Function	Default
D[7]	Reserved	Reserved	0
D[6]	DCD6_OC	0 = Normal condition (no overcurrent) 1 = Overcurrent condition has occurred	0
D[5]	DCD5_OC	0 = Normal condition (no overcurrent) 1 = Overcurrent condition has occurred	0
D[4:3]	Reserved	Reserved	00
D[2]	DCD2_OC	0 = Normal condition (no overcurrent) 1 = Overcurrent condition has occurred	0
D[1]	DCD1_OC	0 = Normal condition (no overcurrent) 1 = Overcurrent condition has occurred	0
D[0]	DCD0_OC	0 = Normal condition (no overcurrent) 1 = Overcurrent condition has occurred	0

DCD0-2 Compensation and DPU Phase Shedding Control Registers

Table 66: DCD0-2 Compensation and DPU Phase Shedding Control Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS0_CONFIG	R/W	Reserved		GM0	Reserved			OFF_DLY[1:0]		0x20	0x06
DPS1_CONFIG	R/W	Reserved		GM1	Reserved			OFF_DLY[1:0]		0x20	0x09
DPS2_CONFIG	R/W	Reserved		GM2	Reserved			OFF_DLY[1:0]		0x20	0x1B

BIT	Name	Function	Default
D[7]	Reserved	Reserved	0
D[5]	GM	GM Gain Selection 0 = Set to lower GM gain 1 = Set to normal GM gain	1
D[4:2]	BW[2:0]	Reserved	000
D[1:0]	OFF_DLY[1:0]	DPU Phase shedding Timer 00 = Drop a phase 130us after load current drop below PFM level 01 = Drop a phase 65us after load current drop below PFM level 10 = Drop a phase 20us after load current drop below PFM level 11 = Disable phase-shedding.	00

DCD3-4 Compensation and DPU Phase Shedding Control Registers

Table 67: DCD3-4 Compensation and DPU Phase Shedding Control Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS3_CONFIG	R/W	RSVD	DAMPB3	GM3	BW [2:0]			OFF_DLY[1:0]		0x30	0x1D
DPS4_CONFIG	R/W	RSVD	DAMPB4	GM4	BW [2:0]			OFF_DLY[1:0]		0x30	0x23

BIT	Name	Function	Default
D[7]	Reserved	Reserved	0
D[6]	DAMPB[X]	0 = Select default compensation 1 = Select alternative compensation	0
D[5]	GM	GM Gain Selection 0 = Set to lower GM gain 1 = Set to normal GM gain	1
D[4:2]	BW[2:0]	Bandwidth Adjustment TBD	100
D[1:0]	OFF_DLY[1:0]	DPU Phase shedding Timer 00 = Drop a phase 130us after load current drop below PFM level 01 = Drop a phase 65us after load current drop below PFM level 10 = Drop a phase 20us after load current drop below PFM level 11 = Disable phase-shedding.	00

DCD5-6 Compensation and DPU Phase Shedding Control Registers

Table 68: DCD5-6 Compensation and DPU Phase Shedding Control Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DPS56_CONFIG	R/W	Reserved				GM6	BW6	GM5	BW5	0x0A	0x0D

BIT	Name	Function	Default
D[7:4]	Reserved	Reserved	0000
D[3]	GM6	GM Gain Selection 0 = Set to lower GM gain 1 = Set to normal GM gain	1
D[2]	BW6	Bandwidth Selection 0 = Use normal bandwidth 1 = Set to lower bandwidth	0
D[1]	GM5	GM Gain Selection 0 = Set to lower GM gain 1 = Set to normal GM gain	1
D[0]	BW5	Bandwidth Selection 0 = Use normal bandwidth 1 = Set to lower bandwidth	0

PMIC Control State Machine Status

Table 69: PMIC Control State Machine Status

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
TSMSTATUS	R	TSMSTATUS[7:0]								0x00h	0x9B

BIT	Name	Function	Default
D[7:0]	TSMSTATUS[7:0]	Indicate PMIC's operating state 0000 = SOC_G3 0001 = SOC_S4 0011 = SOC_S3 0111 = SOC_S0IX 1111 = SOC_S0	0

Power Consumption at Light Load Considerations

Power dissipation at light load is predominantly from the current used by internal circuitry through VSYS, current consumption to perform switching activity of DCDs switching power supply, and quiescent current of LDOs. To achieve the greatest power saving, rails can be manually disabled with I^2C. When DPUs are used with regulators (DCD0-2) or controllers (DCD3/4), there is additional current consumption used by DPU's internal logic and for performing switching activity. To minimize the power consumption from switching activity, auto-mode (PWM/PFM) can be used. For DCD0-2 regulator, the internal FETs are performing the switching activity in light load, so there is no switching activity done by DPU(s) thus minimal power dissipation on the DPU(s). For DCD3/4 the switching activity is always performed by the DPU(s).

The table below shows a typical consumption of an example configuration without any output current load and P9148 as the DPU. VSYS is the baseline current with internal circuitry still operating, while all DCDs and all LDOs, except LDO7, are OFF. P9180A Iq represents the additional current into VSYS and DCD_VIN or LDO_VIN of the respective rail. DCD3/4 are manually set to auto-PFM/PWM mode for greatest power saving. The power consumption in each state (e.g. S3, S4) can be calculated from summing the power loss of the rails that remain active in that state.

	DPU qty	Vin [V]	Vout [V]	P9180A Iq [mA]	P9148 Iq [mA]	Power loss [mW]
Vsys Logic	-	5.0	-	1.000	-	5.00
DCD0	4	5.0	OFF	0.105	0.720	4.13
DCD1	0	5.0	1.00	0.500	-	2.50
DCD2	1	5.0	1.10	0.500	0.180	3.40
DCD3	1	5.0	1.05	0.250	0.550	4.00
DCD4	1	5.0	3.30	0.250	0.550	4.00
DCD5	-	5.0	1.80	0.500	-	2.50
DCD6	-	5.0	1.24	0.500	-	2.50
LDO0	-	1.8	-	0.022	-	0.04
LDO1	-	1.8	-	0.022	-	0.04
LDO2	-	1.8	-	0.022	-	0.04
LDO3	-	1.8	-	0.020	-	0.04
LDO4	-	1.8	-	0.020	-	0.04
LDO5	-	1.1	-	0.095	-	0.10
LDO6	-	5.0	-	0.020	-	0.10
				Total		28.42

Enable Pins

All enable signals are open drain output signals. The polarity is set to low active by default. EN0 to EN4 can be fuse-programmed to be high active upon PMIC start-up. The on/off control of each regulator is controlled either through the programmed sequence or by I²C.

Table 70: Electrical Characteristics – Enable Pins

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{pullup}	External Pull-up Voltage				5.25	V
V_{OL}	Output Voltage Low	I_{OUT} = 2mA			0.4	V
I_{SNK}	Current Sink	V_{ENx} = 0.4V		10		mA
I_{LKG}	Leakage current			100		nA

Table 71: I²C Control Register – EN0 to EN11

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
EN0_CTL	R/W	Reserved					Polarity	EN0_SEL	EN0_EN	0x00	0x56
EN1_CTL	R/W	Reserved					Polarity	EN1_SEL	EN1_EN	0x00	0x57
EN2_CTL	R/W	Reserved					Polarity	EN2_SEL	EN2_EN	0x00	0x5B
EN3_CTL	R/W	Reserved					Polarity	EN3_SEL	EN3_EN	0x00	0x5C
EN4_CTL	R/W	Reserved					Polarity	EN4_SEL	EN4_EN	0x00	0x5D
EN5_CTL	R/W	Reserved					Polarity	EN5_SEL	EN5_EN	0x00	0x69
EN6_CTL	R/W	Reserved					Polarity	EN6_SEL	EN6_EN	0x00	0x68
EN7_CTL	R/W	Reserved					Polarity	EN7_SEL	EN7_EN	0x00	0x64
EN8_CTL	R/W	Reserved					Polarity	EN8_SEL	EN8_EN	0x00	0x62
EN9_CTL	R/W	Reserved					Polarity	EN9_SEL	EN9_EN	0x00	0x6B
EN10_CTL	R/W	Reserved					Polarity	EN10_SEL	EN10_EN	0x00	0x6C
EN11_CTL	R/W	Reserved					Polarity	EN11_SEL	EN11_EN	0x00	0x6D

BIT	Name	Function	Default
D[7:3]	Reserved	Reserved	0
D[2]	Polarity	Polarity bit 0 = Active low. 1 = Active high.	EN0-4: OTP EN5-11: 0
D[1]	ENx_SEL	ON/OFF Select bit 0 = ON/OFF is controlled by configured device sequence. 1 = ON/OFF is controlled by D[0] on this register.	0
D[0]	ENx_EN	Enable bit 0 = OFF 1 = ON	0

Table 72: On/Off Select Bit Table – Enable Pins

D[1]	D[0]	Sequencer control	Enable Pin
0	X	0	HIGH
0	X	1	LOW
1	0	X	HIGH
1	1	X	LOW

Table 73: I²C Sequencing Control – EN0 to EN11

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
EN0_GRP	R/W	Reserved		EN0_TYPE		EN0_GROUP[1]				OTP	0xF4
EN1_GRP	R/W	Reserved		EN1_TYPE		EN1_GROUP[1]				OTP	0xF5
EN2_GRP	R/W	Reserved		EN2_TYPE		EN2_GROUP[1]				OTP	0xF6
EN3_GRP	R/W	Reserved		EN3_TYPE		EN3_GROUP[1]				OTP	0xF7
EN4_GRP	R/W	Reserved		EN4_TYPE		EN4_GROUP[1]				OTP	0xF8
EN5_GRP	R/W	Reserved		EN5_TYPE		EN5_GROUP[1]				OTP	0xF9
EN6_GRP	R/W	Reserved		EN6_TYPE		EN6_GROUP[1]				OTP	0xFA
EN7_GRP	R/W	Reserved		EN7_TYPE		EN7_GROUP[1]				OTP	0xFB
EN8_GRP	R/W	Reserved		EN8_TYPE		EN8_GROUP[1]				OTP	0xFC
EN9_GRP	R/W	Reserved		EN9_TYPE		EN9_GROUP[1]				OTP	0xFD
EN10_GRP	R/W	Reserved		EN10_TYPE		EN10_GROUP[1]				OTP	0xFE
EN11_GRP	R/W	Reserved		EN11_TYPE		EN11_GROUP[1]				OTP	0x7D

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	ENx_TYPE	Rail Type Select Bit 00 = “A” rail type. 01 = “U” rail type. 10 = “S” rail type. 11 = “SX” rail type.	OTP
D[3:0]	ENx_GROUP	Group Delay Bit 0000b = Group 0 0001b = Group 1 0010b = Group 2 0011b = Group 3 0100b = Group 4 0101b = Group 5 0110b = Group 6 0111b = Group 7 1000b = Group 8 1001b = Group 9 1010b = Group 10 1011b = Group 11 1100b = Group 12 1101b = Group 13 1110b = Group 14 1111b = Disable	OTP

Sequencing Signal Registers

Group-Delay Timing

Group-delay timing registers defined the time delay between two consecutive Group-Delay indexes, and are applicable to LDOs, DCDs, and ENs (LDOx_GROUP, DCDx_GROUP, ENx_GROUP) as they are assigned to respective rail type (A, U, S, SX). With OTP the group-delay within each type during turn-on and turn-off are the same.

Table 74: Group-Delay Timing

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
SEQA_TIM	R/W	RSVD	DLY_GRP_OFF_A[2:0]			RSVD	DLY_GRP_ON_A[2:0]			OTP	0xC3
SEQU_TIM	R/W	RSVD	DLY_GRP_OFF_U[2:0]			RSVD	DLY_GRP_ON_U[2:0]			OTP	0xC4
SEQS_TIM	R/W	RSVD	DLY_GRP_OFF_S[2:0]			RSVD	DLY_GRP_ON_S[2:0]			OTP	0xD3
SEQSX_TIM	R/W	RSVD	DLY_GRP_OFF_SX[2:0]			RSVD	DLY_GRP_ON_SX[2:0]			OTP	0xD4

BIT	Name	Function	Default
D[7]	RSVD	Reserved	0
D[6:4]	DLY_GRP_OFF_X[2:0]	Group delay when group-type turns off 000 = 0.25ms 001 = 0.50ms 010 = 1.00ms (default) 011 = 1.50ms 100 = 2.00ms 101 = 2.50ms 110 = 3.00ms 111 = 5.00ms	OTP
D[3]	RSVD	Reserved	0
D[2:0]	DLY_GRP_ON_X[2:0]	Group delay when group-type turns on 000 = 0.25ms 001 = 0.50ms 010 = 1.00ms (default) 011 = 1.50ms 100 = 2.00ms 101 = 2.50ms 110 = 3.00ms 111 = 5.00ms	OTP

General Purpose IOs

The P9180A offers 15 general purpose input/output ports (GPIO) divided into two banks. Each bank has a separated power supply input dividing the GPIO's into a 1.8V (VGPIO0) and 3.3V (VGPIO1) domain. VGPIO0 powers GPIO[8:0], the VGPIO1 supply input powers GPIO[14:9].

Each GPIO can be configured either as CMOS output, open drain output or input. Unless specified, all the GPIO's are defaulted as CMOS input with a weak 50kΩ pull down.

Table 75: Electrical Characteristics – GPIO[8:0]

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VGPIO0	Input Power Supply	C_{IN}= 1µF	1.71	1.8	1.89	V
Input Configuration						
V_{IL}	Input low voltage				0.35*VGPIO0	V
V_{IH}	Input high voltage		0.65*VGPIO0			V
V_{HYS}	Hysteresis			0.33		V
I_{IL}	Input low current	V_{IL}= GND		0		µA
I_{IH}	Input high current	V_{IH}= 1.8V, 50k pull-down		36		µA
CMOS Output Configuration						
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		VGPIO0-0.4			V
I_{OL}	Output low current			4		mA
I_{OH}	Output high current			4		mA
T_{RISE}	Rise time	C_L= 150pF, 10 – 90%, GBD	10		45	ns
T_{FALL}	Fall time	C_L= 150pF, 90 – 10%, GBD	10		45	ns
Open Drain Configuration						
V_{OL}	Output low voltage				0.40	V
I_{OL}	Output low current			12		mA
I_{LKG}	Leakage current			100		nA

Table 76: Electrical Characteristics – GPIO[14:9]

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VGPIO1	Input Power Supply	C_{IN} = 1µF	3.0	3.3	3.6	V
Input Configuration						
V_{IL}	Input low voltage				0.35*VGPIO1	V
V_{IH}	Input high voltage		0.65*VGPIO1			V
V_{HYS}	Hysteresis			0.33		V
I_{IL}	Input low current	V_{IL}= GND		0		µA
I_{IH}	Input high current	V_{IH}= 3.3V, 50k pull-down		66		µA

CMOS Output Configuration						
V_{OL}	Output low voltage				0.40	V
V_{OH}	Output high voltage		VGPIO1-0.40			V
I_{OL}	Output low current			4.0		mA
I_{OH}	Output high current			4.0		mA
T_{RISE}	Rise time	C_L= 150pF, 10 – 90%, GBD	10		45	ns
T_{FALL}	Fall time	C_L= 150pF, 90 – 10%, GBD	10		45	ns
Open Drain Configuration						
V_{OL}	Output low voltage				0.40	V
I_{OL}	Output low current			12		mA
I_{LKG}	Leakage current			100		nA

Table 77: GPIO Output Configuration Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIOCTLO0	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x7C	0x3B
GPIOCTLO1	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x7C	0x3C
GPIOCTLO2	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x7C	0x3D
GPIOCTLO3	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x7C	0x3E
GPIOCTLO4	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x7C	0x3F
GPIOCTLO5	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x7C	0x40
GPIOCTLO6	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x41
GPIOCTLO7	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x42
GPIOCTLO8	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x2B
GPIOCTLO9	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x2C
GPIOCTLO10	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x2D
GPIOCTLO11	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x2E
GPIOCTLO12	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x2F
GPIOCTLO13	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x30
GPIOCTLO14	R/W	Reserved	ALT_FUNC	DIR	DRV	REN	RVAL[1:0]		DOUT	0x0C	0x31

<table>
<tr><th>BIT</th><th>Name</th><th colspan="2">Function</th><th>Default</th></tr>
<tr><td>D[7]</td><td>Reserved</td><td colspan="2">Reserved</td><td>0</td></tr>
<tr><td>D[6]</td><td>ALT_FUNC</td><td colspan="2">Alternative Function
0 = Disabled.
1 = Enabled.</td><td></td></tr>
<tr><td></td><td></td><td colspan="2">Alternative Function
Disabled/Enabled</td><td></td></tr>
<tr><td></td><td></td><td>GPIO0 / DCD2_DIO [default DCD2_DIO]</td><td>GPIO8 / SLEEP [default GPIO8]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO1 / DCD2_DIF [default DCD2_DIF]</td><td>GPIO9 / VDDQSEL [default GPIO9]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO2 / DCD1_DIO [default DCD1_DIO]</td><td>GPIO10 / ADC0 [default GPIO10]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO3 / DCD1_DIF [default DCD1_DIF]</td><td>GPIO11 / ADC1 [default GPIO11]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO4 / DCD0_DIO [default DCD0_DIO]</td><td>GPIO12 / ADC2 [default GPIO12]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO5 / DCD0_DIF [default DCD0_DIF]</td><td>GPIO13 / PANEL_EN [default GPIO13]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO6 / PWM0 [default GPIO6]</td><td>GPIO14 / BACKLIGHT_EN [default GPIO14]</td><td></td></tr>
<tr><td></td><td></td><td>GPIO7 / PWM1 [default GPIO7]</td><td></td><td></td></tr>
<tr><td>D[5]</td><td>DIR</td><td colspan="2">Pin Direction
0 = Input.
1 = Output.</td><td></td></tr>
<tr><td>D[4]</td><td>DRV</td><td colspan="2">Output Driver Type</td><td></td></tr>
</table>

BIT	Name	Function	Default
		0 = Open Drain. 1 = CMOS (push-pull).	
D[3]	REN	Internal Pull Up Enable/Disable 0= Pull Up/Pull Down disabled. 1= Pull Up/Pull Down enabled.	
D[2:1]	RVAL	Internal Pull Up Resistor Value 00= 2KΩ Pull Down. 10 = 50KΩ Pull Down. 01= 2KΩ Pull Up. 11= 50KΩ Pull Up.	
D[0]	DOUT	Pin Output Value 0= Low. 1= High or High-Z.	

Table 78: GPIO Input Configuration Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIOCTLI0	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x43
GPIOCTLI1	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x44
GPIOCTLI2	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x45
GPIOCTLI3	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x46
GPIOCTLI4	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x47
GPIOCTLI5	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x48
GPIOCTLI6	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x49
GPIOCTLI7	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x4A
GPIOCTLI8	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x33
GPIOCTLI9	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x34
GPIOCTLI10	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x35
GPIOCTLI11	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x36
GPIOCTLI12	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x37
GPIOCTLI13	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x38
GPIOCTLI14	R/W	Reserved			GPIGLBYP	GPIDBNC	INTCNT[1:0]		DIN	0x00	0x39

BIT	Name	Function	Default
D[7:5]	Reserved	Reserved	0
D[4]	GPIGLBYP	Glitch Filter ByPass Enable 0 = Glitch filter enabled. 1 = Glitch filter by-passed.	
D[3]	GPIDBNC	De-Bounce Enable 0= De-bounce disabled. 1= De-bounce enabled.	
D[2:1]	INTCNT	Interrupt Detect 00= Disable. 10 = Positive Edge. 01= Negative Edge. 11= Both Edges.	
D[0]	DIN	Pin Status 0= Input low. 1= Input high.	

Pulse Width Modulation (PWM) Generator

PMIC supports two PWM outputs with programmable frequencies of ~183 Hz to a maximum required frequency of ~23.4 kHz and duty cycle granularity of 1/256.

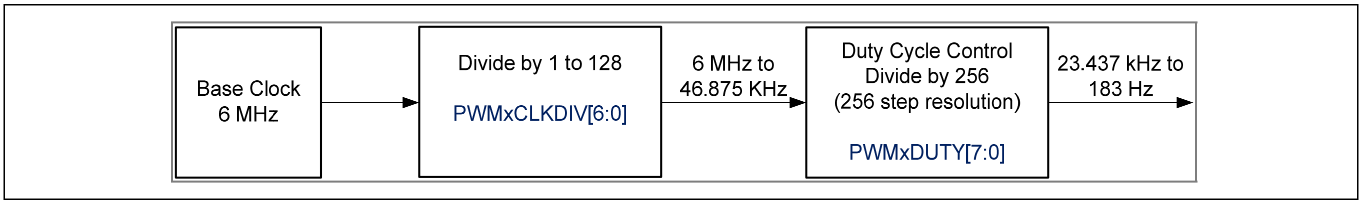


Figure 4: PWM Block Diagram

The PWM sub-block is clocked by a 6MHz internal oscillator. A 7-bit counter counts from 0 to CLKDIV[6:0]. When CLKDIV[6:0] is reached, a 7-bit comparator resets the 7-bit counter to 0. This effectively divides the BASECLK by the 7-bit value CLKDIV[6:0], giving divider options of 2 to 128. The BASECLK division may also be bypassed by setting CLKDIV[6:0] to 0x00.

The Duty Cycle Logic block uses a 7-bit counter from 0x00 to 0xFF, giving 0.39% (1/256) duty cycle granularity in the PWM output. The desired duty cycle of the PWM output is set by DUTYCYCLE[7:0]. When the 8-bit counter output is less than the value of DUTYCYCLE[7:0], the output is HIGH. When the counter value is equal to or greater than the value of DUTYCYCLE[7:0], the output is LOW. When the counter value reaches 0xFF, the counter is reset back to 0x00. The counter output is buffered before driving the external pin. The buffer's power supply is 1.8V (GPIO0VDD).

The PWM frequency is not intended to change on-the-fly (asynchronously). The PWM output must be first disabled before writing to the PWMxCLKDIV[7] registers. The PWM duty cycle however is expected to be changed while the PWM output is enabled.

Each individual PWM output has two control registers to set the clock divider and one to set the duty cycle of each PWM output.

Table 79: PWMxCLKDIV –Clock Divider Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PWM0CLKDIV	R/W	Enable	CLKDIV0[6:0]							0x00	0x4B
PWM1CLKDIV	R/W	Enable	CLKDIV1[6:0]							0x00	0x4C

BIT	Name	Function	Default
D[7]	Enable	1=PWM output enabled 0=PWM output disabled	0
D[6:0]	CLKDIV0[6:0]	Clock divider for PWM[0]. 0x00: Pass-through. No divider. DIVIDEDCLK = BASECLK. 0x01 - 0xFF: DIVIDEDCLK = BASECLK / (CLKDIV[6:0] + 1) Example: If CLKDIV0[6:0] = 0x0000, DIVIDEDCLK = BASECLK If CLKDIV0[6:0] = 0x0063, DIVIDEDCLK = BASECLK / 100 If CLKDIV0[6:0] = 0xFF, DIVIDEDCLK = BASECLK / 256	0

Table 80: PWMxDUTYCYCLE – Duty Cycle Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PWM0DUTYCYCLE	R/W	DUTYCYCLE0[7:0]								0x00	0x4E
PWM1DUTYCYCLE	R/W	DUTYCYCLE1[7:0]								0x00	0x4F

BIT	Name	Function	Default
D[7:0]	DUTYCYCLE[7:0]	0x00 - 0xFF: Duty cycle = (DUTYCYCLE0[7:0] + 1)/256 (0.39% to 100%) Example: If DUTYCYCLEx[7:0] = 0x00, duty cycle = 0.39% (1/256) If DUTYCYCLEx[7:0] = 0x01, duty cycle = 0.781% If DUTYCYCLEx[7:0] = 0xFF, duty cycle = 100%	0

BLIGHT_EN and PANEL_EN Overview

The PMIC provides two outputs for display panel control, BLIGHT_EN to enable the display backlight and PANEL_EN to enable the display panel electronics. The function to control the backlight and display is turned-off by default and must be enabled first. The registers that control the display panel are described below.

Table 81: BLIGHT_EN Output Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
BLIGHT_EN	R/W	Reserved							BACKLIGHT_ENOUT	0x00	0x51

BIT	Name	Function	Default
D[7:1]	RSVD	Reserved	0
D0	BACKLIGHT_ENOUT	Enable Pin Output Value 0 = Low 1 = High (CMOS)	0

Table 82: PANEL_EN Output Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PANEL_EN	R/W	Reserved							PANEL_ENOUT	0x00	0x52

BIT	Name	Function	Default
D[7:1]	RSVD	Reserved	0
D0	PANEL_ENOUT	Enable Pin Output Value 0 = Low 1 = High (CMOS)	0

Sleep State Inputs, Soft-start-Done and Reset Signals

Table 83: Electrical Characteristics – SLP_S4_B, SLP_S3_B, SLP_S0IX_B, SUSPWRDNACK, PLTRST_B, THERMTRIP_B

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage				0.65	V
V_{IH}	Input high voltage		1.45			V

Table 84: Electrical Characteristics – RSMRST_B, COREPWROK

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VGPIO1	Input Power Supply	C_{IN} = 1µF	3.0	3.3	3.6	V
V_{OL}	Output low voltage				0.40	V
V_{OH}	Output high voltage		VGPIO1-0.40			V
I_{OL}	Output low current			4.0		mA
I_{OH}	Output high current			4.0		mA
T_{RISE}	Rise time	C_L= 150pF, 10 – 90%, GBD	10		45	ns
T_{FALL}	Fall time	C_L= 150pF, 90 – 10%, GBD	10		45	ns

Table 85: Electrical Characteristics – VCCAPWROK, DRAMPWROK

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output low voltage				0.40	V
I_{OL}	Output low current			12		mA
I_{LKG}	Leakage current			100		nA

Table 86: Electrical Characteristics – IRQ, SDWN_B, MODEM_OFF_B, PWRBTN_B

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VGPIO0	Input Power Supply	C_{IN} = 1µF	1.71	1.8	1.89	V
V_{OL}	Output low voltage				0.40	V
V_{OH}	Output high voltage		VGPIO0-0.40			V
I_{OL}	Output low current			4.0		mA
I_{OH}	Output high current			4.0		mA
T_{RISE}	Rise time	C_L= 150pF, 10 – 90%, GBD	10		45	ns
T_{FALL}	Fall time	C_L= 150pF, 90 – 10%, GBD	10		45	ns

Table 87: Electrical Characteristics – PROCHOT_B

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output low voltage				0.40	V
I_{OL}	Output low current			12		mA
I_{LKG}	Leakage current			100		nA

I²C Interface

The P9180A is a slave device only. It is designed to operate with a wide frequency range of 400kHz – 3.4MHz. The PMIC is accessed using a 7-bit addressing scheme. The PMIC I²C slave is not allowed to stretch the clock, and is capable of being multi-mastered in a debug environment. The I²C bus is only used for non-latency critical register access and communication between the SoC and PMIC.

Table 88: Electrical Specifications - I²C

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Voltage (V_{DD} = LDO7)		1.71	1.8	1.89	V
V_{IL}	Input low voltage			0.3*V_{DD}		V
V_{IH}	Input high voltage		0.7*V_{DD}			V
V_{HYS}	Hysteresis		0.1			V
V_{OL}	Output low voltage				0.2*V_{DD}	V
C_{PIN}	Capacitance	SDA & SCL pins	2		5	pF
T_{FALL_HS}		3.33Mb/s Operation	10		40	ns
T_{FALL_FS}		400Kb/s Operation	20		300	ns
T_R/T_F	Rise and Fall times		30		70	%

The PMIC supports the standard I²C read and write functions. The configuration register space is covered into one 256-byte partitions. The PMIC supports four 7-bit device addresses configurable through register EXP2 (0x92), bits [7:6]. The address can be configured as 0x5E (1011110), 0x6E (1101110), 0x4F (1001111), and 0x77 (1110111) to allow for cases where multiple P9180A's are used on the same board or other I2C address conflicts arise. Note that in 8-bit format, these addresses correspond to 0xBC, 0xDC, 0x9E, and 0xEE for writes, and 0xBD, 0xDD, 0x9F, and 0xEF for reads.

	7-bit	8-bit (Write)	8-bit (Read)
Device 1	0x5E	0xBC	0xBD
Device 2	0x6E	0xDC	0xDD
Device 3	0x4F	0x9E	0x9F
Device 4	0x77	0xEE	0xEF

Table 89: I²C Addresses

Reading data back from PMIC registers follow the "combined protocol" as described in the I²C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details.

The following diagrams capture the different high-speed and fast-speed transaction format/protocol.

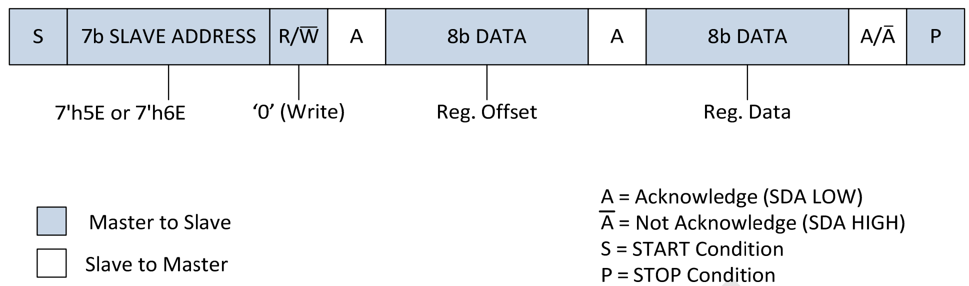


Figure 5: I²C Fast Speed Write

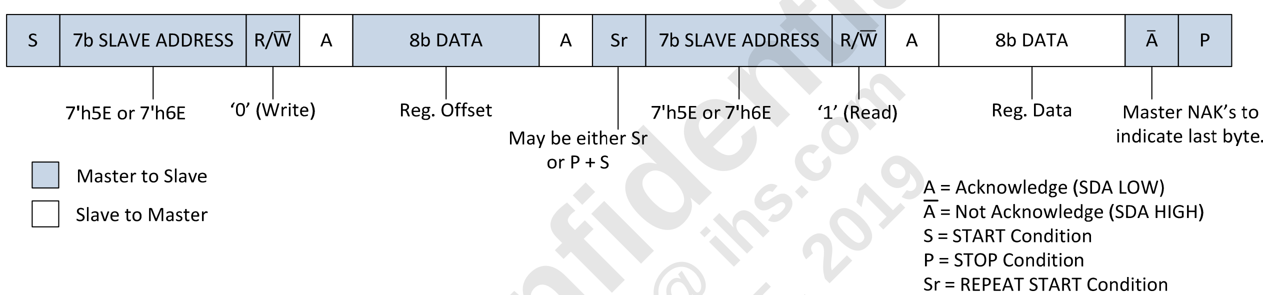


Figure 6: I²C Fast Speed Read

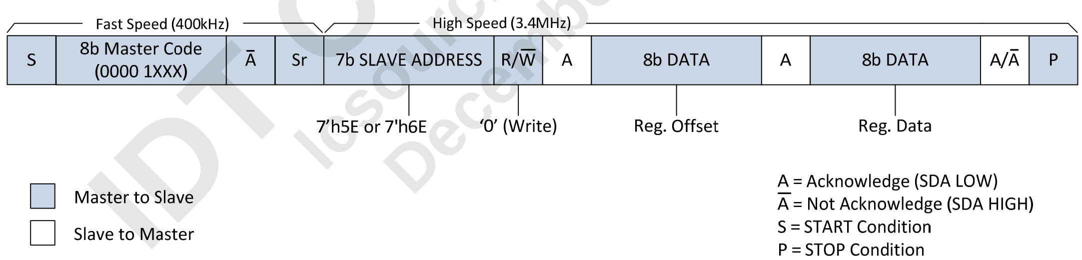


Figure 7: I²C High Speed Write

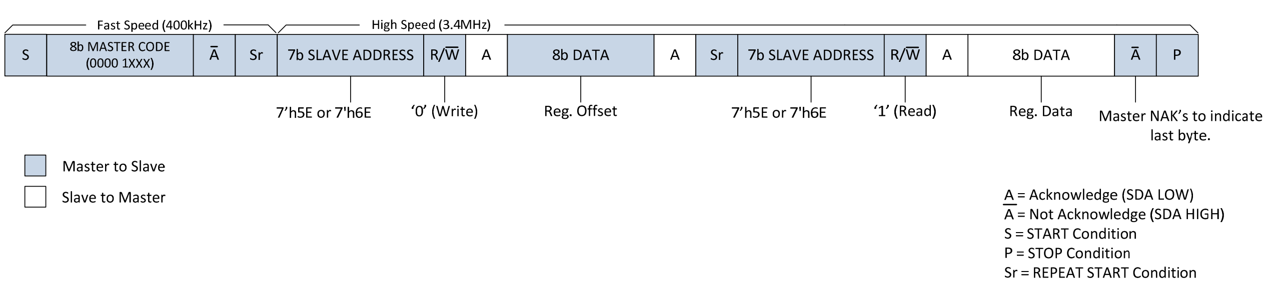


Figure 8: I²C High Speed Read

Sequential offset accesses within a single transaction ("burst" reads and writes) are supported by P9180A's I²C module.

Register Requirements

Two read-only registers below are provided to allow the customer to track the vendor and revision of their chip.

Table 90: Vendor Identification Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VENDOR_ID	R	VENDOR_ID[7:0]								0x28	0x00

Table 91: Chip Revision Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
REVISION	R	RSVD		MAJREV0[2:0]			MINREV0[2:0]			0x01	0x01

Bit	Name	Function	Default
D[7:6]	RSVD	RSVD	00
D[5:3]	MAJREV0[2:0]	Major Revision: The first stepping should start with ‘000’ and increment by 1 for each new complete mask stepping 000 = A 001 = B 010 = C 011 = D 100 = E 101 = F 110 = G 111 = H	000
D[2:0]	MINREV0[2:0]	Minor Revision; The first stepping should start with ‘000’ and increment by 1 for each new metal layer stepping. Resets to ‘000’ when MAJREV increments 000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7	001

Analog to Digital Converter (ADC)

The PMIC includes a general purpose, 10bit, analog to digital converter. It is used for measuring system voltages, die temperature, and regulator output currents. The table below lists the used channels of the ADC:

CHANNEL	DESCRIPTION	EXTERNAL PINS	SIGNAL RANGE
1	PMIC die temperature	n/a	-30˚C to 125˚C
2	VSYS Voltage	VSYS	3V to 5.525V
3	System Voltage 0	ADC0	0 to 1.2V
4	System Voltage 1	ADC1	0 to 1.2V
5	System Voltage 2	ADC2	0 to 1.2V
6	DCD0 Current	Internal	DCD0 Max Current
7	DCD1 Current	Internal	DCD1 Max Current
8	DCD2 Current	Internal	DCD2 Max Current
9	DCD5 Current	Internal	DCD5 Max Current
10	DCD6 Current	Internal	DCD6 Max Current

Current Monitor

Each of DCD0, DCD1, DCD2, DCD5, and DCD6 switching regulators are monitored for output current. The current sensing is done internally and averaged across 1ms. The average current is digitalized by using a 10 bits ADC (refer to ADC section) and stored into 2 x 8 bits registers for each voltage rail in both SVID and I²C registers shown in VR Current Monitoring section.

Table 92: Analog to Digital Converter Electrical Characteristics

Conditions unless otherwise specified: T_A= 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF}	ADC reference voltage	Internally provided		1.2		V
$I_{DD(ADC)}$	Supply Current	Full scale current		60		µA
RES	ADC resolution			10		Bits
INL	Integral Non Linearity	GBD	-2		+2	LSB
DNL	Differential Non Linearity	GBD	-1		+1	LSB
Gain	Gain Error	Mid scale	-1		+1	LSB
$V_{MEAS(ADC)}$	ADC input voltage	External pins ADC[2:0]	0		1.2	V
		VSYS	0		5.6	V
SF	Voltage scale factor	External pins ADC[2:0]		1.0		V/V
		VSYS		$\frac{3}{14}$		V/V
$R_{IN(ADC[x])}$	ADC[2:0] input resistance			10		MΩ

Power Buttons PWRBTNIN_B and PMIC_EN

The PMIC offers two ways to trigger the system to power on or off: PMIC_EN and PWRBTNIN_B. It is recommended that only one power-on/off method is used, either with PWRBTNIN_B or PMIC_EN. If PWRBTNIN_B is used, PMIC_EN should be tied low. If PMIC_EN is used to power-on/off the PMIC, the PWRBTNIN_B pin should be left floating (unconnected). However, the PWRBTNIN_B pin is still monitored and will pass level changes to the PWRBTN_B output. When the PMIC is used with DPU(s), PWRBTNIN_B (or PMIC_EN when used) should not be asserted until DPU is powered on.

PMIC Enable (PMIC_EN)

PMIC_EN is an active high signal and is usually driven by a system controller or power-good signal of a pre-regulator. After asserting the PMIC_EN pin high the PMIC powers on without delay and the rails are turned on following the programmed sequence. De-asserting the PMIC_EN signal initiates a shutdown of all rails, following the programmed shut-down sequence. PMIC_EN can be asserted high (1.55V typ. for 5V VSYS, and 1.15V typ. for 3V VSYS) after VSYS has reached a steady state level, and is above $VSYSREF_R$. This can be achieved by adding RC filter (10kOhm and 1uF) from VSYS to PMIC_EN pin. Pull PMIC_EN low (1.05V typ. for 5V VSYS, and 0.75V VSYS for 3V VSYS) to disable the rails.

Power Button input (PWRBTNIN_B) & Power Button output (PWRBTN_B)

The power button pin (PWRBTNIN_B) is an active-low input to the PMIC. It is internally connected to VSYS through a weak pull-up current source (50uA, ±10%). It includes a 30ms de-bouncing circuit to ensure that spurious transitions aren't logged while the switch contacts bounce on initial contact. The output of the de-bouncing circuit enters the edge detect circuits. The falling edge can trigger a transition out of the SoC G3 state. This pin is usually connected thru a push-button switch to ground. Pressing the PWRBTNIN_B longer than 30ms will turn on the PMIC. If the PMIC is powered-on, holding down the power button for longer than a set time (default of 4 seconds) will force a Cold Off.

The output of the de-bouncing circuit also goes to the timer logic block that measures the length of time that the Power Button has been held down, and this value can be read from the Hold Time field (HT[3:0]) in the PBSTATUS register.

The PMIC always passes the power button information via an output signal PWRBTN_B to the SoC. PWRBTN_B is a level shifted copy of PWRBTNIN_B after the 30ms de-bouncing circuit. PWRBTN_B is valid when RSMRST_B=1 (de-asserted).

If the system is off (SoC G3 state), pressing the Power Button by itself for greater than 30ms will cause the PMIC to turn on all the "A" type rails, de-assert RSMRST_B (PWRBTN_B should be high before this) and pass the power button information to the SoC. If the system is on (SoC S4/S3/S0iX/S0 states), pressing this button will cause the PMIC to pass a level shifted copy of PWRBTNIN_B (via PWRBTN_B) after the 30ms de-bouncing circuit to the SoC, which will initiate actions for the PMIC to perform.

Forcing a Cold Off using Power Button

The output of both the power button feed into a fault timer which measures the time from when the button is pressed until it is released. This duration (in half-seconds) can be read from the hold time bit field, PBHT[2:0]. The timer retains this value until the next time both buttons are pressed simultaneously, or if the timer logic is reset by the CLRHT bit in PBCONFIG.

The PMIC triggers a Cold Off if the fault timer exceeds the duration set in the Fault Time field (FLT[3:0]) in the PBCONFIG register (default of 4 seconds). If enabled (FLT is not equal to 0h) the power-down logic compares the hold time bits to the fault time bits, and forces a Cold Off upon a match. If software control is desired, FLT can be set to 0h during the PMIC initialization, but this default will allow a forced power down if for some reason the software cannot boot properly. Software must set the CLRHT bit in PBCONFIG before updating FLT to prevent the fault condition from possibly triggering immediately from a previous value.

Configuration Registers

Table 93: Power Button Configuration Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PBCONFIG	R/W	RSVD	RSVD	CLRHT	CLRFLT	FLT[3:0]				0x08	0x26

BIT	Name	Function	Default
D[7]	RSVD	Reserved	0
D[6]	RSVD	Reserved	0
D[5]	CLRHT	This bit is self clearing and always reads 0 0 = No action performed 1 = Reset the HT timer logic.	0
D[4]	CLRFLT	This bit is self clearing and always reads 0 0 = No action performed 1 = Reset the FLT timer logic.	0
D[3:0]	FLT[3:0]	Time that the power button has to be held down, in half-second intervals, before a system shutdown is triggered. 0000 = Disabled 0001 = .5 second 0010 = 1 seconds 0011 = 1.5 seconds 0100 = 2 seconds .... 1111 = 7.5 seconds	1000

Table 94: Power Button Status Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
PBSTATUS	R/W	Reserved			PBLVL	PBHT[3:0]				0x10	0x27

BIT	Name	Function	Default
D[7:5]	Reserved	Reserved	0
D[4]	PBLVL	0 = Power button pressed 1 = Power button released	1
D[3:0]	PBHT	Time that the power button has been held down, in half-second intervals: 0000 = 0 seconds 0001 = .5 second 0010 = 1 seconds 0011 = 1.5 seconds 0100 = 2 seconds .... 1111 = 7.5 seconds	0

VBAK Charger

The P9180A provides the capability to charge an external SuperCap or coin cell. The charger output is pin VBAK. The VBAK voltage domain powers two PMIC-internal registers which store system events, like over-temperature shutdown or UVLO shutdown, and the charger configuration VBAK_VCHG and VBAK_RCHG.

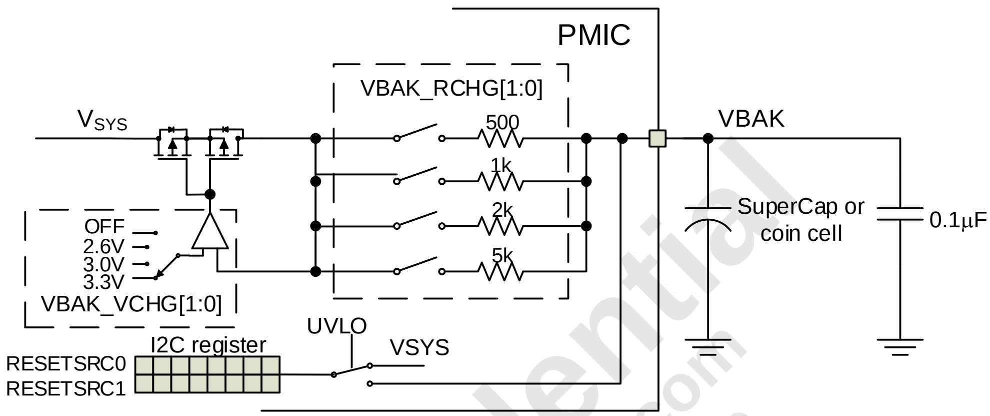


Figure 9. VBAK Charger Block Diagram

In case VSYS is disconnected and below the UVLO threshold, VBAK is powered by the SuperCap or coin cell and will retain information until the battery or SuperCap voltage on VBAK drops below 0.8V and stored data is reset.

The charger output remains active after the PMIC enters SoC-G3 state, however, after the system is exiting SoC-G3 via PWRBTNIN_B, the charger registers VBAK_VCHG and VBAK_RCHG are reset and have to be re-enabled via I2C.

Table 95: Electrical Characteristics – VBAK

V_{SYS}= 5.0V, C_O = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{O(BAK)}$	Output voltage setting	VBAK_VCHG[1:0]	00		Disabled		V
			01		2.6		
			10		3.0		
			11		3.3		
I_{SHDN}	Shutdown current				790		µA
	Regulation voltage accuracy			-1.5		+1.5	%
$R_{CHG(BAK)}$	Internal series resistance	VBAK_RCHG[1:0]	00		500		Ω
			01		1k		
			10		2k		
			11		5k		
$I_{LIM(BAK)}$	Maximum output current	VBAK_VCHG[1:0] (VSYS = 3.5-5.25V VBAK_RCHG[1:0] = 500 Ω)	2.6V	0.95	1.1	1.25	mA
			3.0V	1.65	1.9	2.15	
			3.3V	2.15	2.5	2.85	
$C_{O(BAK)}$	External output capacitor	Optional			0.1		µF

THEORY OF OPERATION

The P9180A is an integrated power-management IC (PMIC) targeted for applications powered by a rechargeable battery or a regulated 5V system supply. The product offers seven configurable step-down converters capable of delivering up to 5.0A load current for memory, processor core, I/O, auxiliary, pre-regulation for LDOs. In addition, the device includes 8 low dropout linear regulators that can be supplied from a battery or a regulated supply. The PMIC is configured/controlled via I2C. Other features include 15 general purpose I/O (GPIO), push button control, integrated state machine for power sequencing and thermal management.

The P9180A is rated for a wide temperature range of -40 to +85ºC, and is offered in two packages options: 8mm x 8mm QFN package and 9mm x 9mm GQFN package.

Control Signals

RSMRST_B

Resume reset is an output signal. When all A-rails are switched-on and are in regulation, RSMRST_B is pulled high to VGPIO1 (3.3V). RSMRST_B is pulled low when the A-rails are powered down and the device enters SoC G3.

DRAMPWROK

DRAMPWROK is an open-drain output signal. It is pulled high when DCD2 (SOC VDDQ rail) is above 90% of its regulating voltage during the soft-start process. DRAMPWROK is logic low when DCD2 is shutdown.

VCCAPWROK

VCCAPWROK is an active-high open-drain output signal. VCCAPWROK asserts when all voltage rails that are supposed to be on in group S0IX and S0 soft start are completed. The nominal voltage of VCCAPWROK is high when asserted, 0V when de-asserted.

COREPWROK

COREPWROK is an active high dedicated output signal. COREPWROK asserts when all voltage rails that are supposed to be on in group S0IX and S0 soft start are completed. The nominal voltage of COREPWROK is VGPIO1 (3.3V) when asserted, 0V when de-asserted. COREPWROK does not de-assert in S0IX state.

Shallow Sleep State Mode (SLP_S0IX_B)

SLP_S0IX_B is an input signal from the SoC indicating shallow sleep mode. When SLP_S0IX_B is pulled low, the SoC launches shallow sleep entry task list. All the active switching regulators are placed into power save mode per S0IX state. Prior to initiating the sleep mode entry, the SoC will program exit VID values for VCC over SVID and communicate standby state information to the PMIC over I^2C.

Sleep Mode State 3 (SLP_S3_B)

SLP_S3_B is a dedicated input pin for enabling and disabling the low power Sleep Mode State. When pulled low, sleep mode is initiated, and all the power rails are turned off according the timing diagram. Prior to activating the sleep mode, the SoC will program exit VID values for VCC/VNN over SVID and communicate standby state information to the PMIC over I^2C. It is valid when RSMRST_B=1.

Deep Sleep Mode (SLP_S4_B)

SLP_S4_B is a dedicated input pin for enabling and disabling the Deep Sleep Mode State. When pulled low, deep sleep mode is initiated, and all the power rails are turned off according the timing diagram. Prior to activating the deep sleep mode, the SoC will program exit VID values for VCC/VNN over SVID and communicate standby state information to the PMIC over I^2C. It is valid when RSMRST_B=1 (de-asserted) and SLP_S3_B=0 (asserted).

Platform Reset (PLTRST_B)

Platform reset pin is an input signal from the SoC that indicates the SoC already came out of reset upon de-assertion (PLTRST_B=1). The nominal voltage of PLTRST_B is 0V when asserted, 1.8V when de-asserted.

Suspend Power Down Acknowledgement (SUSPWRDNACK)

Suspend Power Down Acknowledgement is an input signal from the SoC telling the PMIC to turn off all A rails. It is valid when RSMRST_B=1 (de-asserted) and SLP_S4=0 (asserted). The nominal voltage of SUSPWRDNACK is 1.8V when asserted, 0V when de-asserted.

Interrupt Request (IRQ)

Interrupt request is an output signal generating interrupts to the SoC. It is pulled high when at least one unmasked interrupt bit is set in the 1st level interrupt register. It is valid when RSMRST_B=1 (de-asserted). The nominal voltage of IRQ is 1.8V when pulled high, 0V when pulled low. The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms.

Thermal Trip (THERMTRIP_B)

THERMTRIP is an active low dedicated input signal that notifies the PMIC of a SoC thermal event. It is valid when RSMRST_B=1 and PLTRST_B=1 (de-asserted). The nominal voltage of THERMTRIP is 0V when asserted, 1.8V when de-asserted. Upon sensing the THERMTRIP signal has transitioned low, the PMIC must shut down all rails immediately (hard shutdown, not executing a Cold-Off task list). To avoid spurious detection during power sequencing, the THERMTRIP signal is only to be sampled if PLTRST_B is de-asserted.

Processor HOT (PROCHOT_B)

PROCHOT_B is an active-low, open-drain output signal used to notify the SoC of a PMIC, battery or system thermal event. PROCHOT_B will be asserted when the PMIC temperature, battery temperature or system temperature has crossed the alert thresholds define in the thermal monitoring section. It is valid when RSMRST_B=1 and PLTRST_B=1 (de-asserted). The nominal voltage of PROCHOT_B is 0V when asserted, 1.0V when de-asserted. The SoC must go into a lower power state until the PMIC thermal event is cleared and the pin is de-asserted.

Shutdown Warning (SDWN_B)

The Shut-Down Warning is an output signal sent from P9180A to the modem as a warning that a system shutdown event is about to take place. During power down task lists, the SDWN_B is pulled to ground. If the power down is not initiated, the output signal is pulled high (1.8V).

If the PMIC enters a catastrophic shutdown condition which would normally bypass a Cold Off task list being run, the SDWN_B pin is asserted a minimum of 90µs prior to this catastrophic shutdown commencing.

The nominal voltage of SDWN_B is 0V when asserted, 1.8V when de-asserted.

SVID Interface

Serial Voltage Identification (SVID)

To dynamically adjust the voltage settings of the SoC rails, the SoC communicates with the P9180A through SVID interface. SVID's commands comprise of 9 bits – 4 MSBs determine the address and 5 LSBs are the command bits. P9180A PMIC supports 3 SVID voltage regulators – DCD0, DCD1 and DCD2. The SVID address of each voltage regulator can be changed by OTP setting or I²C register write.

Table 96: SVID_ID – SVID ID Setting for DCD0/DCD1/DCD2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
SVID_ID	R/W			SVID_ID_DCD2		SVID_ID_DCD1		SVID_ID_DCD0		OTP	0xAC

BIT	Name	Function	Default
D[7:6]	Reserved	Reserved	0
D[5:4]	SVID_ID_DCD2	DCD2 SVID address 00 = 0x2 (default) 01 = 0x0 10 = 0x1 11 = 0x3	OTP
D[3:2]	SVID_ID_DCD1	DCD1 SVID address 00 = 0x1 (default) 01 = 0x0 10 = 0x2 11 = 0x5	OTP
D[1:0]	SVID_ID_DCD0	DCD0 SVID address 00 = 0x0 (default) 01 = 0x1 10 = 0x3 11 = 0x4	OTP

Serial Voltage Identification (SVID) Command Set

DCD0, DCD1 and DCD2 implement VR12.1/IMVP8 SVID protocol. Table below list the SVID command set supported by P9180A PMIC.

Table 97. Serial Voltage Identification (SVID) Command Set

#	Command	Master payload contents	Slave payload contents	Description
01h	SetVID-fast (Individual address & all call address)	VID code	NA	Applicable for DCD0, DCD1 and DCD2. Set the new VID target, VR Jumps to new VID target with controlled (up or down) slew rate programmed by the VR. When VR receives VID moving up command it will exit all low power states to the normal state to ensure the fastest slew to the new voltage. VR sets VR_settled bit and issues alert when VR has reached new VID target.
02h	SetVID-slow (Individual address & all call address)	VID code	NA	Applicable for DCD0, DCD1 and DCD2. Set the VID target, VR Jumps to new VID target with controlled slew rate (up or down) programmed by the VR. When VR receives VID moving up command it will exit all low power states to the normal state. VR sets VR_settled and issues alert when VR has reached new VID target.
03h	SetVID-decay (Individual address & all call address)	VID code	NA	Applicable for DCD0, DCD1 and DCD2. Sets the VID target, VR jumps to new VID target, but does not control the slew rate, the output voltage decays at a rate proportional to the load current. SetVID-decay is only used in VID down direction and implies VR goes to PS2 state. VR sets VR_settled and Alert line is asserted for SetVID-decay.
04h	SetPS	Byte indicating power status of voltage rail	NA	Applicable for DCD0, DCD1 and DCD2. SoC set the power state of the VR according to core P-state and C-state so that VR controller can be configured to improve efficiency, especially at light load
05h	SetRegADR (Individual address only. NAK all call address)	Address of the index in the data table	NA	Sets the address pointer in the data register table. Typically the next command SetRegDAT is the payload that gets loaded into this address. However for multiple writes to the same address, only one SetRegADR is needed.
06h	SetRegDAT (Individual address only. NAK all call address)	New data register contents	NA	Writes the contents to the data register that was previously identified by the address pointer with SetRegADR.
07h	GetReg (Individual address only. NAK all call address)	Define which register	Specified register contents	Slave returns the contents of the specified register as the payload. The majority of the VR monitoring data is accessed through the GetReg command.

VR 12.1 Compatibility

The P9180A has been developed with according to the VR12.0 specification, but does support the VR12.1 extension with the features required for the Intel© "Braswell" SoC. The below table documents the implementation (YES=Supported)

Table 98: VR12.1 Compliance

Feature (X=required, O=Optional)	VR12.1	P9180A	Notes
VID 0.25-1.52V	X	0.25-1.30V	0.5-1.30V according to Braswell Specification
Dynamic VID Fast	X	YES	Minimum or Target slew rate.
Dynamic VID Slow	X	YES	Minimum or Target slew rate
Decay Slew Rate	X	YES	
Voltage Settled	X	YES	
PS0/PS1 VR Power States	X	YES	Normal Power Mode
PS2 - VR Power State	X	YES	Very low power mode
PS3 - VR Power State	X	YES	Ultra low power state.
PS4 - VR Power State	X	YES	Near Off mode.
Temp Max	O	YES	OTP or pin programmed, Read by master, supports temperature zones & VRHOT trip point
Temp Sensor Input	X	YES	Rails that support turbo must have Temp sensor inputs
DCLL	X	YES	Register support for OTP programming of DCLL is optional. However, DCLL programmability is required.
Enable	X	YES	VR enable
VR Ready	X	YES	Single phase output ready
VR_Hot#	X	YES	Active low thermal monitor output, utilizing either temperature sensor input.
Address	X	YES	OTP or pin programmed.
Capability (06H)	1xxx xxx1b	YES	
Icc_Max (21h)	X	YES	Must be programmed by platform designer to reflect capability of platform. Default 00h indicates this value is not programmed and platform won't boot.
Temp_Max (22h)	O	NO	
Slew Rate Fast (24h)	X	YES	Indicate slew rate fast capability of VR
Slew Rate Slow (25h)	X	YES	Indicate slew rate slow capability of VR
Vboot (26h)	X	YES	OTP or pin programmed, not read by master, PWM must support various Vboot levels
VR Tolerance (27h)	O	NO	Optional read by master
Current Calibration offset (28h)	O	NO	OTP or pin programmed, not read by master, used in PWM only
Temp Calibration(29h)	O	NO	OTP or pin programmed, not read by master, used in PWM only
Vout Max (30h)	X	YES	Programmed by master

Voltage Offset (33h)	X	YES	Programmed by master
Iout (15h)	X	YES	Read by master
VR Temperature (17h) (ADC)	O	NO	Read by master
Output Voltage (16h) (ADC)	O	NO	Read by master
Output Power (18h) (ADC)	O	NO	Read by master
Temperature Zone(12h)	X	YES	Read by master
Multi VR Config (34h)	X	YES	

Table below list the SVID register set and the corresponding I²C register supported by P9180A PMIC for DCD0, 1, 2.

Table 99: Serial Voltage Identification (SVID) Register Set

SVID Reg#	I2C Reg#	Register	Description	Access (SOC)	Default
00h	00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID is assigned by Intel. This register is mandatory and the VR must return the assigned vendor ID.	Read Only	28h
01h	B3h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	Read Only	00h
02h	01h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The vendor assigns this data.	Read Only	01h
10h	B6h	Status_1	Data register read after the alert# signal is asserted. Conveying the status of the VR.	Read Only	00h
11h	B7h	Status_2	Data Register showing status_2 data. Conveying the status of the SVID bus.	Read Only	00h
15h	84h 86h 8Ch	DCD0/DCD1/ DCD2 Output Current, Iout (H)	Running 1 ms averaging update. 10 bits ADC, store the upper 8 MSB of the ADC output onto this register.	Read Only	00h
1Ch	B8h	Status2_last read	This register contains a copy of the Status_2 data that was last read with the GetReg (Status_2) command. In the case of a communications error or parity error, when the VR is sending the payload back to the master, the master can read the Status2_lastread register so the alert data is not lost.	Read Only	00h
26h	DCh	Vboot	Data register containing Vboot voltage, OTP programmed. VR12 VID format, IE 97h = 1.0 Volts	Read Only	97h
30h	BDh	Vout max	This register is programmable by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “Reject, not supported” acknowledge. VR12.1 VID data format. Must be programmed by MASTER during boot up sequence if a value other than default is desired. Offset (33h) does not affect Vout_max. IE VID+offset can be > Vout_max.	Read/Write	D2h =>1.295V
31h	BEh	VID setting	Data register containing currently programmed VID voltage. VID data format. Default is 00h, zero volts out, VR off.	Read/Write	00h
32h	BFh	PWR state	Register containing the current programmed power state. Default is 00h, normal power mode	Read/Write	00h

33h	C0h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for the margin 2s complement.
			00h = no margin.
			01h = +1 VID step,
			02h = +2 VID steps
			FFh = -1 VID step
				Read/Write	00h

39h	-	S0IX VID	Data register containing the VID voltage that is used to DECAY to when the SLP_S0IX_B is asserted and PLTRST_B de-asserted (enter S0IX state); The voltage ramps to Vboot (#26h) register using slow ramp set in Vslew (#2Ah) at de-assertion of SLP_S0IX_B (exit from S0IX state).	Read/Write	00h

CONTROL AND MONITORING

State Machine

The PMIC implements a simple state machine which interprets a very limited “instruction set”. Its purpose is to execute basic power sequencing and thermal monitoring tasks without requiring intervention by the HW/SW, from code stored locally. This section outlines the functions that state machine shall perform.

In P9180A power-state transition (power sequencing) related tasks and general purpose Analog to Digital converter tasks are handled concurrently. The intention is ensure that power sequencing tasks are always handled in a time-deterministic manner (that is, they cannot be delayed by other tasks being requested of the ADC, etc.)

Execution

On power up, the state machine will begin in the IDLE state. When an event occurs (the Cold Boot event is set by default), execution of tasks associated with that event are started automatically. Once the end of the task list is reached, the state machine will cease execution and return to the IDLE state.

Input Power Source Detection

The PMIC supports only analog detection of VSYS.

System Voltage (VSYS) Detection Threshold

A voltage comparator is used to compare the VSYS voltage level to a reference voltage in order to determine whether VSYS is up and valid. The output of the comparator is used to inform the PMIC a power state transition between G3 and SoC G3.

VSYS Rising
When the VSYS level at the comparator becomes higher than reference voltage (including rising edge hysteresis), VSYS is considered valid.

VSYS Falling
When the VSYS level at the comparator becomes lower than reference voltage (including falling edge hysteresis), VSYS is considered invalid.

The requirements of the analog voltage referred to here as VSYSREF, used as the “Valid VSYS” threshold, are detailed in the table below.

Table 100: VSYSREF Definition

Parameter	Description	Min	Typ	Max	Unit
$VSYSREF_R$	VSYS Rising Threshold		2.90		V
$VSYSREF_F$	VSYS Falling Threshold		2.50		V

Power States

The PMIC has six defined states which are characterized by the behavior of platform power rails, SoC sideband signals (COREPWROK, PLTRST_B), and internal state machine modes. Below is the description of each of the states.

- G3
  - No valid platform power sources exist.
  - VBAT and VBAK are below VMIN for the PMIC internal logic power rail VPL.

- This is a true “G3” state. No power is consumed in this state.

- SoC-G3
  - The PMIC internal logic power rail VPL is powered, either from the RTC backup battery (VBAK>VMIN), main battery or an adapter (VSYS > $VSYSREF_R$).
- SoC-S0
  - All SoC rails have been powered up.
  - PLTRST_B is de-asserted. COREPWROK is asserted. (SoC has begun code execution.)
  - The SoC may choose to power up/down any of the “Default Off” rails as SW demands.
- SoC-S0IX
  - Low-power platform state which will be entered and exited by sleep state signal SLP_S0IX.
  - PLTRST_B is de-asserted. COREPWROK is asserted.
  - Temperature monitoring state machine enters a “standby” mode with reduced frequency of temperature measurements.
- S3
  - Low-power platform state which will be entered and exited by sleep state signal SLP_S3.
  - PLTRST_B is asserted. COREPWROK is de-asserted.
- S4
  - Low-power platform state which will be entered and exited by sleep state signals SLP_S4.
  - PLTRST_B is asserted. COREPWROK is de-asserted.

G3 State

In the “G3” state, the PMIC is completely powered off, with no valid power sources available on the platform. To enter this state, all power sources (battery and adapter) must have been removed from the system.

In this state, no rails are in regulation. No PMIC logic is active. In this state, the device appears to be “off” to the user.

Exit from this state is triggered by the application of a valid power source. Transitions out of this state are summarized in the table below.

Table 101. G3 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Main Battery Insertion	VSYS > $VSYSREF_R$	SoC G3	When VSYS input voltage is sufficiently high (above $VSYSREF_R$), PMIC waits for PWRBTNIN_B or PMIC_EN to be pressed/toggled I^2C Register Map is reset to defaults.
Main Battery Becomes Valid			
USB or DC Adapter Insertion			

SoC-G3 State

By default, in the “SoC G3” state, the only system rail present is VPL - an internal standby rail powering battery-backed logic.

The events causing a transition out of the ‘SoC G3’ state are shown in the table below.

Table 102. SoC G3 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Main Battery Removal / Depletion	$VSYS < VSYSREF_F$	G3	VPL-powered logic loses state, resets to defaults.
Adapter Removal			
Power Button Pressed PMIC_EN toggles high	$VSYS > VSYSREF_R$	SoC S4	Start Cold Boot sequence to boot platform.

SoC S0 State

In the "SoC S0 State", the PMIC has completed bring-up of the platform, and released the SoC from reset. In this state, the behavior of PMIC state machines may be directly modified and controlled by the SoC, through commands issued over the I^2C and SVID interfaces.

In this state, the device will appear "on" to the user.

The events causing a transition out of the 'SoC S0' state are shown in the table below.

Table 103. SoC S0 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Power Source Removal	$VSYS < VSYSREF_F$	G3	VPL-powered logic loses state, resets to defaults.
Thermal Critical Event		SoC G3	Hardware-enforced shutdown of rails.
Non-Thermal Critical Event			Execute Cold Off Task List.
Power Button Held	Power button timer expires	SoC S3	PMIC passes PWRBTNIN_B information to SoC. The SoC may Toggle SLP_S3_B=0 then SLP_S4_B=0, then SUSPWRDNACK=1 to finally enter SoC G3, up to the SoC to decide.
Power Button Held		S0IX or SoC S3	PMIC passes PWRBTNIN_B information to SoC. The SoC may: • Toggle SLP_S0IX_B = 0 enter S0IX or • Toggle SLP_S3_B=0 then SLP_S4_B=0, then SUSPWRDNACK=1 to finally enter SoC G3 It's up to the SoC to decide.

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Warm Reset	PLTRST_B = 0	SoC S0	Resets I^2C and SVID.
SLP_S0IX	SLP_S0IX_B = 0	SoC S0IX	Enter S0IX task list.

Shallow Sleep Mode State (SoC S0IX)

The SoC supports three possible standby states: S0IX (shallow sleep mode), S3 (sleep mode) and S4 (deep sleep mode). Each of these states represents a different level of SoC standby, with S0IX being the “shallowest” (highest power) and S4 being the “deepest” (lowest power). Each of these three sub-states has its own entry task list, required because of the different states of power rails in each.

The entering and exiting of each the SoC S0IX state is controlled by a signal which is delivered to the PMIC by the SoC via a dedicated physical pin SLP_S0IX.

- Rails that are on:
  - They are shown in the power sequencing diagrams
  - VRs shall be placed in PFM/power save mode
  - Internal PMIC rails
- Interfaces available:
  - SVID is ON in S0IX
  - I^2C is ON in S0IX
- Input source comparators and interrupts active.
- All registers powered, with states retained.
- Thermal monitoring of the PMIC is disabled.

The events causing a transition out of the ‘SoC S0IX’ state are shown in the table below.

Table 104. S0IX State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Power Source Removal	VSYS < $VSYSREF_F$	G3	VPL-powered logic loses state, resets to defaults.
Thermal Critical Event		SoC G3	Hardware-enforced shutdown of rails (no Task List).
Non-Thermal Critical Event			Execute Cold Off Task List.
Power Button Held	Power button timer expires	SoC S3	PMIC passes PWRBTNIN_B information to SoC. The SoC may Toggle SLP_S3=0 then SLP_S4=0, then SUSPWRDNACK=1 to finally enter SoC G3, up to the SoC to decide.

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Power Button Held		SoC S0 or SoC S3	PMIC passes PWRBTNIN_B information to SoC. The SoC may • Toggle SLP_S0IX_B = 1 to exit S0IX or • Toggle SLP_S3=0 then SLP_S4=0, then SUSPWRDNACK=1 to finally enter SoC G3 It's up to the SoC to decide.
Warm Reset	PLTRST_B = 0	SoC S0IX	Resets I^2C and SVID
SLP_S0IX	SLP_S0IX_B = 1	SoC S0	Exit S0IX task list.

Sleep Mode State (SoC S3)

The entering and exiting of each the SoC S3 state is controlled by a signal which is delivered to the PMIC by the SoC via a dedicated physical pin SLP_S3.

- Rails that are on:
  - They are shown in the power sequencing diagrams
  - Switching regulators may be placed in Power-Save mode (PFM)
  - Internal PMIC rails
- Interfaces available:
  - SVID is OFF in S3
  - I^2C is OFF in S3
- Input source comparators and interrupts active.
- All registers powered, with states retained.
- Thermal monitoring of the PMIC is disabled.

The events causing a transition out of the 'SoC S3' state are shown in the table below.

Table 105. SoC S3 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Power Source Removal	$VSYS < VSYSREF_F$	G3	VPL-powered logic loses state, resets to defaults.
Thermal Critical Event		SoC G3	Hardware-enforced shutdown of rails (no Task List).
Non-Thermal Critical Event			Execute Cold Off Task List.

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Power Button Held	Power button timer expires	SoC S4	PMIC passes PWRBTNIN_B information to SoC. The SoC may toggle SLP_S4=0 then SUSPWRDNACK=1 to finally enter SoC G3, up to the SoC to decide.
Power Button Held	If exit S3 to SoC S0	SoC S0 or SoC S4	PMIC passes PWRBTNIN_B information to SoC. The SoC may • Toggle SLP_S3=1 to exit S3 or • Toggle SLP_S4=0 then SUSPWRDNACK=1 to finally enter SoC G3 It's up to the SoC to decide.
SLP_S3	SLP_S3_B = 1	SoC S0	Exit S3 task list.
SLP_S4	SLP_S4_B = 0	SoC S4	Enter S4 task list.

Deep Sleep Mode (SoC S4 State)

The entering and exiting of each the SoC S4 state is controlled by a signal which is delivered to the PMIC by the SoC via a dedicated physical pin SLP_S4. The exiting of deep sleep mode: also gated by BATLOW_B.

- Rails that are on:
  - They are shown in the power sequencing diagrams
  - Switching regulators shall be placed in Power-Save Mode (PFM)
  - Internal PMIC rails
- Interfaces available:
  - SVID is OFF in S4
  - I^2C is OFF in S4
- Interrupts active.
- All registers powered, with states retained.
- Thermal monitoring of the PMIC is disabled.

The events causing a transition out of the 'SoC S4' state are shown in the table below.

Table 106. Deep Sleep Mode: State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Power Source Removal	$VSYS < VSYSREF_F$	G3	VPL-powered logic loses state, resets to defaults.
SUSPWRDNACK	SUSPWRDNACK = 1		
Thermal Critical Event		SoC G3	Hardware-enforced shutdown of rails (no Task List).
Non-Thermal Critical Event			Execute Cold Off Task List.
Power Button Held	Power button timer expires	SoC G3	PMIC passes PWRBTNIN_B information to SoC. The SoC may set SUSPWRDNACK=1 to enter SoC G3, up to the SoC to decide.
Power Button Held	If exit S4 to SoC S3	SoC S3 or SoC G3	PMIC passes PWRBTNIN_B information to SoC. The SoC may: • Toggle SLP_S4_B=1 to exit S4 or • Toggle SLP_S4_B=0 then SUSPWRDNACK=1 to finally enter SoC G3 It's up to the SoC to decide
SLP_S4_B=1		SoC S3	Exit S4 task list.

Power State Transitions

The following is a summary of the 10 power state transitions defined for the PMIC.

- Cold Boot
- Warm Reset
- Enter Standby S0IX
- Exit Standby S0IX
- Enter Standby S3
- Exit Standby S3
- Enter standby S4
- Exit Standby S4
- Cold Off
- Modem Reset

Some of these state transitions are triggered by hardware events, such as the power button being pressed, or power source insertion. But the transitions are gated by signals, SLP_S0IX, SLP_S3, SLP_S4 and SUSPWRDNACK from the SoC if these signals are present in power sequence diagrams.

The behaviors associated with each of these state transitions are stored in PMIC's power sequencing state machine. The sections below discuss the trigger sources of each transition and the default sequencing behavior during each.

The voltage rails are classified in the following categories which will be referred to in such a way to simplify the power state transition (power sequencing) diagrams:

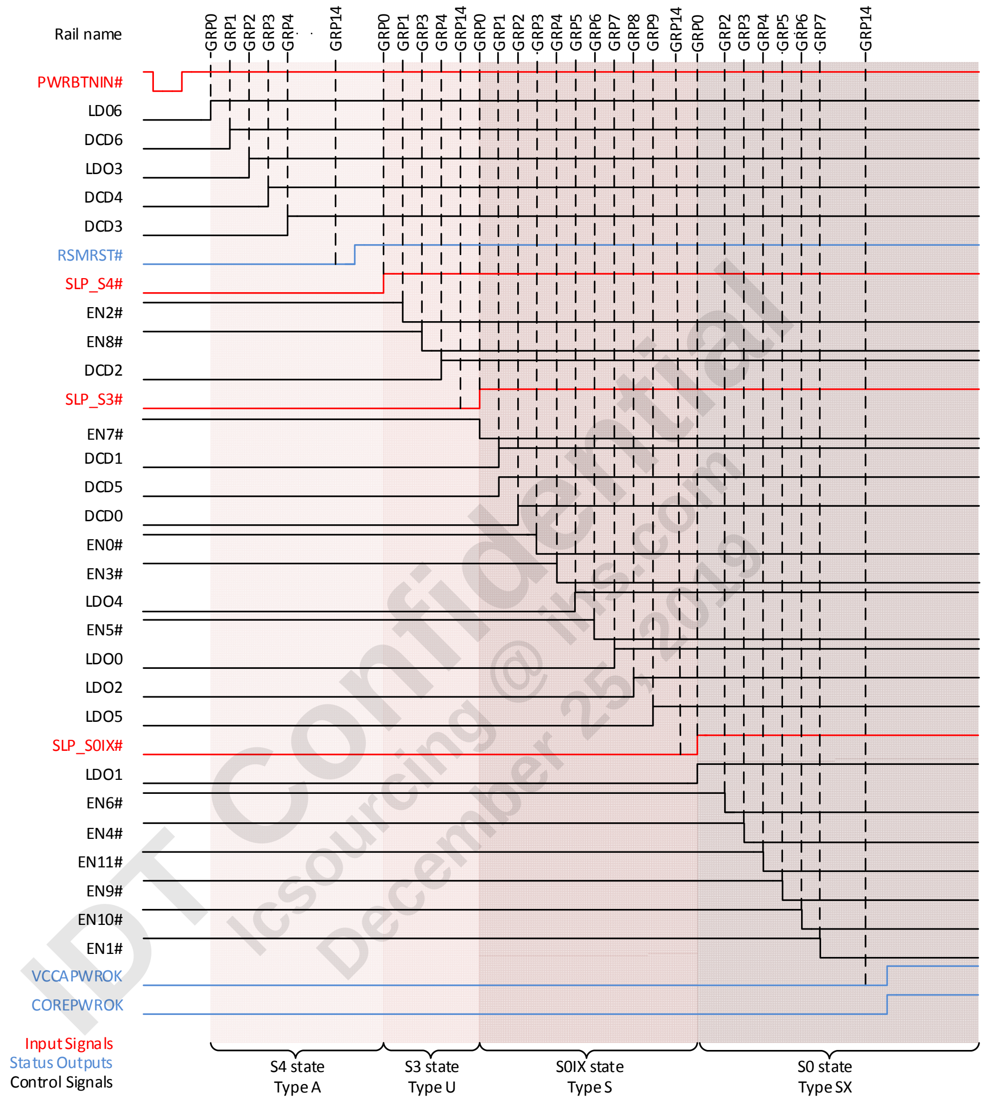


Figure 10. Power Sequence Timing Diagram

- SUS rails (A rails): DCD6 (V1.0A), LDO3 (V1.2A), DCD4 (V1.8A), and DCD3 (V3.3A). They together with LDO6 (VUSBPHY) remain on in “SoC S4” state. They are turned off in “SoC G3” state.
- U rails: DCD2 (VDDQ). It remains on in “SoC S3” state, and is turned off in “SoC S4” state.
- S rails: among them are DCD1 (VNN), DCD5 (V1.05S), DCD0 (VCC), LDO4 (V1.2S), LDO0 (V1.5S), LDO2 (V1.35S), and LDO5 (VDDQ_VTT). They remain on in “SoC S0IX” state. They are turned off in “SoC S3” state.
- SX rails: LDO1 (VSFRSX). It is on in “SoC S0” state, and is turned off in “SoC S0IX” state.
- Default On rails: VRs that are turned during COLD BOOT by the power sequencing state machine
- Defaults Off rails: VRs that are not turned during COLD BOOT by the power sequencing state machine. They are managed by the SoC. Their on/off status depends on a platform device or other conditions.

Cold Boot

A cold boot sequence is followed whenever the PMIC is fully turning on the system from a powered-down state. As such, a cold boot sequence begins at the “SoC G3” state, and terminates at the “SoC S0” state. Once all of the rails are on, the COREPWROK signal will assert and the PLTRST_B will de-assert. This will effectively turn on the SoC in order for it to begin executing code and controlling the system.

During this state transition, one or more of the sleep signals (SLP_Sx) could be asserted at some point of time. The VRs that are turned on during the transition should not be put in low power mode even if some of the sleep signals may still be asserted since the end state of cold boot is SoC S0 state.

During this state transition, the SoC rails are sequenced in an order critical to SoC operation. In addition, the rails are turned on one at a time in a ramp-rate controlled manner (voltage slew rate limited) in order to avoid battery inrush current situations that could cause shut down events.

All the triggers listed in the table below will cause the PMIC to bring up the SUS rails. After that, signals from the SoC (SLP_S4, SLP_S3) are needed for the PMIC to complete the cold boot sequence.

Table 107. Cold Boot Triggers

Event	Conditions (all must be satisfied)
Power Button Pressed	$VSYS > VSYSREF_R$

Warm Reset

A Warm Reset resets the SoC as well as the I^2C and SVID interfaces in the PMIC. Configuration registers are not reset to default (unless explicitly defined otherwise).

During a Warm Reset, only the PLTRST_B pin from the SoC is toggled. All rails remain in regulation during the reset.

Table 108. Warm Reset Triggers

Event	Conditions (all must be satisfied)
Warm Reset Request	SoC toggles the PLTRST_B=0

Shallow Sleep State Mode (SLP_S0IX_B)

SLP_S0IX_B is an input signal from the SoC indicating shallow sleep mode. In this mode, the PMIC consumes the highest power. When SLP_S0IX_B is pulled low, the SoC launches shallow sleep entry task list. All the active switching regulators are placed into power save mode per S0IX state. Prior to initiating the sleep mode entry, the SoC will program exit VID values for VCC over SVID and communicate standby state information to the PMIC over I^2C.

Table 109. Enter and exit SoC S0IX Triggers

Event	Conditions (all must be satisfied)
Enter SoC S0IX Request	SLP_S0IX_B = 0
Exit SoC S0IX Request	SLP_S0IX_B=1

When pulled high, the PMIC exits the shallow sleep mode. VDDQ_VTT and SX rails are turned on. The VCC rail will be turned on by SVID commands (not by SLP_S0IX_B). The rest of the rails will come out of PFM/power save mode.

The SLP_S0IX_B signal is ignored if either SLP_S3_B or SLP_S4_B are connected to logic low. It should only be considered valid if RSMRST_B=1. The nominal voltage of SLP_S0IX_B is 0V when asserted, 1.8V when de-asserted.

Sleep Mode State 3 (SLP_S3_B)

SLP_ S3 is a dedicated input pin for enabling and disabling the low power Sleep Mode State. When pulled low, sleep mode is initiated, and all the power rails are turned off according to the below timing diagram. Prior to activating the sleep mode, the SoC will program exit VID values for VCC/VNN over SVID and communicate standby state information to the PMIC over I^{2}C. It is valid when RSMRST_B=1.

Table 110. Low Power Sleep Mode Entry and Exit

Event	Conditions (all must be satisfied)
Sleep Mode Entry	SoC pulls SLP_S3_B pin low (SLP_S3_B=LOW)
Sleep Mode Exit	SoC pulls SLP_S3_B pin high (SLP_S3_B =HIGH)

Deep Sleep Mode (SLP_S4_B)

SLP_S4_B is a dedicated input pin for enabling and disabling the Deep Sleep Mode State. When pulled low, deep sleep mode is initiated, and all the power rails are turned off according to the below timing diagram. Prior to activating the deep sleep mode, the SoC will program exit VID values for VCC/VNN over SVID and communicate standby state information to the PMIC over I^{2}C. It is valid when RSMRST_B=1 (de-asserted) and SLP_S3_B=0 (asserted).

Table 111. Deep Sleep Mode Entry and Exit

Event	Conditions (all must be satisfied)
Enter SoC S4 Request	SoC asserts the SLP_S3_B pin (SLP_S3_B=LOW)
Exit SoC S4 Request	SoC de-asserts the SLP_S4_B pin (SLP_S3_B=HIGH).

Cold Off

A Cold Off, either through a SoC request or a system event, puts the PMIC in the 'Mechanical Off' state. The system remains in this state until the Power button is pressed, or until VSYS is removed.

Table 112. Cold Off Triggers

Event	Conditions (all must be satisfied)
Non-Thermal Critical Event	VSYS removal SUSPWRDNACK = 1 & SLP_S4_B = 0 & RSMRST_B = 1
Power Button Held	Power button timer expires SUSPWRDNACK = 1 RSMRST_B = 1 SLP_S4_B = 0
Power Button Held	Power button pressed for a defined length (up to SoC to define the length) SUSPWRDNACK = 1 & SLP_S4_B = 0 & RSMRST_B = 1

Modem Reset

A Modem Reset task list is initiated by setting the MODEMRSTSEQ bit in the MODEMCTRL register. (The MODEMOFF bit in the same register directly controls the status of the MODEM_OFF_B output pin, but does not launch this task list).

Table 113. Modem Reset Triggers

Event	Conditions (all must be satisfied)
Modem Reset Request	SoC writes to the MODEMRSTSEQ bit in the MODEMCTRL register.

The Modem Reset task list toggles the Shutdown Warning (SDWN_B) and MODEM_OFF_B pins, implementing appropriate (modem-specific) delay timings. The default behavior for the Modem Reset task list is illustrated in the below diagram.

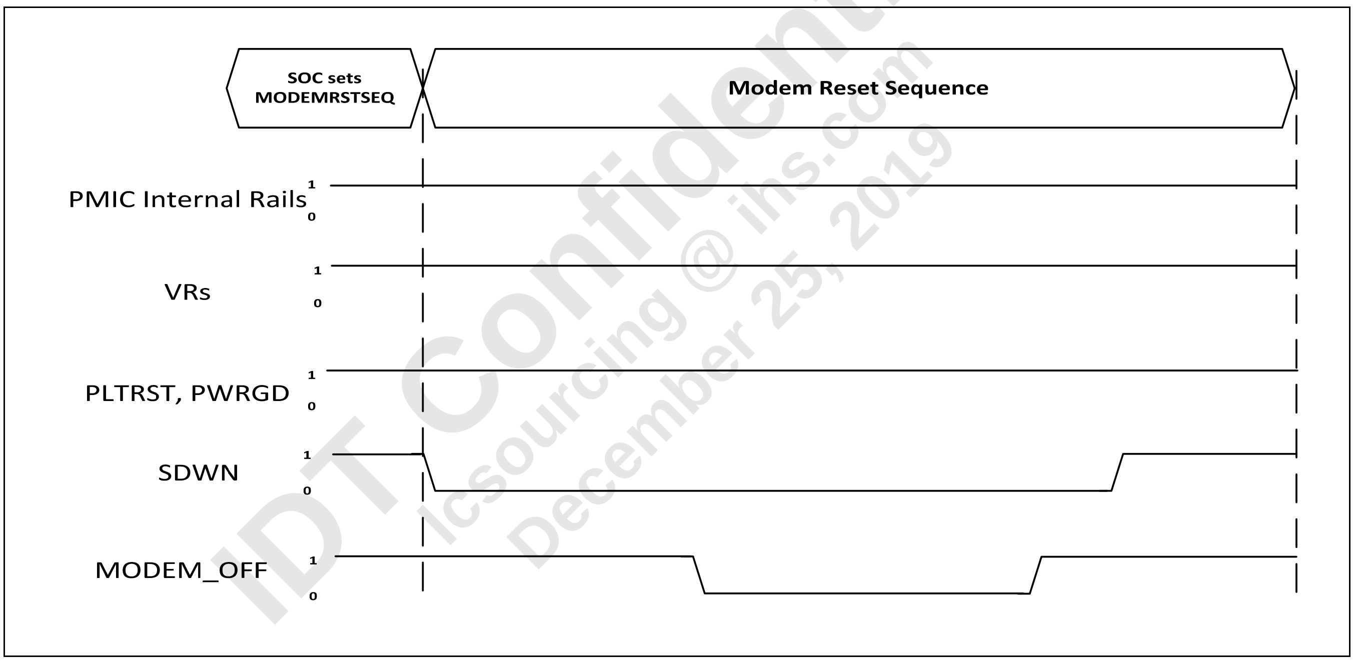


Figure 11. Modem Reset Sequence Timing Diagram

NOTES:

1. SDWN_B low to MODEM_OFF_B low delay time: 400-800µs.
2. MODEM_OFF_B low duration > 14ms.
3. MODEM_OFF_B high to SDWN_B high delay time > 5ms

PMIC Resets

The following table summarizes the reset sources for the PMIC.

Table 114. PMIC Reset Sources

Reset Source	Reset Trigger	Reset Type / Sequence
SoC Request	PLTRST_B	Warm Reset
External Button	PWRBTNIN_B held longer than the time defined in FLT[3:0]	Cold Off
Critical Event	PMICTEMP	Hard shutdown of all VR's, return to SoC G3 (not to wait for SLP_Sx from SoC).
	THERMTRIP	
Wake Event from Cold Off	PWRBTNIN_B pressed	Cold Boot

MODEMCTRL

The MODEMCTRL register can be written to by the SoC to manually control the MODEM_OFF_B pin, or to launch a Modem Reset task list.

Table 115: MODEMCTRL - Modem Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MODEMCTRL	R/W	RSVD						MODEM RSTSEQ	MODEM OFF	0x00	0x29

BIT	Name	Function	Default
D[7:2]	RSVD	Reserved	0
D[1]	MODEMRSTSEQ	This bit is self-clearing and always reads 0 0 = No action 1 = Initiate a Modem Reset task list	0
D[0]	MODEMOFF	Controls the state of the MODEM_OFF_B pin. 0 = MODEM_OFF_B driven to electrical low (asserted). 1 = MODEM_OFF_B driven to electrical high (de-asserted). If the MODEM_OFF_B pin state is modified by the task list processor's IO_CTL command, this bit updates to reflect the pin's current state.	1

NOTE:

1. A write must only set one bit. Action is taken immediately.

Reset Source Indicators

The PMIC contains two registers which are intended to store the cause of a shutdown or reset, for FW to interrogate on next startup. These registers are backed up by the backup battery so that on the next boot, software can determine the cause of the previous shutdown even if the battery was removed and replaced. These bits are write-1-to-clear.

If the RESETSRC registers are not cleared by the SoC, stale bits (from past resets) will auto-clear. This is to ensure that between RESETSRC0 and RESETSRC1, only the most recent reset reason is flagged for SW.

Table 116: Reset Source Register 0

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
RESETSRC0	R/W	RSYSTEMP2	RSYSTEMP1	RSYSTEMP0	RI2C	RSVD	RPWRBTN	RPMICTEMP	RTHERMTRIP	0x00	0x20

BIT	Name	Function	Default
D[7]	RSYSTEMP2	0 = Default 1 = Previous shutdown was due to an over-temperature condition on ADC channel 2.	0
D[6]	RSYSTEMP1	0 = Default 1 = Previous shutdown was due to an over-temperature condition on ADC channel 1.	0
D[5]	RSYSTEMP0	0 = Default 1 = Previous shutdown was due to an over-temperature condition on ADC channel 0.	0
D[4]	RI2C	0 = Default 1 = Previous shutdown was due to an I2C (SW) initiated reset.	0
D[3]	RSVD	Reserved	0
D[2]	RPWRBTN	0 = Default 1 = Previous shutdown was due to a Power Button initiated reset	0
D[1]	RPMICTEMP	0 = Default 1 = Previous shutdown was due to a PMIC internal over-temperature event. (PMIC sets this bit).	0
D[0]	RTHERMTRIP	0 = Default 1 = Previous shutdown was due to the SoC asserting THERMTRIP. (PMIC sets this bit).	0

Table 117: Reset Source Register 1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
RESETSRC1	R/W	RVSYS	ROV1	ROV0	RNORM	RCHG[1:0]		VCHG[1:0]		0x00	0x21

BIT	Name	Function	Default
D[7]	RVSYS	0 = Default 1 = Previous shutdown was due to the user removing VSYS during operation.	0
D[6]	ROV1	0 = Default 1 = Previous shutdown was due to an over-voltage condition on DCD1.	
D[5]	ROV0	0 = Default 1 = Previous shutdown was due to an over-voltage condition on DCD0.	
D[4]	RNORM	0 = Default 1 = Previous shutdown was due to a normal turn-off after SUSPWRDNOK.	
D[3:2]	VBAK_RCHG[1:0]	Coin cell charger series resistor setting: 00= 0.5kΩ. 10 = 2kΩ. 01= 1kΩ. 11= 5kΩ.	0x0

D[1:0]	VBAK_VCHG[1:0]	Coin cell charger output voltage setting: 00= Charger is turned-off. 10 = 3.0V. 01= 2.6V. 11= 3.3V.	0x0

Wake Source Indicator

The PMIC contains one registers that is intended to store the cause of a wake event, so that software can determine why the system was woken from Cold Off. These bits are write-1-to-clear.

If the WAKESRC register is not cleared by the SoC, stale bits (from past wakes) will auto-clear. This is to ensure that only the most recent wake reason is flagged for SW.

Table 118: Wake Source Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
WAKESRC	R/W	RSVD							WAKEPBTN	0X00	0x22

BIT	Name	Function	Default
D[7:1]	Reserved	Reserved	0
D[0]	WAKEPBTN	0 = Default 1 = Wake was triggered by user pressing the power button.	0

Interrupt Request (IRQ)

Interrupt request is an output signal generating interrupts to the SoC. It is pulled high when at least one unmasked interrupt bit is set in the 1st level interrupt register. It is valid when RSMRST_B=1 (de-asserted). The nominal voltage of IRQ is 1.8V when pulled high, 0V when pulled low. The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms.

Interrupting the SoC

When PMIC needs to interrupt the SoC it asserts the IRQ line. The following sequence illustrates the interrupt handling flow:

1. A PMIC event occurrence which sets 2nd level and 1st level (IRQLVL1) I²C register flags. In response to an unmasked flag being set in IRQLVL1, PMIC interrupts the SoC by asserting the IRQ line. This IRQ line is connected to an interruptible GPIO pin at SoC.
2. Because IRQ was set, SoC reads the 1st and 2nd level PMIC interrupt registers over I²C, determining the cause of the interrupt.
3. SoC clears the interrupt event in the PMIC via a register write to the 2nd level interrupt register over I²C.
4. If IRQLVL1 has all unmasked interrupts cleared, the PMIC de-asserts the IRQ signal, signaling that the interrupt has been handled.
5. The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms.

The PMIC may assert the IRQ line due to two separate events occurring simultaneously. It is the SoC’s responsibility to read all the interrupt registers and assign proper priority to handling the events.

Interrupt Request (IRQ) Control Unit

The interrupt control unit maintains the state of the First Level IRQ tree and is responsible for asserting and de-asserting the PMIC's IRQ to the application SoC. It contains status bits for interrupts from all the second-level sub-blocks as well as the Power Button.

Interrupt Descriptions

If unmasked, the second-level interrupts will propagate to the appropriate first-level interrupt bit, as assigned below. If the first-level interrupt is unmasked, it will propagate to the IRQ virtual pin, which will remain high as long as unmasked interrupts have not been cleared.

First-Level Interrupts (IRQLVL1)

The interrupt indicator to the Application Processor SoC, IRQ, is transmitted across the IRQ pin of the PMIC to a GPIO of the SoC. Causes of the interrupt are investigated by the SoC by reading the IRQ status registers over I2C. The PMIC interrupt scheme contains two levels. The first-level interrupt register contains 7 IRQ bits, and indicates which PMIC sub-block triggered the interrupt. One bit is dedicated to each of the interrupt-causing PMIC sub-blocks. For all units, the second-level interrupt registers indicate the specific interrupt triggers for each sub-block. A masking system is provided to enable or disable specific interrupt handlers.

If any bits are set in the first-level IRQ mask, the assertion of an interrupt from the masked sub-block(s) will not cause an assertion of the IRQ signal, nor will it set the associated first-level IRQ bit. By limiting the first-level IRQ bits set to only those that are unmasked, this disambiguates the dispatching of interrupts.

First-Level IRQ bits may not be directly cleared; they are cleared by clearing all unmasked second-level IRQ bits, than are implicitly cleared.

When all unmasked first-level IRQ bits are implicitly cleared (all unmasked second-level interrupts directly cleared), the IRQ pin is de-asserted.

Table 119: IRQLVL1 – Level 1 Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
IRQLVL1	R/W	RSVD	VR	GPIO	RSVD	ADC	RSVD	THRM	RSVD	0x00	0x02

BIT	Name	Function	Default
D7	RSVD	RSVD	0
D6	VR	0 = VR IRQ not asserted 1 = VR IRQ asserted – Write ‘1’ to clear	0
D5	GPIO	0 = GPIO IRQ not asserted 1 = GPIO IRQ asserted – Write ‘1’ to clear	0
D4	RSVD	RSVD	0
D3	ADC	0 = ADC IRQ not asserted 1 = ADC IRQ asserted – Write ‘1’ to clear	0
D2	RSVD	RSVD	
D1	THRM	0 = THRM (Thermal Unit) IRQ not asserted 1 = THRM (Thermal Unit) IRQ asserted – Write ‘1’ to clear	0
D0	RSVD	RSVD	0

Table 120: IRQLVL1MSK – Level 1 Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MIRQLVL1	R/W	RSVD	MVR	MGPIO	RSVD	MADC	RSVD	MTHRM	RSVD	0x6A	0x0E

BIT	Name	Function	Default
D7	RSVD	RSVD	0
D6	MVR	0 = VR IRQ unmasked 1 = VR IRQ masked	1
D5	MGPIO	0 = GPIO IRQ unmasked 1 = GPIO IRQ masked	1
D4	RSVD	RSVD	0
D3	MADC	0 = ADC IRQ unmasked 1 = ADC IRQ masked	1
D2	RSVD	RSVD	0
D1	MTHRM	0 = THRM (Thermal Unit) IRQ unmasked 1 = THRM (Thermal Unit) IRQ masked	1
D0	RSVD	RSVD	0

Second-Level Interrupts

While First-Level Interrupt bits inform the interrupt handler of which sub-block interrupted, Second-Level Interrupt registers/bits provide the interrupt handler with the specific nature of the block's interrupt event.

If any bits are set in a second-level interrupt mask, then the appropriate second level interrupt bit is prevented from asserting the first level interrupt bit for the corresponding sub-block, nor will the bit become set. (Only unmasked 2nd level interrupt bits may be set).

Interrupt bits are write-1-to-clear. This includes all second-level interrupt register locations and the power-button interrupt bit. The IRQ signal will not be de-asserted until all unmasked interrupt bits are cleared.

Table 121: Second Level Interrupts

INT Name	Register	Source	First-Level Interrupt	Related Status Bit	DESCRIPTION
VSYS	VSYSIRQ	ADC	ADC		This indicates that a VSYS is out of range ("invalid").
VRFAULT	VRIRQ	ADC	VR		This indicates that a VR overvoltage or over current fault has occurred. The VR fault interrupt will reset to 0 on Cold Off.
PMICALRT	THRMIRQ	Thermal Control Unit	THRM		Set by the thermal state machine when a PMIC die temperature thermal alert occurs

INT Name	Register	Source	First-Level Interrupt	Related Status Bit	DESCRIPTION
ADC2ALRT	ADCIRQ	ADC	ADC		Set by the thermal state machine when a system voltage 2 alert occurs
ADC1ALRT	ADCIRQ	ADC	ADC		Set by the thermal state machine when a system voltage 1 alert occurs
ADC0ALRT	ADCIRQ	ADC	ADC		Set by the thermal state machine when a system voltage 0 alert occurs
SYSTEMP	ADCIRQ	ADC	ADC		Bit is set when a SYSTEMP conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made).
GPIO	GPIOIRQ	GPIO	GPIO	DIN	Each GPIO pin can be configured as input with programmable interrupt edge for rise, fall or both. See GPIOCTLI registers for INTCNT settings. Triggered when the conditions set in GPIOCTLI registers have been met. The status of the GPIO input can be verified by reading the DIN bit from the GPIOCTLI register.

GPIO IRQ Registers

Table 122: GPIO0 Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIO0IRQ	R/W	RSVD	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	0x00	0x0B

BIT	NAME	FUNCTION	DEFAULT
D[7]	RSVD	RSVD	0
D[6]	GPIO14	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[5]	GPIO13	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[4]	GPIO12	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[3]	GPIO11	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[2]	GPIO10	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[1]	GPIO9	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[0]	GPIO8	0 = No Interrupt Pending 1 = Interrupt Pending	0

Table 123: GPIO1 Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPIO1IRQ	R/W	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	0x00	0x0C

BIT	NAME	FUNCTION	DEFAULT
D[7]	GPIO7	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[6]	GPIO6	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[5]	GPIO5	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[4]	GPIO4	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[3]	GPIO3	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[2]	GPIO2	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[1]	GPIO1	0 = No Interrupt Pending 1 = Interrupt Pending	0
D[0]	GPIO0	0 = No Interrupt Pending 1 = Interrupt Pending	0

Table 124: GPIO0 Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MGPIO0IRQ	R/W	RSVD	MGPIO14	MGPIO13	MGPIO12	MGPIO11	MGPIO10	MGPIO9	MGPIO8	0x7F	0x19

BIT	NAME	FUNCTION	DEFAULT
D[7]	RSVD	RSVD	0
D[6]	MGPIO14	0 = No Mask 1 = Mask Interrupt	1
D[5]	MGPIO13	0 = No Mask 1 = Mask Interrupt	1
D[4]	MGPIO12	0 = No Mask 1 = Mask Interrupt	1
D[3]	MGPIO11	0 = No Mask 1 = Mask Interrupt	1
D[2]	MGPIO10	0 = No Mask 1 = Mask Interrupt	1

D[1]	MGPIO9	0 = No Mask 1 = Mask Interrupt	1
D[0]	MGPIO8	0 = No Mask 1 = Mask Interrupt	1

Table 125: GPIO1 Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MGPIO1IRQ	R/W	MGPIO7	MGPIO6	MGPIO5	MGPIO4	MGPIO3	MGPIO2	MGPIO1	MGPIO0	0xFF	0x1A

BIT	NAME	FUNCTION	DEFAULT
D[7]	MGPIO7	0 = No Mask 1 = Mask Interrupt	1
D[6]	MGPIO6	0 = No Mask 1 = Mask Interrupt	1
D[5]	MGPIO5	0 = No Mask 1 = Mask Interrupt	1
D[4]	MGPIO4	0 = No Mask 1 = Mask Interrupt	1
D[3]	MGPIO3	0 = No Mask 1 = Mask Interrupt	1
D[2]	MGPIO2	0 = No Mask 1 = Mask Interrupt	1
D[1]	MGPIO1	0 = No Mask 1 = Mask Interrupt	1
D[0]	MGPIO0	0 = No Mask 1 = Mask Interrupt	1

General Purpose ADC (GPADC)

The general purpose ADC (referred to as GPADC or ADC) is used for die temperature, current, and voltage measurements. It is managed at a hardware level by ADC state machine, similar to how rail transitions sequences are handled. The state machine performs ADC operations (regular readings of the die temperature, currents and voltages, programmed in registers) and may be modified by the SoC after boot and initialization. The state machine for the GPADC is distinct from any other state machine (such as the one for power sequence controlling boot flow). This prevents the management of lengthy ADC transactions from blocking time-critical power sequencing tasks.

The GPADC shall be able to perform the following task lists:

- Repeated (on-going) VR current acquisition (initiated via timer define VRIMONCTL)
- SoC-requested die temperature acquisition (initiated via GPADCREQ)
- SoC-requested VR current acquisition (initiated via GPADCREQ)
- SoC-requested voltage measurements on ADC[2:0] inputs

The figure below illustrates the interaction between the I²C control registers, ADC state machine, SRAM, and ADC hardware to perform temperature monitoring and GPADC acquisition.

GPADC Read Requests

The SoC may manually add GPADC read requests to the ADC queue whenever there is free instruction space in the queue and the BUSY bit in the GPADCREQ register is cleared. Manual GPADC requests are initiated by setting the appropriate bit in the GPADCREQ register. In response to this bit being set, the corresponding tasks are performed in the ADC.

When the queue fills, the BUSY bit is set, and the SoC may not trigger any additional ADC task lists until the queue has room. The PMIC hardware enforces that no additional commands are written by ignoring any requests from the SoC.

If the SoC sets the "IRQEN" bit in the GPADCREQ register, the PMIC will interrupt the SoC when the requested ADC task list is complete (via the ADCIRQ register).

The GPADCREQ register is defined below.

Table 126: GPADC Conversion Request Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
GPADCREQ	R/W	VSYS	VRI	RSVD	RSVD	ADC	RSVD	IRQEN	BUSY	0x00	0x72

BIT	Name	Function	Default
D[7]	VSYS	Set for capturing VSYS. Bit automatically clears after it is set.	0
D[6]	VRI	Set for capturing VR current of all 5 VR current channels. Bit automatically clears after it is set.	0
D[5]	RSVD	RSVD	0
D[4]	RSVD	RSVD	0
D[3]	ADC	Set for capturing ADC0, ADC1, and ADC2. Bit automatically clears after it is set	0

D[2]	RSVD	RSVD	0
D[1]	IRQEN	If this bit is set, the GPADC conversion requested generates a SoC interrupt when complete. Bit automatically clears after it is set.	0
D[0]	BUSY	The GPADC state machine sets this read-only bit when there is no more room in the ADC instruction queue. Software should check that this bit is clear before setting GPADCREQ[5:1]. GPADC requests issued while BUSY=1 will be ignored.	0

Table 127: GPADC Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
ADCIRQ	R/W	VSYS	VRI	RSVD	RSVD	ADC	RSVD			0x00	0x08

BIT	Name	Function	Default
D[7]	VSYS	Bit is set when a VSYS conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made). Bit is cleared by writing a '1'.	0
D[6]	VRI	Bit is set when a VRI conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made). Bit is cleared by writing a '1'.	0
D[5:4]	RSVD	Reserved	00
D[3]	ADC	Bit is set when a ADC conversion completes (and the GPADCREQ:IRQEN bit was set when the request was made). Bit is cleared by writing a '1'.	0
D[2:0]	RSVD	Reserved	000

Table 128: GPADC Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MADCIRQ	R/W	MVSYS	MVRI	RSVD	RSVD	MADC	RSVD			0xC8	0x15

BIT	Name	Function	Default
D[7]	MVSYS	0 = No Mask 1 = Interrupt Masked	1
D[6]	MVRI	0 = No Mask 1 = Interrupt Masked	1
D[5:4]	RSVD	Reserved.	00
D[3]	MADC	0 = No Mask 1 = Interrupt Masked	1
D[2:0]	RSVD	Reserved	000

When a GPADC conversion is performed, results are stored in a series of registers which are dedicated to specific channels. (*RSLT registers). These result registers are detailed below.

Table 129: THRMRSLTH – Thermal Result Register High (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMRSLTH	R	RSVD						DIETEMP[9:8]		0x00	0x7E

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved.	000000
D[1:0]	DIETEMP[9:8]	Upper 2 bits of the temperature result for PMIC die temperature (DIETEMP).	00

Table 130: THRMRSLTL – Thermal Result Register Low (LSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMRSLTL	R	DIETEMP[7:0]								0x00	0x7F

Bit	Name	Function	Default
D[7:0]	DIETEMP[7:0]	Lower 8 bits of the temperature result for PMIC die temperature (DIETEMP).	00000000

The actual die temperature of the PMIC calculates as follows:

$$T_J = DIETEMP[9:0] \times 180/143 - 154.55 \text{ (in °C)}$$

Table 131: VSYSRSLTH – VSYS Result Register High (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VSYSRSLTH	R	RSVD						VSYS[9:8]		0x00	0x80

Bit	Name	Function	Default
D[7:2]	RSVD	Reserved.	000000
D[1:0]	VSYS[9:8]	Upper 2 bits of the ADC result for VSYS voltage.	00

Table 132: VSYSRSLTL – VSYS Result Register Low (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VSYSRSLTL	R	VSYS[7:0]								0x00	0x81

Bit	Name	Function	Default
D[7:0]	VSYS[7:0]	Low 8 bits of the ADC result for VSYS voltage.	00000000

VR Current Monitoring

The PMIC monitors DCD0, 1, 2, 5, 6 switching regulator output currents, and the corresponding I2C and SVID registers for current reading is shown below.

Table 133: Voltage Rails and Corresponding Result Register

VOLTAGE RAILS	I2C REGISTER		SVID RAILS ADDRESS	SVID REGISTER
	IOUT_H	IOUT_L		IOUT (H)
DCD0	0x84	0x85	SVID_ID_DCD0	0x15
DCD1	0x86	0x87	SVID_ID_DCD1	0x15
DCD2	0x8C	0x8D	SVID_ID_DCD2	0x15
DCD5	0x88	0x89	N/A	N/A
DCD6	0x8A	0x8B	N/A	N/A

Table 134: IOUT_H – Current Result Register High (MSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
IOUT_H	R	IOUT[9:2]								0x00	See Table 133

Bit	Name	Function	Default
D[7:0]	IOUT[9:2]	Upper 8 bits of the current result for DCDx (IOUT).	00000000

Table 135: IOUT_L – Current Result Register Low (LSB)

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
IOUT_L	R	RSVD						IOUT[1:0]		0x00	See Table 133

Bit	Name	Function	Default
D[1:0]	IOUT[1:0]	Lower 2 bits of the current result for DCDx (IOUT). Always read 0b00	00

Normally, the above regulators are monitored in S0 state. The output current is averaged and measured every 1ms (default). To provide flexibility, a control register is defined below to let the user enable/disable this function and set the measurement frequency.

Table 136: VR Current Monitor Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
VRIMONCTL	R/W	RSVD		MODE	VRIFRQS[1:0]		VRIFRQA[1:0]		VRIM EN	0x2B	0x71

BIT	Name	Function	Default
D[7:6]	RSVD	Reserved	00
D[5]	MODE	Resets the two thermal monitoring timers based on the durations specified in VRIFRQS/VRIFRQA. 0 = Active Mode. VRIFRQA durations used. 1 = Standby Mode. VRIFRQS durations used	1
D[4:3]	VRIFRQS[1:0]	Specifies the frequency at which VR current measurements are initiated while in standby mode (MODE=1). Values: 00 = Disabled 01 = 1ms (Default) 10 = 5ms 11 = 10ms	01
D[2:1]	VRIFRQA[1:0]	Specifies the frequency at which VR current measurements are initiated while in active mode (MODE=0). Values: 00 = 0.25s 01 = 0.5ms (Default) 10 = 1ms 11 = 3ms	01
D[0]	VRIMEN	Setting this bit enables ADC-based current monitoring timers. Current monitoring timers are reset when this bit is set to 1.	1

The result registers for VR current measurements can be defined in a similar way as the other result registers in previous section. They are listed in the GPADC register requirements table.

Thermal Monitoring

The PMIC is capable of monitoring the PMIC die temperature, via an internal temperature measurement circuit.

The THRMCTL register is the master control for the timer-based thermal monitoring state machine. It is defined in the table below.

Table 137: Thermal Monitor Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMMONCTL	R/W	RSVD			MODE	TEMPFRQS	TEMPFRQA[1:0]		THRM EN	0x15	0x8E

BIT	Name	Function	Default
D[7:5]	RSVD	Reserved	
D[4]	MODE	Resets the two thermal monitoring timers based on the durations specified in TEMPFRQS/TEMPFRQA. 0 = Active Mode. TEMPFRQA durations used. 1 = Standby Mode. TEMPFRQS durations used	1
D[3]	TEMPFRQS	Specifies the frequency at which die temperature measurements are initiated while in standby mode (MODE=1). Values: 0 = Disabled (Default) 1 = 30s	0
D[2:1]	TEMPFRQA[1:0]	Specifies the frequency at which die temperature measurements are initiated while in active mode (MODE=0). Values: 00 = Disabled 01 = 5s 10 = 10s (Default) 11 = 30s	10
D[0]	THRMEN	Setting this bit enables ADC-based thermal monitoring timers. Thermal monitoring timers are reset when this bit is set to 1. The PMIC must still shut down the PMIC if die temperature exceeds its critical limit when this bit is set to 0.	1

Thermal Alerts

The PMIC supports the ability to configure a die temperature threshold which, when crossed (in either direction with configurable hysteresis), will launch an interrupt to the SoC.

The thresholds are stored as 10-bit count values, to be compared directly against GPADC readings. When a temperature result ADC count captured by the GPADC in a given set of THRMRSLT registers drops below the count specified by the corresponding THRMALRT registers for that sensor, a thermal alert is triggered signifying that the threshold has been crossed and that the temperature has risen into the alert zone. Similarly, when the THRMRSLT register rises above the threshold in THRMALRT (plus an optional hysteresis count specified in THRMALRT), a thermal alert is triggered, signifying that the temperature has dropped out of the alert zone.

Table 138: PMIC Die Temperature Threshold Register High

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DIE_THRMALRTH	R/W	P_EN	EN	DIETEMP_HYS[4:1]				DIETEMP_ALRT[9:8]		0xE4	0xAF

BIT	Name	Function	Default
D[7]	P_EN	Die Temperature Policy Action Enable - When set, any crossover of the die temperature must assert PROCHOT_B and any cross down below DIETEMP_HYST must de-assert PROCHOT_B	1
D[6]	EN	Die Measurement Enable 1 = Enable, 0 = Disabled	1
D[5:2]	DIETEMP_HYS[3:0]	Hysteresis value for die temperature.	1001
D[1:0]	DIETEMP_ALRT[9:8]	Upper 2 bits of the temperature alert threshold for the die temperature.	00

Table 139: PMIC Die Temperature Threshold Register Low

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
DIE_THRMALRTL	R/W	DIETEMP_ALRT[7:0]								0xE6	0xB0

BIT	Name	Function	Default
D[7:0]	DIETEMP_ALRT[7:0]	Lower 8 bits of the temperature alert threshold for die temperature.	11100110

In addition to prescribing the ADC threshold for triggering an alert, the THRMALRTH register also includes a 4-bit field, HYS[3:0], which defines hysteresis for the thermal alert. A hysteresis value is used to avoid spurious interrupt assertions when temperatures hover near the alert threshold. Example:

- When DIETEMP[9:0] drops to be equal to or lesser than DIETEMP_ALRT[9:0], a thermal interrupt is generated via the THRMIRQ register. Bit[3] is set in the THRMSTAT status register, indicating that the die temperature is currently in a thermal alert condition.
- After having initiated an alert, when/if DIETEMP[9:0] rises to be equal to or greater than DIETEMP_ALRT + DIETEMP_HYS, an interrupt is generated via the THRMIRQ register indicating that the thermal alert condition is exited. The Bit[3] bit in the THRMSTAT register is cleared, allowing it to be set again.

When a thermal event is triggered for a particular sensor, the PMIC takes the following actions:

- Sets the appropriate bit in the 2nd level thermal interrupt register (THRMIRQ)
- Setting this bit, in turn, sets the 1st level interrupt bit, triggering an interrupt to the SoC over the INT pin.
- Sets or clears (depending on ADC count) the appropriate status register in the THRMSTAT status register.

The second level interrupt register for the thermal monitoring state machine, THRMIRQ, is defined below.

Table 140: Thermal Monitor Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
THRMIRQ	R/W	RSVD				PMICALRT	ADC2ALRT	ADC1ALRT	ADC0ALRT	0x00	0x04

BIT	Name	Function	Default
D[7:4]	RSVD	Reserved	0000
D[3]	PMICALRT	Set by the thermal state machine when a PMIC die temperature thermal alert occurs	0
D[2]	ADC2ALRT	Set by the state machine when an ADC2 temperature thermal alert occurs	0
D[1]	ADC1ALRT	Set by the state machine when an ADC1 temperature thermal alert occurs	0
D[0]	ADC0ALRT	Set by the state machine when an ADC0 temperature thermal alert occurs	0

Table 141: Thermal Monitor Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
MTHRMIRQ	R/W	RSVD				MPMICALRT	MADC2ALRT	MADC1ALRT	MADC0ALRT	0x0F	0x11

BIT	Name	Function	Default
D[7:4]	RSVD	Reserved	0000
D[3]	MPMICALRT	Set by the thermal state machine when a PMIC die temperature thermal alert occurs	1
D[2]	MADC2ALRT	Set by the state machine when an ADC2 temperature thermal alert occurs	1
D[1]	MADC1ALRT	Set by the state machine when an ADC1 temperature thermal alert occurs	1
D[0]	MADC0ALRT	Set by the state machine when an ADC0 temperature thermal alert occurs	1

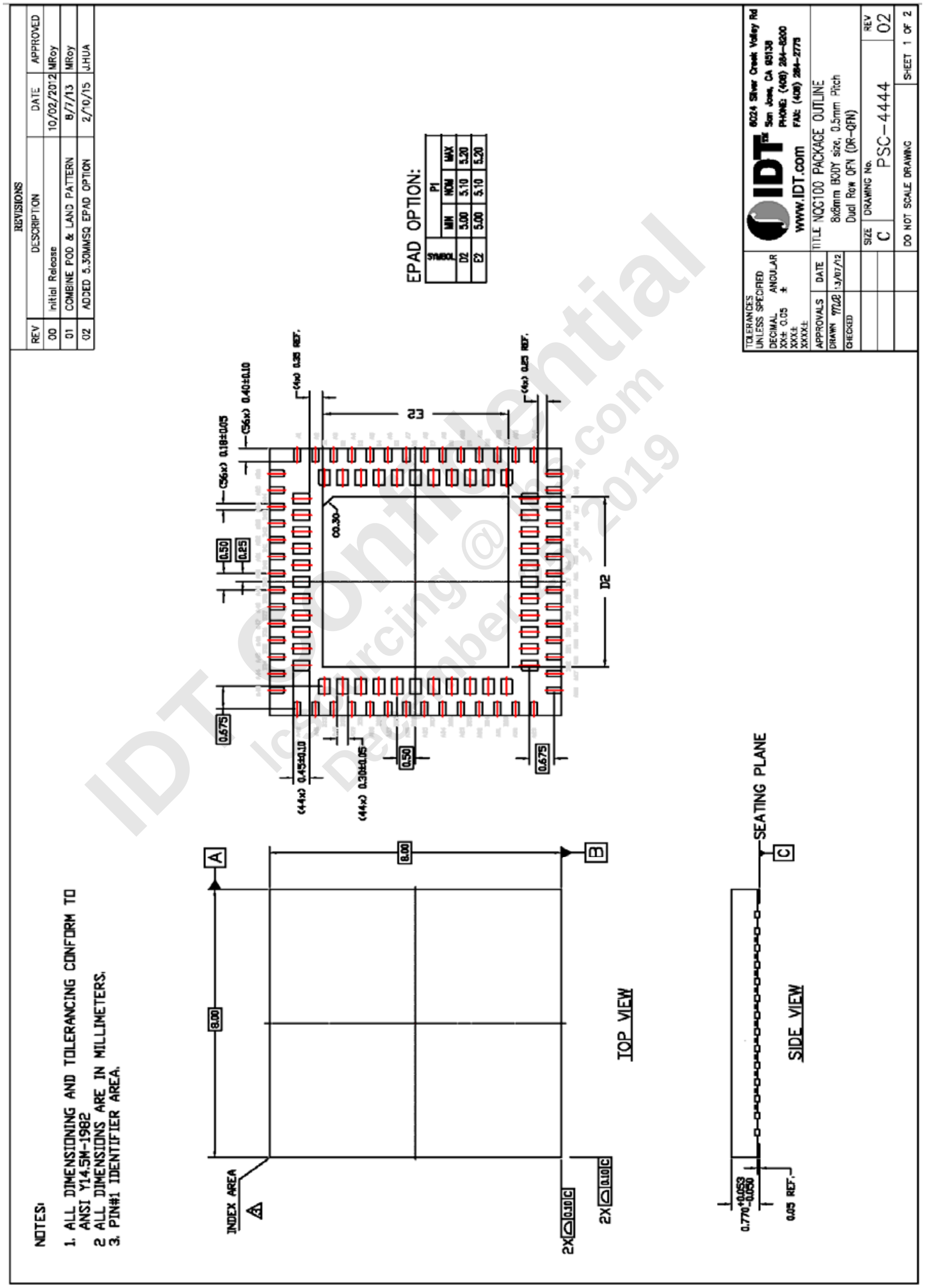
The thermal interrupt status register, THRMSTAT, is defined below. If an alert condition is removed, the status bit will clear. However, the interrupt generated (in the 2nd level interrupt register, THRMIRQ) will persist until cleared by the SoC.

Table 142: Thermal Monitor Status Register

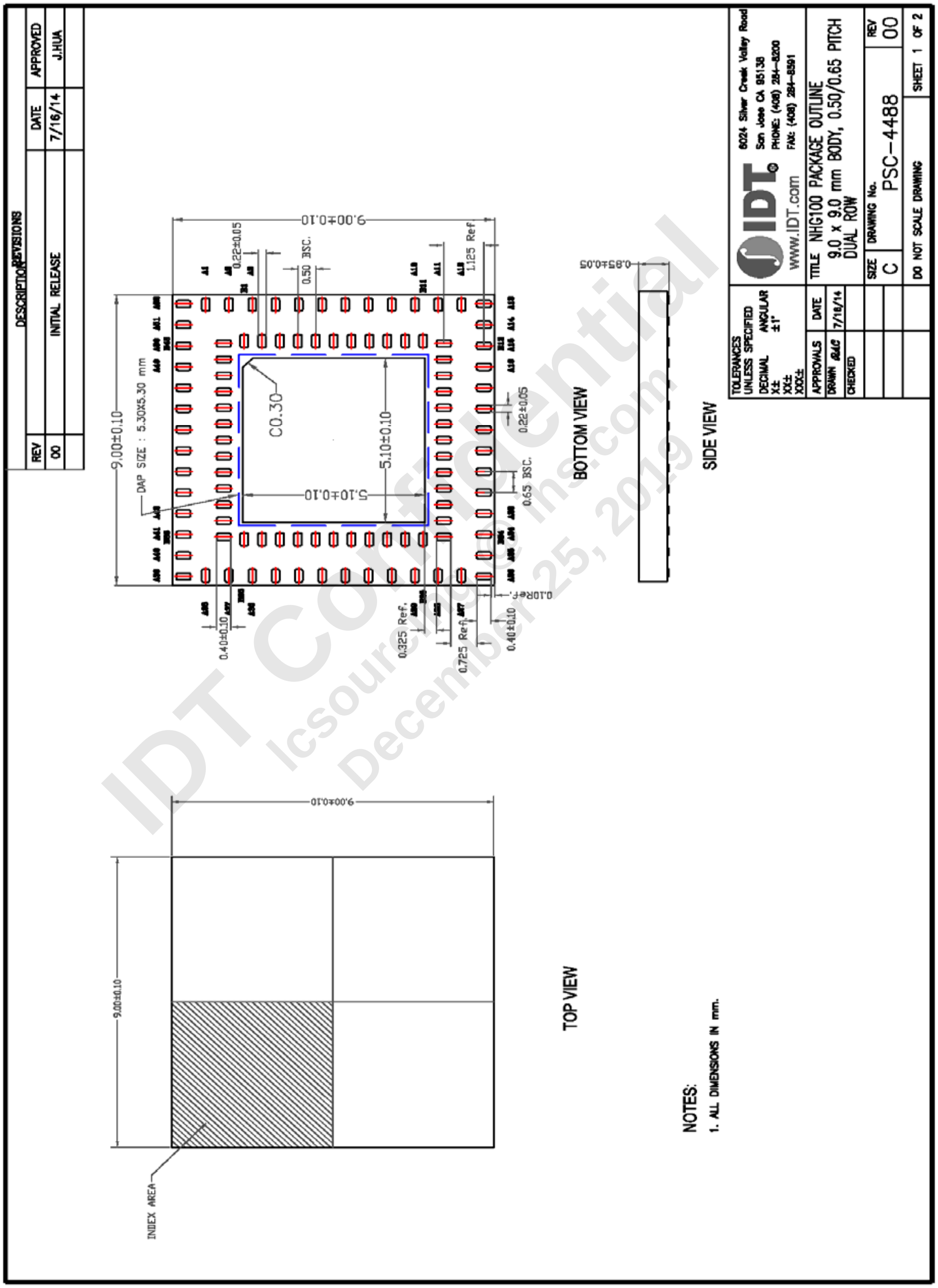
Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Address
STHRMIRQ	R/W	RSVD				SPMICALRT	SADC2ALRT	SADC1ALRT	SADC0ALRT	0x00	0x05

BIT	Name	Function	Default
D[7:4]	RSVD	Reserved	0000
D[3]	SPMICALRT	Set by the thermal state machine when a PMIC die temperature thermal alert is occurring.	0
D[2]	SADC2ALRT	Set by the state machine when an ADC2 temperature thermal alert is occurring.	0
D[1]	SADC1ALRT	Set by the state machine when an ADC1 temperature thermal alert is occurring.	0
D[0]	SADC0ALRT	Set by the state machine when an ADC0 temperature thermal alert is occurring.	0

PACKAGE OUTLINE: QFN (NQG)



PACKAGE OUTLINE: GQFN (NHG)



ORDERING GUIDE

Table 143. Ordering Summary

PART NUMBER[1]	MARKING[1]	PACKAGE[2]	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9180A-xxNQGI	P9180A-xxNQGI	NQG100	-40°C to +85°C	Tray	260
P9180A-xxNQGI8	P9180A-xxNQGI	NQG100; T&R	-40°C to +85°C	Tape and Reel	3,000
P9180A-xxNHGI	P9180A-xxNHGI	NHG100	-40°C to +85°C	Tray	207
P9180A-xxNHGI8	P9180A-xxNHGI	NHG100; T&R	-40°C to +85°C	Tape and Reel	3,000

1 The –xx part number suffix identifies the device configuration. Please refer to the P9180A configuration addendum or contact IDT for additional information.

2 NQG100: 100ld-8x8 DR-QFN, Please refer to http://www.idt.com/package/nqg100 for package information.
NHG100: 100ld-9x9 DR-GQFN, Please refer to http://www.idt.com/package/nhg100 for package information.

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