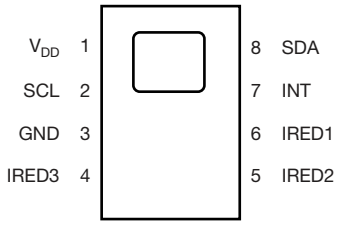
High Resolution Digital Proximity Sensor With I²C Interface



LINKS TO ADDITIONAL RESOURCES

3D Models | Design Tools | Technical Notes

DESCRIPTION

VCNL3036X01 integrates a proximity sensor (PS), a mux, and a driver for up to 3 external IREDs into one small package. It incorporates photodiodes, amplifiers, and analog to digital converting circuits into a single chip by CMOS process. PS programmable interrupt features of individual high and low thresholds offers the best utilization of resource and power saving on the microcontroller.

FEATURES

- Package type: surface-mount
- Dimensions (L x W x H in mm): 4.0 x 2.36 x 0.75
- AEC-Q101 qualified
- Integrated modules: proximity sensor (PS) and signal conditioning IC
- Temperature compensation: -40 °C to +105 °C
- Low power consumption I²C (SMBus compatible) interface
- Output type: I²C bus
- Operation voltage: 2.5 V to 3.6 V
- Floor life: 168 h, MSL 3, according to J-STD-020
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE

GREEN (5-2008)

PROXIMITY FUNCTION

- Programmable IRED sink current
- Intelligent cancellation to reduce cross talk phenomenon
- Smart persistence scheme to reduce PS response time
- Selectable for 12-bit / 16-bit PS output data

INTERRUPT

- Programmable interrupt function for PS with upper and lower thresholds
- Adjustable persistence to prevent false triggers for PS

APPLICATIONS

- Force feedback applications
- Proximity / optical switch for consumer, computing, automotive, and industrial devices

PRODUCT SUMMARY

PART NUMBER	OPERATING RANGE (1) (mm)	OPERATING VOLTAGE RANGE (V)	I²C BUS VOLTAGE RANGE (V)	IRED PULSE CURRENT (2) (mA)	SPECTRAL BANDWIDTH RANGE $\lambda_{0.5}$ (nm)	OUTPUT CODE	ADC RESOLUTION PROXIMITY / AMBIENT LIGHT
VCNL3036X01	0 to 500	2.5 to 3.6	1.8 to 5.5	200	500 to 910	16 bit, I²C	16 bit / -

Notes

(1) Part should be operated in dark condition (not in direct sunlight)

(2) Adjustable through I²C interface

ORDERING INFORMATION

ORDERING CODE	PACKAGING	VOLUME (1)	REMARKS
VCNL3036X01-GS08	Tape and reel	MOQ: 3300 pcs	4.0 mm x 2.36 mm x 0.75 mm
VCNL3036X01-GS18		MOQ: 13 000 pcs	

Note

(1) MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)					
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Supply voltage		V_{DD}	2.5	3.6	V
Operation temperature range		T_{amb}	-40	+105	°C
Storage temperature range		T_{stg}	-40	+110	°C

RECOMMENDED OPERATING CONDITIONS (T_{amb} = 25 °C, unless otherwise specified)					
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Supply voltage		V_{DD}	2.5	3.6	V
Operation temperature range		T_{amb}	-40	+105	°C
I^2C bus operating frequency		$f_{(I2CCLK)}$	10	400	kHz

PIN DESCRIPTIONS			
PIN ASSIGNMENT	**SYMBOL**	**TYPE**	**FUNCTION**
1	V_{DD}	-	Power supply input
2	SCL	I	I^2C digital bus clock input
3	GND	-	Ground
4	IRED3	I	Cathode (IRED3) connection
5	IRED2	I	Cathode (IRED2) connection
6	IRED1	I	Cathode (IRED1) connection
7	INT	O	Interrupt pin
8	SDA	I / O (open drain)	I^2C data bus data input / output

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER		**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Supply voltage			V_{DD}	2.5	-	3.6	V
Supply current		Excluded LED driving	I_{DD}	-	300	-	µA
		Light condition = dark, V_{DD} = 3.3 V	I_{DD} (SD)	-	0.2	-	µA
I^2C supply voltage			$V_{PULL\ UP}$	1.8	-	5.5	V
PS enable			I_{PSSD}	-	200	-	µA
I^2C signal input	Logic high	V_{DD} = 3.3 V	V_{IH}	1.55	-	-	V
	Logic low		V_{IL}	-	-	0.4	
	Logic high	V_{DD} = 2.6 V	V_{IH}	1.4	-	-	V
	Logic low		V_{IL}	-	-	0.4	
Full PS counts		12-bit / 16-bit resolution		-	-	4096 / 65 535	steps
PS detection range		Kodak gray card (1)(2)		0	-	500	mm
Operating temperature range			T_{amb}	-40	-	+105	°C
LED anode voltage				-	-	5.5	V
IRED driving current				-	-	200	mA

Notes

(1) Depending on external IRED

(2) Part should be operated in dark condition (not in direct sunlight)

I²C BUS TIMING CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**SYMBOL**	**STANDARD MODE**		**FAST MODE**		**UNIT**
		MIN.	**MAX.**	**MIN.**	**MAX.**	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	µs
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	µs
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	µs
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	µs
Data hold time	$t_{(HDDAT)}$	-	3450	-	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I²C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	µs
I²C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	µs
Clock / data fall time	$t_{(F)}$	-	300	-	300	ns
Clock / data rise time	$t_{(R)}$	-	1000	-	300	ns

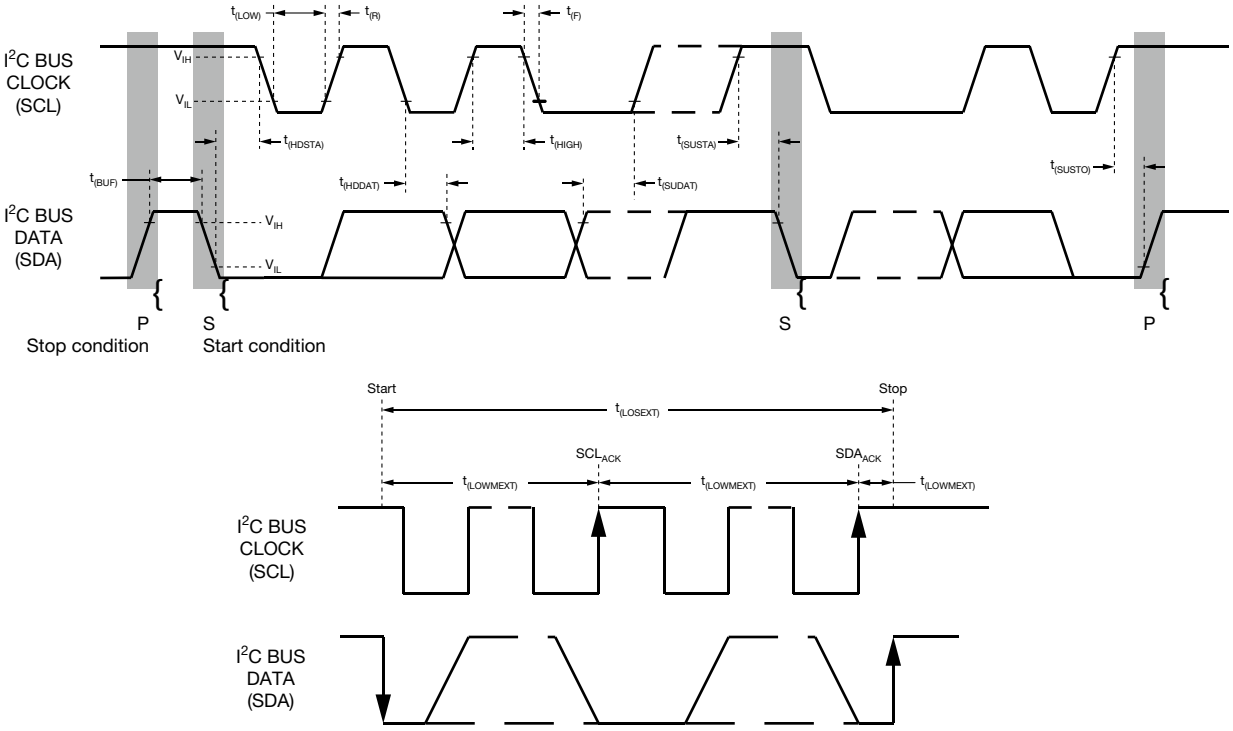


Fig. 1 - I²C Bus Timing Diagram

PARAMETER TIMING INFORMATION

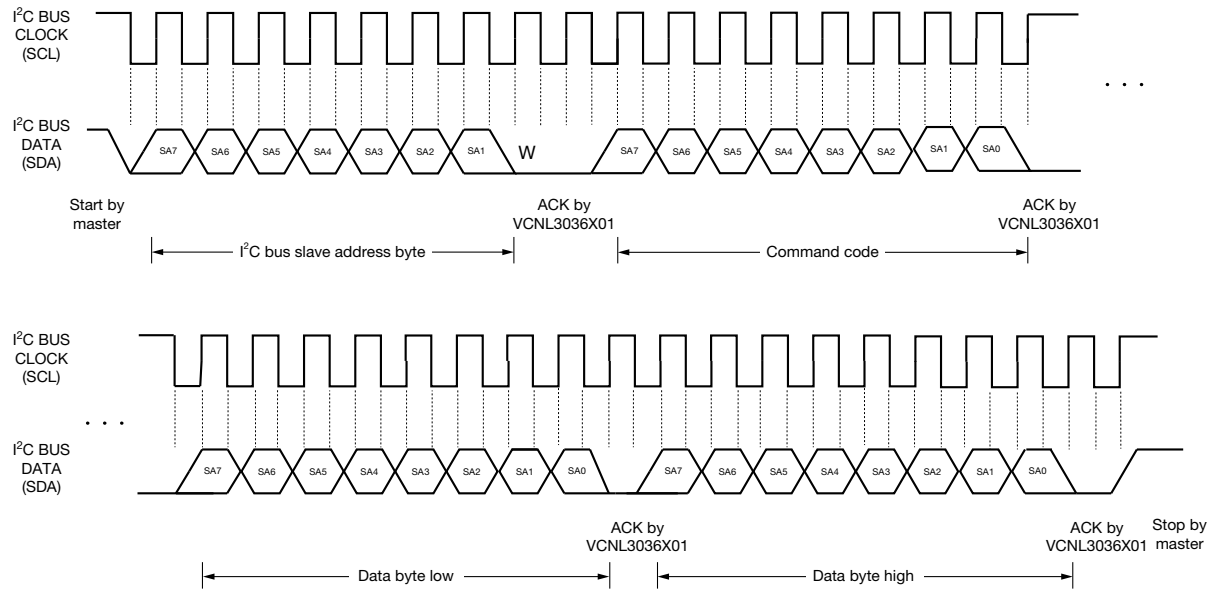


Fig. 2 - I²C Bus Timing for Sending Word Command Format

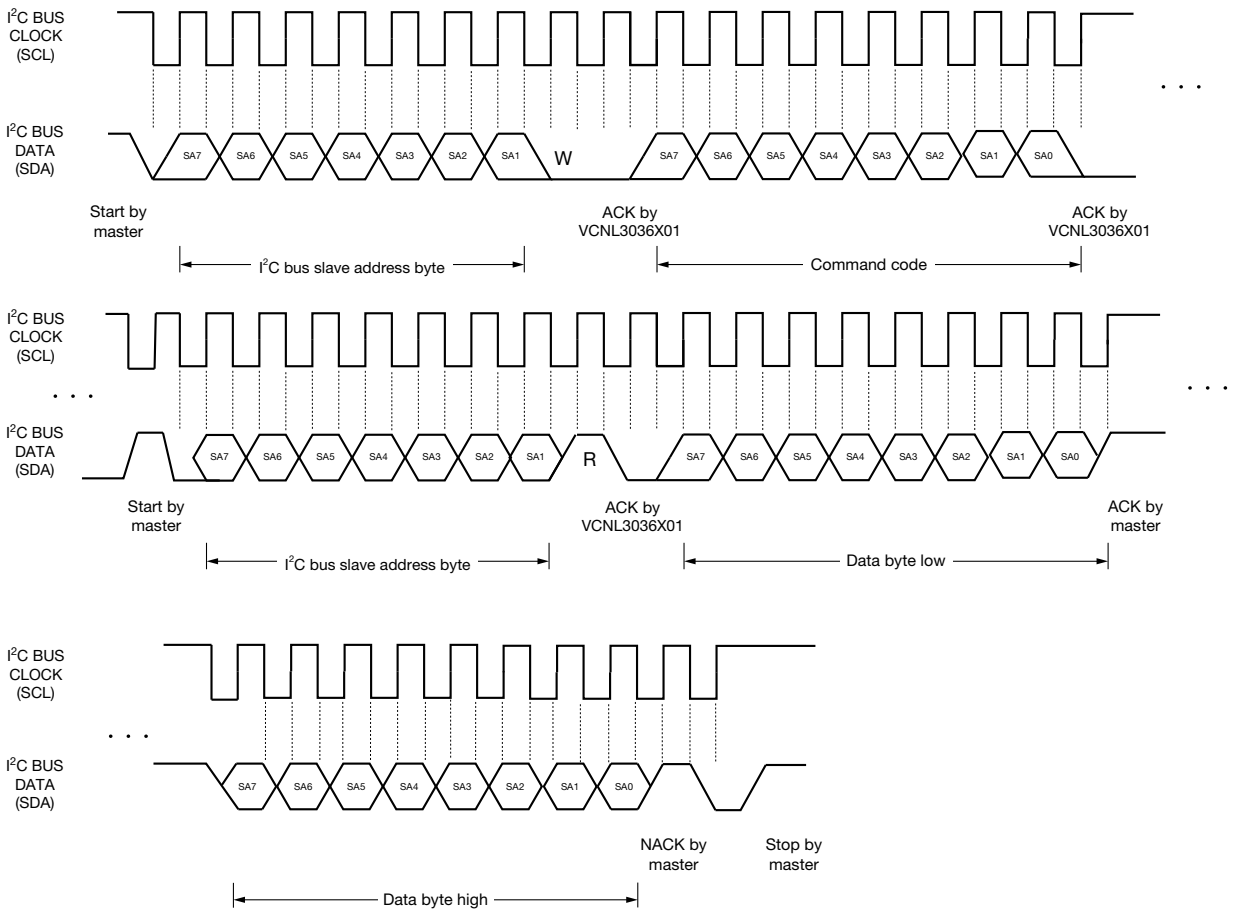


Fig. 3 - I²C Bus Timing for Receiving Word Command Format

TYPICAL PERFORMANCE CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

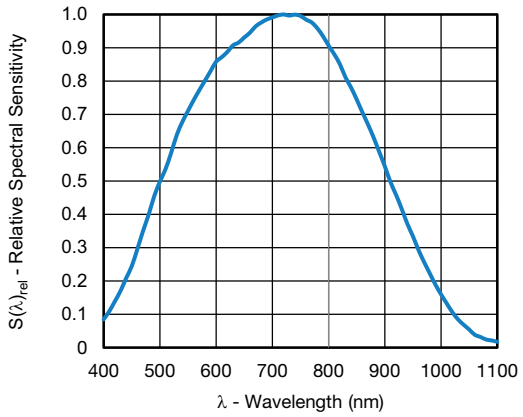


Fig. 4 - Relative Spectral Sensitivity vs. Wavelength (proximity sensor)

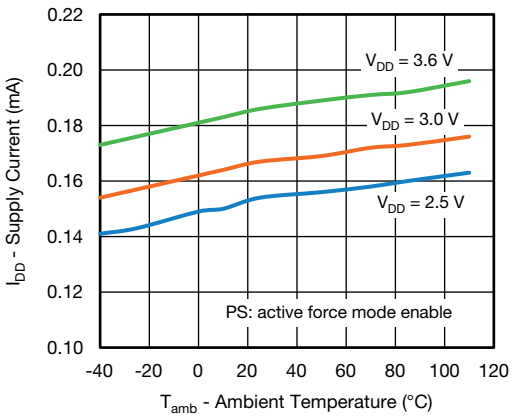


Fig. 5 - Supply Current vs. Ambient Temperature

APPLICATION INFORMATION

Pin Connection with the Host

VCNL3036X01 integrates proximity sensor and an LED driver with three inputs for external IREDs all together with I²C interface. It is very easy for the baseband (CPU) to access PS output data via I²C interface without extra software algorithms. The hardware schematic is shown in the following diagram.

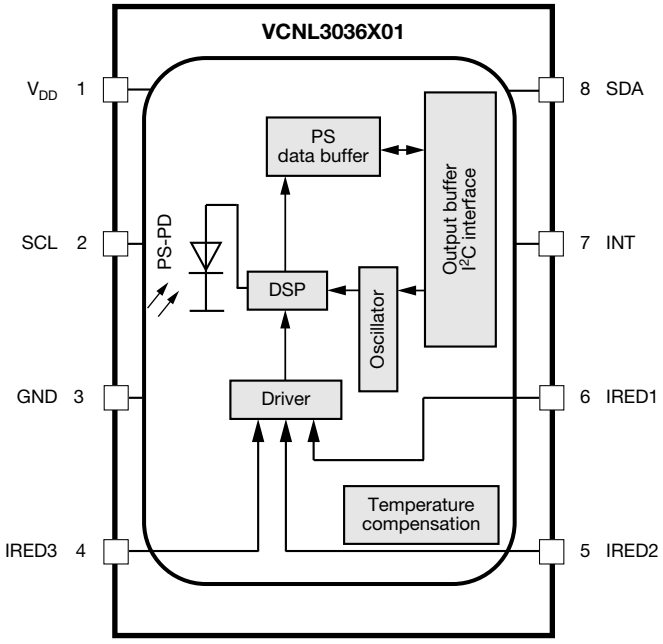
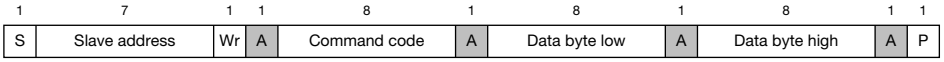


Fig. 6 - Detailed Block Diagram

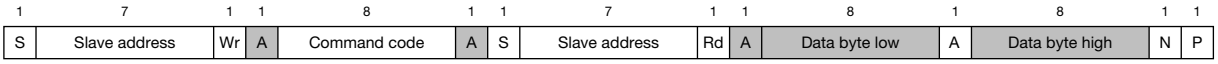
Digital Interface

VCNL3036X01 applies single slave address 0x41 (HEX) of 7-bit addressing following I²C protocol. All operations can be controlled by the command register. The simple command structure helps users easily program the operation setting and latch the light data from VCNL3036X01. As Fig. 10 shows, VCNL3036X01's I²C command format is simple for read and write operations between VCNL3036X01 and the host. The white sections indicate host activity and the gray sections indicate VCNL3036X01's acknowledgement of the host access activity. Write word and read word protocol is suitable for accessing registers particularly for 12-bit / 16-bit PS data. Interrupt can be cleared by reading data out from register: INT_Flag. All command codes should follow read word and write word protocols.

Send Byte → Write Command to VCNL3036X01



Receive Byte → Read Data from VCNL3036X01



S = start condition
P = stop condition
A = acknowledge
N = no acknowledge
Shaded area = VCNL3036X01 acknowledge

Fig. 7 - Write Word and Read Word Protocol

Function Description

For proximity sensor function, VCNL3036X01 supports different kinds of mechanical designs to achieve the best proximity detection performance for any color of object with more flexibility. The basic PS function settings, such as duty ratio, integration time, interrupt, and PS enable / disable, and persistence, are handled by the register: PS_CONF1. Duty ratio controls the PS response time. Integration time represents the duration of the energy being received. The interrupt is asserted when the PS detection levels over the high threshold level setting (register: PS_THDH) or lower than low threshold (register: PS_THDL). If the interrupt function is enabled, the host reads the PS output data from VCNL3036X01 that saves host loading from periodically reading PS data. More than that, INT flag (register: INT_Flag) indicates the behavior of INT triggered under different conditions. PS persistence (PS_PERS) sets up the PS INT asserted conditions as long as the PS output value continually exceeds the threshold level. The intelligent cancellation level can be set on register: PS_CANC to reduce the cross talk phenomenon.

VCNL3036X01 also supports an easy use of proximity detection logic output mode that outputs just high / low levels saving loading from the host. Normal operation mode or proximity detection logic output mode can be selected on the register: PS_MS. A smart persistence is provided to get faster PS response time and prevent false trigger for PS. Descriptions of each slave address operation are shown in table 1.

TABLE 1 - COMMAND CODE AND REGISTER DESCRIPTION

COMMAND CODE	DATE BYTE LOW / HIGH	REGISTER NAME	R / W	DEFAULT VALUE	FUNCTION DESCRIPTION
0x00	L	Reserved	R	0x01	Reserved
	H	Reserved	R	0x01	Reserved
0x01	L	Reserved	R	0x00	Reserved
	H	Reserved	R	0x00	Reserved
0x02	L	Reserved	R	0x00	Reserved
	H	Reserved	R	0x00	Reserved
0x03	L	PS_CONF1	R / W	0x01	PS duty ratio, integration time, persistence, and PS enable / disable
	H	PS_CONF2	R / W	0x00	PS gain, PS output resolution selection, PS interrupt trigger method
0x04	L	PS_CONF3	R / W	0x00	PS smart persistence, active force mode, IRED select
	H	PS_MS	R / W	0x00	LED current selection
0x05	L	PS_CANC_L	R / W	0x00	PS cancellation level setting
	H	PS_CANC_M	R / W	0x00	PS cancellation level setting
0x06	L	PS_THDL_L	R / W	0x00	PS low interrupt threshold setting LSB byte
	H	PS_THDL_M	R / W	0x00	PS low interrupt threshold setting MSB byte
0x07	L	PS_THDH_L	R / W	0x00	PS high interrupt threshold setting LSB byte
	H	PS_THDH_M	R / W	0x00	PS high interrupt threshold setting MSB byte
0x08	L	PS1_Data_L	R	0x00	PS1 LSB output data
	H	PS1_Data_M	R	0x00	PS1 MSB output data
0x09	L	PS2_Data_L	R	0x00	PS2 LSB output data
	H	PS2_Data_M	R	0x00	PS2 MSB output data
0x0A	L	PS3_Data_L	R	0x00	PS3 LSB output data
	H	PS3_Data_M	R	0x00	PS3 MSB output data
0x0B	L	Reserved	R	0x00	Reserved
	H	Reserved	R	0x00	Reserved
0x0C	L	Reserved	R	0x00	Reserved
	H	Reserved	R	0x00	Reserved
0x0D	L	Reserved	R	0x00	Reserved
	H	INT_Flag	R	0x00	PS interrupt flags
0x0E	L	ID_L	R	0x80	Device ID LSB
	H	ID_M	R	0x00	Device address: 0x41

Note

- All of reserved register are used for internal test. Please keep as default setting

Command Register Format

VCNL3036X01 provides an 8-bit command register for PS controlling independently. The description of each command format is shown in following tables.

TABLE 2 - REGISTER: RESERVED		
REGISTER NAME		**COMMAND CODE: 0x00_L (0x00 DATA BYTE LOW)**
Command	Bit	Description
Reserved	7 : 0	Default = 01H

TABLE 3 - REGISTER: RESERVED		
		COMMAND CODE: 0x00_H (0x00 DATA BYTE HIGH)
Command	Bit	Description
Reserved	7 : 0	Default = 01H

TABLE 4 - REGISTER RESERVED		
		COMMAND CODE: 0x01_L (0x01 DATA BYTE LOW) AND 0x01_H (0x01 DATA BYTE HIGH)
Register	Bit	Description
Reserved	7 : 0	Reserved

TABLE 5 - REGISTER: RESERVED		
		COMMAND CODE: 0x02_L (0x02 DATA BYTE LOW) AND 0x02_H (0x02 DATA BYTE HIGH)
Register	Bit	Description
Reserved	7 : 0	Reserved

TABLE 6 - REGISTER: PS_CONF1 DESCRIPTION		
REGISTER: PS_CONF1		**COMMAND CODE: 0x03_L (0x03 DATA BYTE LOW)**
Command	Bit	Description
PS_Duty	7 : 6	(0 : 0) = 1/40, (0 : 1) = 1/80, (1 : 0) = 1/160, (1 : 1) = 1/320 PS IRED on / off duty ratio setting
PS_PERS	5 : 4	(0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 3, (1 : 1) = 4 PS interrupt persistence setting
PS_ IT	3 : 1	(0 : 0 : 0) = 1T, (0 : 0 : 1) = 1.5T, (0 : 1 : 0) = 2T, (0 : 1 : 1) = 2.5T, (1 : 0 : 0) = 3T, (1 : 0 : 1) = 3.5T, (1 : 1 : 0) = 4T, (1 : 1 : 1) = 8T, PS integration time setting
PS_SD	0	0 = PS power on, 1 = PS shut down, default = 1

TABLE 7 - REGISTER: PS_CONF2 DESCRIPTION		
REGISTER: PS_CONF2		**COMMAND CODE: 0x03_H (0x03 DATA BYTE HIGH)**
Command	Bit	Description
MPX_INT_EN	7	0 = disabled, 1 = enabled
MPX_MODE	6	0 = disabled, 1 = enabled
PS_Gain	5 : 4	(0 : 0) and (0 : 1) = two step mode, (1: 0) single mode x 8, (1 : 1) single mode x 1
PS_HD	3	0 = PS output is 12 bits, 1 = PS output is 16 bits
PS_NS	2	(0 : 0) and (0 : 1) = two step mode, (1: 0) single mode x 8, (1 : 1) single mode x 1
PS_INT	1 : 0	(0 : 0) = interrupt disable, (0 : 1) = trigger by closing, (1 : 0) = trigger by away, (1 : 1) = trigger by closing and away

TABLE 8 - REGISTER: PS_CONF3 DESCRIPTION		
REGISTER: PS_CONF3		**COMMAND CODE: 0x04_L (0x04 DATA BYTE LOW)**
Command	Bit	Description
LED_I_LOW	7	0 = disabled = normal current, 1 = enabled = 1/10 of normal current, with that the current is accordingly: 5 mA, 7.5 mA, 10 mA, 12 mA, 14 mA, 16 mA, 18 mA, 20 mA
IRED select	6 : 5	(0 : 0) = IRED1, (0 : 1) = IRED2, (1 : 0) = IRED3, (1 : 1) = IRED3
PS_SMART_PERS	4	0 = disable; 1 = enable PS smart persistence
PS_AF	3	0 = active force mode disable (normal mode), 1 = active force mode enable
PS_TRIG	2	0 = no PS active force mode trigger, 1 = trigger one time cycle VCNL3036X01 output one cycle data every time host writes in '1' to sensor. The state returns to '0' automatically.
PS_MS	1	0 = proximity normal operation with interrupt function 1 = proximity detection logic output mode enable
PS_SC_EN	0	0 = turn off sunlight cancel; 1 = turn on sunlight cancel PS sunlight cancel function enable setting

TABLE 9 - REGISTER: PS_MS DESCRIPTION		
REGISTER: PS_MS		**COMMAND CODE: 0x04_H (0x04 DATA BYTE HIGH)**
Command	Bit	Description
Reserved	7	0
PS_SC_CUR	6 : 5	(0 : 0) = 1 x typical sunlight cancel current, (0 : 1) = 2 x typical sunlight cancel current, (1 : 0) = 4 x typical sunlight cancel current, (1 : 1) = 8 x typical sunlight cancel current
PS_SP	4	0 = typical sunlight capability, 1 = 1.5 x typical sunlight capability
PS_SPO	3	0 = output is 00h in sunlight protect mode, 1 = output is FFh in sunlight protect mode,
LED_I	2 : 0	(0 : 0 : 0) = 50 mA; (0 : 0 : 1) = 75 mA; (0 : 1 : 0) = 100 mA; (0 : 1 : 1) = 120 mA (1 : 0 : 0) = 140 mA; (1 : 0 : 1) = 160 mA; (1 : 1 : 0) = 180 mA; (1 : 1 : 1) = 200 mA LED current selection setting

TABLE 10 - REGISTER PS_CANC_L AND PS_CANC_M DESCRIPTION		
		COMMAND CODE: 0x05_L (0x05 DATA BYTE LOW) AND 0x05_H (0x05 DATA BYTE HIGH)
Register	Bit	Description
PS_CANC_L	7 : 0	0x00 to 0xFF, PS cancellation level setting_LSB byte
PS_CANC_M	7 : 0	0x00 to 0xFF, PS cancellation level setting_MSB byte

TABLE 11 - REGISTER: PS_THDL_L AND PS_THDL_M DESCRIPTION		
		COMMAND CODE: 0x06_L (0x06 DATA BYTE LOW) AND 0x06_H (0x06 DATA BYTE HIGH)
Register	Bit	Description
PS_THDL_L	7 : 0	0x00 to 0xFF, PS interrupt low threshold setting_LSB byte
PS_THDL_M	7 : 0	0x00 to 0xFF, PS interrupt low threshold setting_MSB byte

TABLE 12 - REGISTER: PS_THDH_L AND PS_THDH_M DESCRIPTION		
		COMMAND CODE: 0x07_L (0x07 DATA BYTE LOW) AND 0x07_H (0x07 DATA BYTE HIGH)
Register	Bit	Description
PS_THDH_L	7 : 0	0x00 to 0xFF, PS interrupt high threshold setting_LSB byte
PS_THDH_M	7 : 0	0x00 to 0xFF, PS interrupt high threshold setting_MSB byte

TABLE 13 - READ OUT REGISTER DESCRIPTION			
Register	Command Code	Bit	Description
PS1_Data_L	0x08_L (0x08 data byte low)	7 : 0	0x00 to 0xFF, PS1 LSB output data
PS1_Data_M	0x08_H (0x08 data byte high)	7 : 0	0x00 to 0xFF, PS1 MSB output data
PS2_Data_L	0x09_L (0x09 data byte low)	7 : 0	0x00 to 0xFF, PS2 LSB output data
PS2_Data_M	0x09_H (0x09 data byte high)	7 : 0	0x00 to 0xFF, PS2 MSB output data
PS3_Data_L	0x0A_L (0x0A data byte low)	7 : 0	0x00 to 0xFF, PS3 LSB output data
PS3_Data_M	0x0A_H (0x0A data byte high)	7 : 0	0x00 to 0xFF, PS3 MSB output data
Reserved	0x0B_L (0x0B data byte low)	7 : 0	Reserved
Reserved	0x0B_H (0x0B data byte high)	7 : 0	Reserved
Reserved	0x0C_L (0x0C data byte low)	7 : 0	Reserved
Reserved	0x0C_H (0x0C data byte high)	7 : 0	Reserved
Reserved	0x0D_L (0x0D data byte low)	7 : 0	Default = 0x00
INT_Flag	0x0D_H (0x0D data byte high)	7	MPX_DATA_READY_FLAG
		6	PS_SPFLAG, PS entering protection mode
		5 : 2	Reserved
		1	PS_IF_CLOSE, PS rises above PS_THDH INT trigger event
		0	PS_IF_AWAY, PS drops below PS_THDL INT trigger event
ID_L	0x0E_H (0x0E data byte low)	7 : 0	0x80
ID_M	0x0E_H (0x0E data byte high)	7 : 6	(0 : 0)
		5 : 4	(0 : 0) Slave address = 0x41 (7-bit)
		3 : 0	Version code (0 : 0 : 0 : 0)

Adjustable Sampling Time

VCNL3036X01's embedded IRED driver drives up to 3 external IREDs by a pulsed duty cycle. The IRED on / off duty ratio is programmable by I^2C command at register: PS_Duty which is related to the current consumption and PS response time. The higher the duty ratio adopted, the faster response time achieved with higher power consumption. For example, PS_Duty = 1/320, peak IRED current = 100 mA, averaged current consumption is 100 mA/320 = 0.3125 mA.

Initialization

VCNL3036X01 includes default values for each register. As long as power is on, it is ready to be controlled by host via I^2C bus.

Threshold Window Setting

- Programmable PS Threshold

  VCNL3036X01 provides both high and low thresholds for PS (register: PS_THDL, PS_THDH)

- PS Persistence

  The PS persistence function (PS_PERS, 1, 2, 3, 4) helps to avoid false trigger of the PS INT. For example, if PS_PERS = 3 times, the PS INT will not be asserted unless the PS value is greater than the PS threshold (PS_THDH) value for three periods of time continuously

- PS Active Force Mode

  An extreme power saving way to use PS is to apply PS active force (register: PS_CONF3 command: PS_FOR = 1) mode. Anytime host would like to read out just one of PS data, write in '1' at register: PS_CONF3 command: PS_FOR_Trig. Without commands placed, there is no PS data output. VCNL3036X01 stays in standby mode constantly

Intelligent Cancellation

VCNL3036X01 provides an intelligent cancellation method to reduce cross talk phenomenon for the proximity sensor. The output data will be subtracted by the input value on register: PS_CANC.

Interruption (INT)

VCNL3036X01 has PS interrupt feature operated by a single pin “INT”. The purpose of the interrupt feature is to actively inform the host once INT has been asserted. With the interrupt function applied, the host does not need to be constantly pulling data from the sensor, but to read data from the sensor while receiving interrupt request from the sensor. As long as the host enables PS interrupt (register: PS_INT) function, the level of INT pin (pin 7) is pulled low once INT asserted. All registers are accessible even if INT is asserted.

To effectively adopt PS INT function, it is recommended to use PS detection mechanism at register: PS_INTT = 1 for the best PS detection performance which can be adjusted by high / low THD level of PS. PS INT trigger way is defined by register: PS_INT.

Interruption Flag

Register: INT_Flag represents all of interrupt trigger status for PS. Any flag value changes from “0” to “1” state, the level of INT pin will be pulled low. As long as host reads INT_Flag data, the bit will change from “1” state to “0” state after reading out, the INT level will be returned to high afterwards.

PROXIMITY DETECTION LOGIC OUTPUT MODE

VCNL3036X01 provides a proximity detection logic output mode that uses INT pin (pin 7) as a proximity detection logic high / low output (register: PS_MS). When this mode is selected, the PS output (pin 7; INT/P_{out}) is pulled low when an object is closing to be detected and returned to level high when the object moves away. Register: PS_THDH / PS_THDL defines how sensitive PS detection is.

One thing to be stated is that whenever proximity detection logic mode applied, INT pin is only used as a logic high / low output. Meanwhile, host has to simulate the GPIO pin as an INT pin function. If not, host needs to periodically reading the state of INT at this GPIO pin.

PROXIMITY DETECTION HYSTERESIS

A PS detection hysteresis is important that keeps PS state in a certain range of detection distance. For example, PS INT asserts when PS value over PS_THDH. Host switches off panel backlight and then clears INT. When PS value is less than PS_THDL, host switches on panel backlight. Any PS value lower than PS_THDH or higher than PS_THDL, PS INT will not be asserted. Host does keep the same state.

MULTIPLEX FEATURE WITH VCNL3036X01

VCNL3036X01 allows to connect up to 3 external IREDs. Each may be selected separate to allow for normal proximity.

If one select e.g. IRED2 then also PS2 delivers the corresponding proximity data. To allow for a fast quasi-parallel measurements of all three channels the MPX_MODE may be activated (set to “1”).

Within “PS_FORCE_MODE” all three IREDs will be sequentially switched and available proximity result of this directly shown within the three PS_DATA register.

Beside MPX_MODE enabled and PS_FORCE_MODE set this sequence starts direct after setting the PS_TRIG bit. Availability of the data will be indicated with setting the MPX_DATA_READY flag or also the Interrupt if this is set-up also. Please see below diagram.

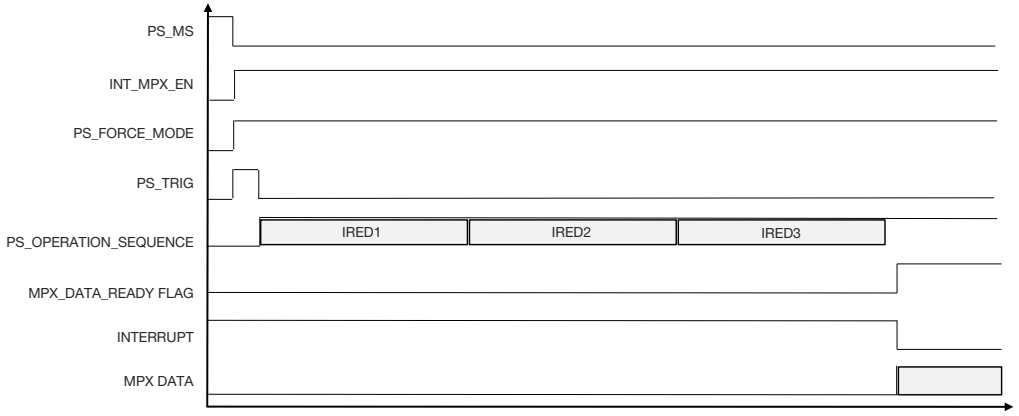


Fig. 8 - VCNL3036X01 MPX Mode Sequence

APPLICATION CIRCUIT BLOCK REFERENCE

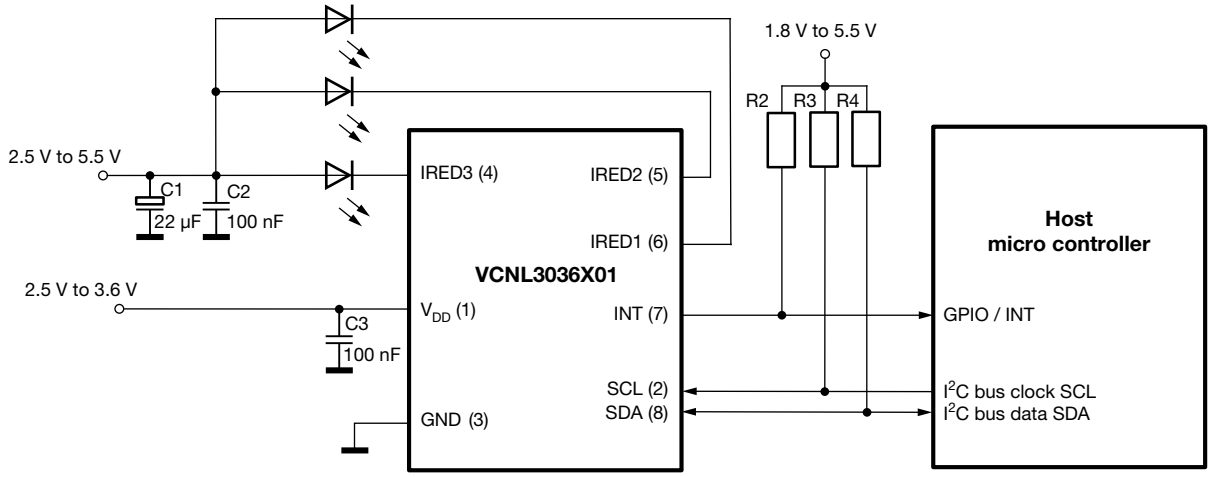


Fig. 9 - Circuitry with Two Separate Power Supply Sources

Three additional capacitors in the circuit are proposed for the following purposes: (1) the 100 nF capacitor near the V_{DD} pin is used for power supply noise rejection, (2) the 22 µF plus parallel 100 nF capacitors - connected to the common anode of the external IREDs - are used to prevent the IRED voltage from instantly dropping when an IRED is switched on, and (3) 2.2 kΩ to 4.7 kΩ are recommended values for the pull up resistor of I^2C. The value of the pull-up resistor at the INT line could be 10 kΩ applied on the INT pin.

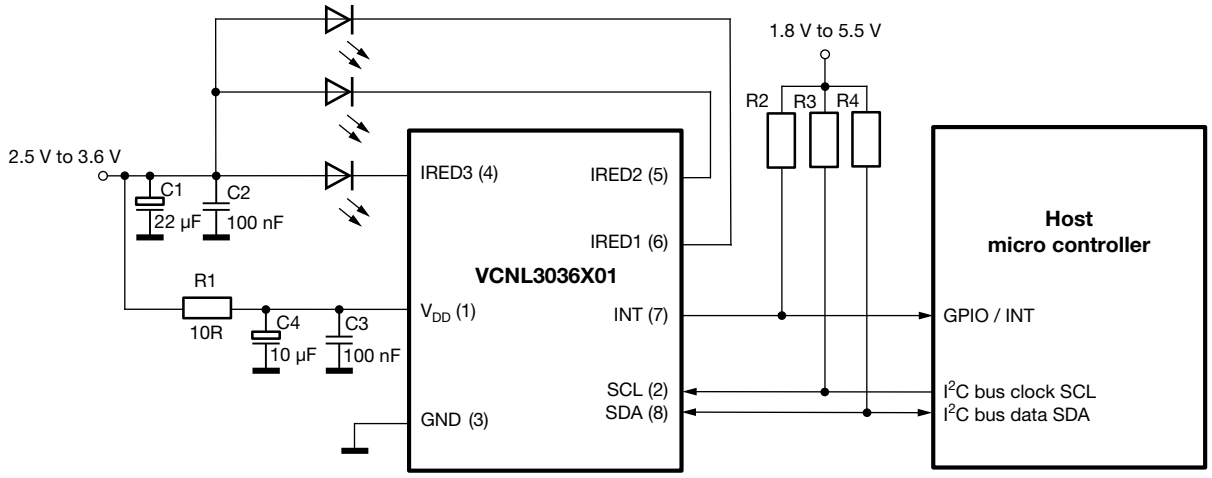
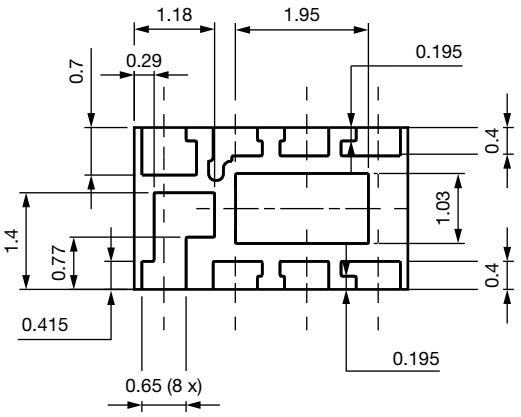


Fig. 10 - Circuitry with just One Common Power Supply Source

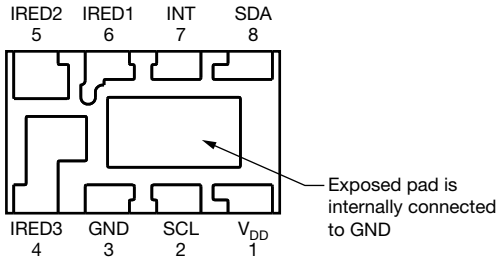
For high currents of the IREDs and / or power supply close to the lower limit of 2.5 V this R-C decoupling will prevent that the V_{DD} voltage drop below specified minimum.

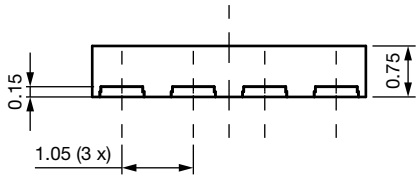
Mechanical placement of the external IRED depends on the application.

PACKAGE DIMENSIONS in millimeters

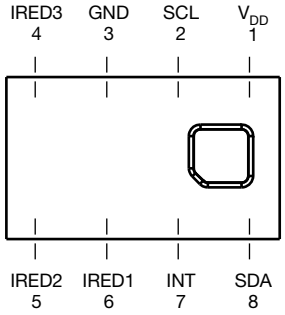


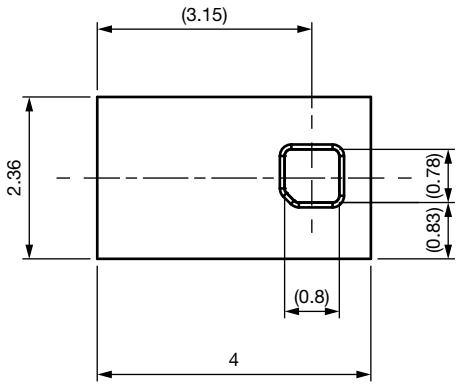
Pinning bottom view



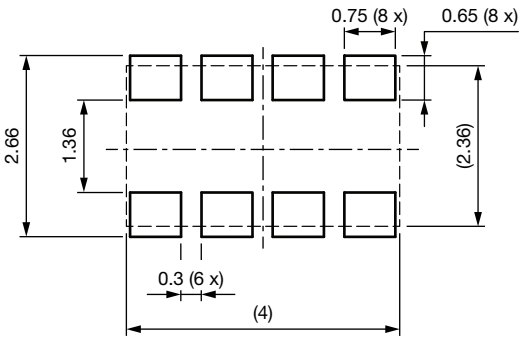


Pinning top view





Recommended solder foot print



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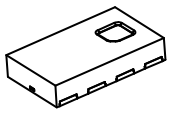
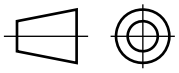
Issue: 1; 27.07.2020

Not indicated tolerances ± 0.1 mm





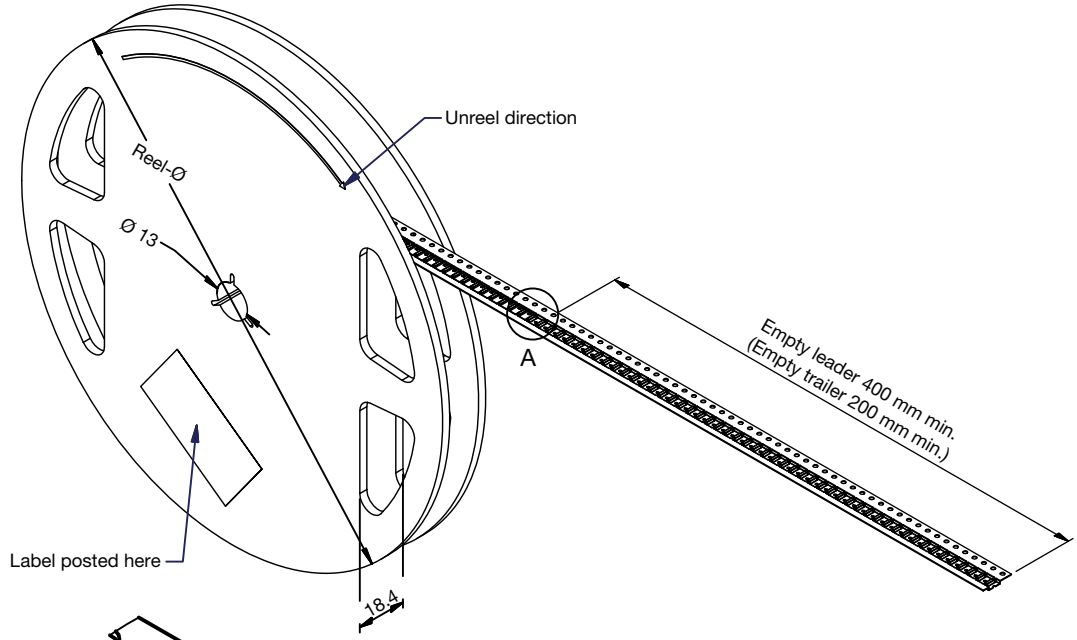
Technical drawings according to DIN specification.

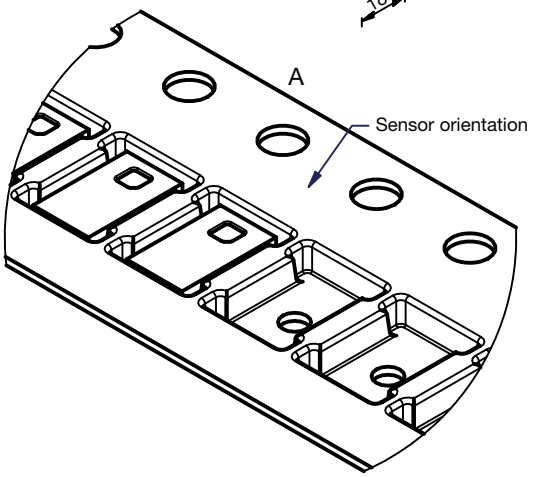
TAPE AND REEL DIMENSIONS in millimeters

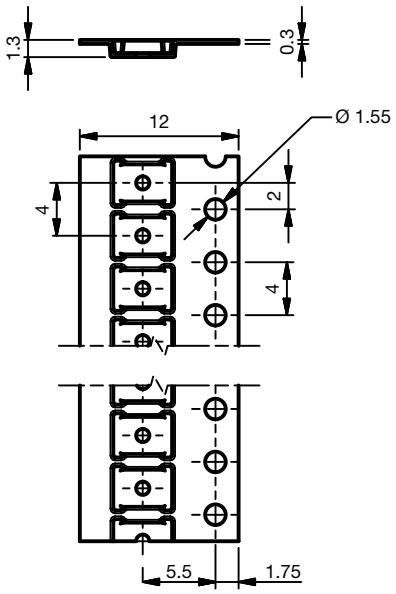
Reel-size:
GS 08: Ø 180 mm ± 2 mm = 3300 pcs.
GS 18: Ø 330 mm ± 2 mm = 13 000 pcs.

Non tolerated dimensions ± 0.1 mm

Reel-design is representative for different types.







Drawing No.: 9.800-5143.01-4
Issue: prel., 06.06.2017

SOLDER PROFILE

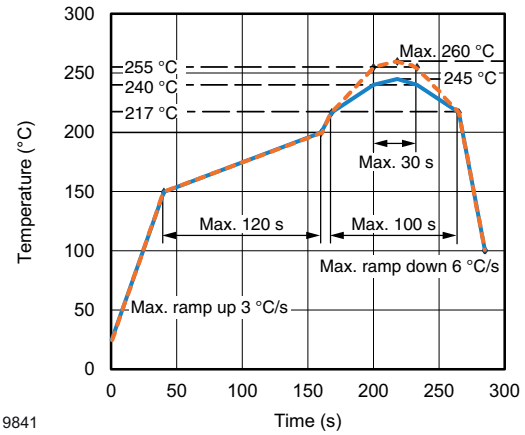


Fig. 11 - Lead (Pb)-free Reflow Solder Profile according to J-STD-020

DRYPACK

Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

FLOOR LIFE

Floor life (time between soldering and removing from MBB) must not exceed the time indicated on MBB label:

Floor life: 168 h

Conditions: T_{amb} < 30 °C, RH < 60 %

Moisture sensitivity level 3, according to J-STD-020.

DRYING

In case of moisture absorption devices should be baked before soldering. Conditions see J-STD-020 or label. Devices taped on reel dry using recommended conditions 192 h at 40 °C (+ 5 °C), RH < 5 %.

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