Rad Hard NPN Silicon Switching Transistor
Screened per MIL-PRF-19500 & ESCC 22900

Screened Levels:
MVR

QPL RANGE and RAD LEVEL	
Radiation Level	**MVR2N2222AUA**
TID	100 Krad
ELDRS	100 Krad

DESCRIPTION

This RHA level NPN switching transistor, MVR2N2222AUA device in a UA package, is ideal to drive many high-reliability applications. This device is constructed and screened to a JANTXV performance level with radiation test method 1019 wafer lot acceptance conducted on all die lots. Fully compliant to **GSFC EEE-INST-002** reliability, screening and radiation hardness assurance requirements for space flight projects.

Important: For the latest information, visit our website http://www.microsemi.com.

FEATURES

- JEDEC registered 2N2222
- TID level screened per MIL-PRF-19500
- Also available with ELDRS testing to 0.01 Rad(s)/ sec
- PIND testing option available
- MKCR/MHCR chip die available
- RHA (Radiation Hardness Assured) lot by lot validation testing

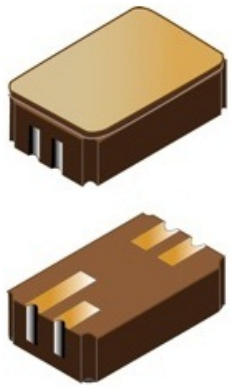
APPLICATIONS / BENEFITS

- Rad-Hard power supplies
- Rad-Hard motor controls
- General purpose switching
- Instrumentation Amps
- EPS Satellite switching power applications

MAXIMUM RATINGS

Parameters/Test Conditions	Symbol	Value	Unit
Junction and Storage Temperature	T_J and T_{STG}	-65 to +200	ºC
Thermal Resistance Junction-to-Solder Pad (Ambient) (see Figure 4)	$R_{\Theta JSP(AM)}$	40	ºC/W
Thermal Resistance Junction-to-Solder Pad (Infinite Sink) (see Figure 3)	$R_{\Theta JSP(IS)}$	110	ºC/W
Thermal Resistance Junction-to-Ambient (see Figure 3) (1)	$R_{\Theta JA}$	325	ºC/W
Total Power Dissipation: (see Figures 1 and 2) @ T_A = +25 ºC @ $T_{SP(IS)}$ = +25 ºC @ $T_{SP(AM)}$ = +25 ºC	P_T	0.5 1.0 1.5	W
Collector-Base Voltage, Emitter Open	V_{CBO}	75	V
Emitter-Base Voltage, Collector Open	V_{EBO}	6	V
Collector-Emitter Voltage, Base Open	V_{CEO}	50	V
Collector Current, dc	I_C	800	mA
Solder Temperature @ 10 s	T_{SP}	260	ºC

Notes: 1. For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute MIL-PRF-19500/255 figures 8 and 13 and use $R_{\theta JA}$.



UA Package

Also available in:

TO-206AA (TO-18) package
(leaded top-hat)
MVR2N2221A(L)

UB package
(surface mount)
MVR2N2221AUB

MSC – Lawrence
6 Lake Street,
Lawrence, MA 01841
Tel: 1-800-446-1158 or
(978) 620-2600
Fax: (978) 689-0803

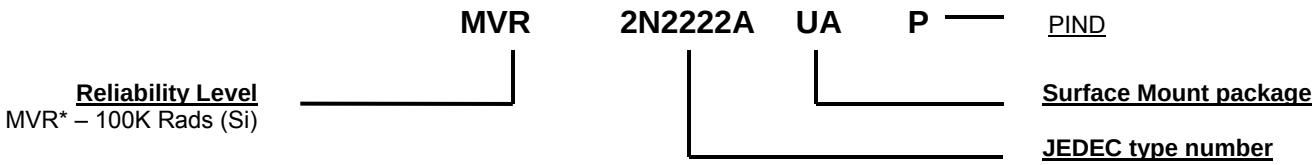
MSC – Ireland
Gort Road Business Park,
Ennis, Co. Clare, Ireland
Tel: +353 (0) 65 6840044
Fax: +353 (0) 65 6822298

Website:
www.microsemi.com

MECHANICAL and PACKAGING

- CASE: Hermetically sealed ceramic package
- TERMINALS: Gold plate over nickel
- MARKING: Manufacturer's ID, date code, part number
- POLARITY: NPN (see package outline)
- TAPE & REEL option: Per EIA-481 (consult factory for quantities)
- WEIGHT: Approximately 0.12 grams
- See Package Dimensions on last page.

PART NOMENCLATURE



*The MVR designator is our internal part nomenclature assigned to this family of parts, in lieu of pending JANTXVR submissions through DLA (Defense Logistic Agency).

SYMBOLS & DEFINITIONS

Symbol	Definition
I_B	Base current: The value of the dc current into the base terminal.
I_C	Collector current: The value of the dc current into the collector terminal.
I_E	Emitter current: The value of the dc current into the emitter terminal.
R_G	Gate drive impedance or Gate resistance
V_{CB}	Collector-base voltage: The dc voltage between the collector and the base.
V_{CBO}	Collector-base voltage, base open: The voltage between the collector and base terminals when the emitter terminal is open-circuited.
V_{CE}	Collector-emitter voltage: The dc voltage between the collector and the emitter.
V_{CEO}	Collector-emitter voltage, base open: The voltage between the collector and the emitter terminals when the base terminal is open-circuited.
V_{EB}	Emitter-base voltage: The dc voltage between the emitter and the base
V_{EBO}	Emitter-base voltage, collector open: The voltage between the emitter and base terminals with the collector terminal open-circuited.

ELECTRICAL CHARACTERISTICS @ T_A= 25 ºC unless otherwise noted.

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage I_C = 10 mA	$V_{(BR)CEO}$	50		V
Collector-Base Cutoff Current V_{CB} = 75 V V_{CB} = 60 V	I_{CBO}		10 10	µA nA
Emitter-Base Cutoff Current V_{EB} = 6.0 V V_{EB} = 4.0 V	I_{EBO}		10 10	µA nA
Collector-Emitter Cutoff Current V_{CE} = 50 V	I_{CES}		50	nA
ON CHARACTERISTICS (1)				
Forward-Current Transfer Ratio I_C = 0.1 mA, V_{CE} = 10 V I_C = 1.0 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 150 mA, V_{CE} = 10 V I_C = 500 mA, V_{CE} = 10 V	h_{FE}	 50 75 100 100 30	 325 300 	
Collector-Emitter Saturation Voltage I_C = 150 mA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA	$V_{CE(sat)}$		0.3 1.0	V
Base-Emitter Voltage I_C = 150 mA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA	$V_{BE(sat)}$	0.6	1.2 2.0	V

DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Small-Signal Short-Circuit Forward Current Transfer Ratio I_C = 1.0 mA, V_{CE} = 10 V, f = 1.0 kHz	h_{fe}	50		
Magnitude of Small–Signal Short-Circuit Forward Current Transfer Ratio I_C = 20 mA, V_{CE} = 20 V, f = 100 MHz	$\|h_{fe}\|$	2.5		
Output Capacitance V_{CB} = 10 V, I_E = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{obo}		8.0	pF
Input Capacitance V_{EB} = 0.5 V, I_C = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{ibo}		25	pF

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-On Time	t_{on}		35	ηs
Turn-Off Time	t_{off}		300	ns

GRAPHS

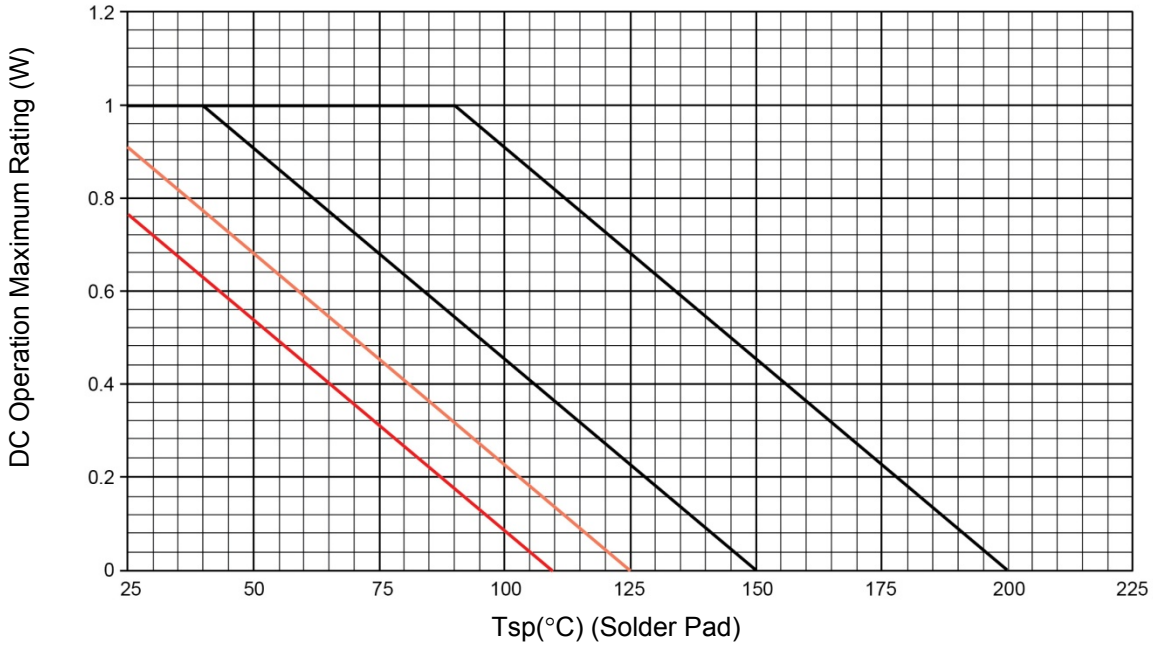


FIGURE 1
Temperature-Power Derating (Infinite sink mount to PCB)

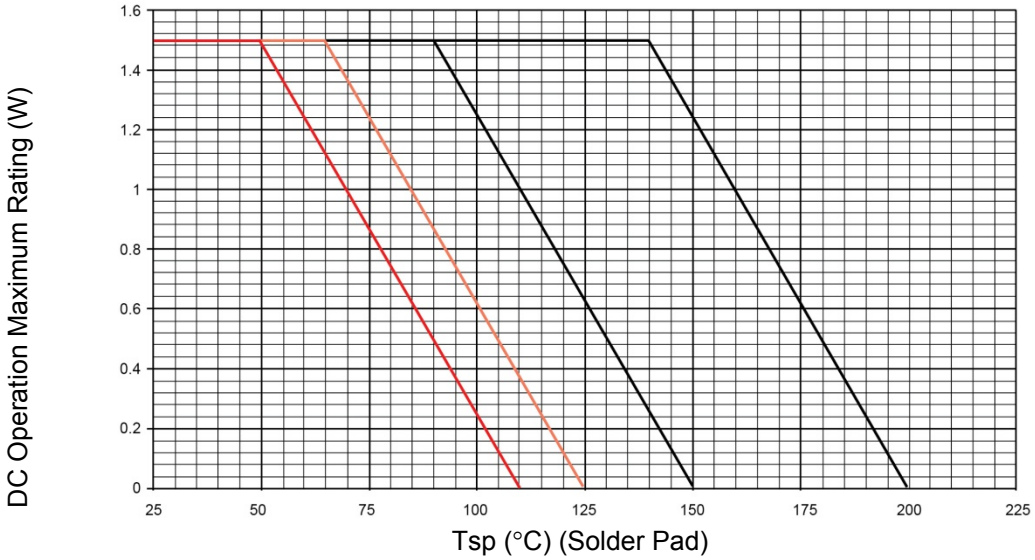


FIGURE 2
Temperature-power Derating (Adhesive mount to PCB)

GRAPHS (continued)

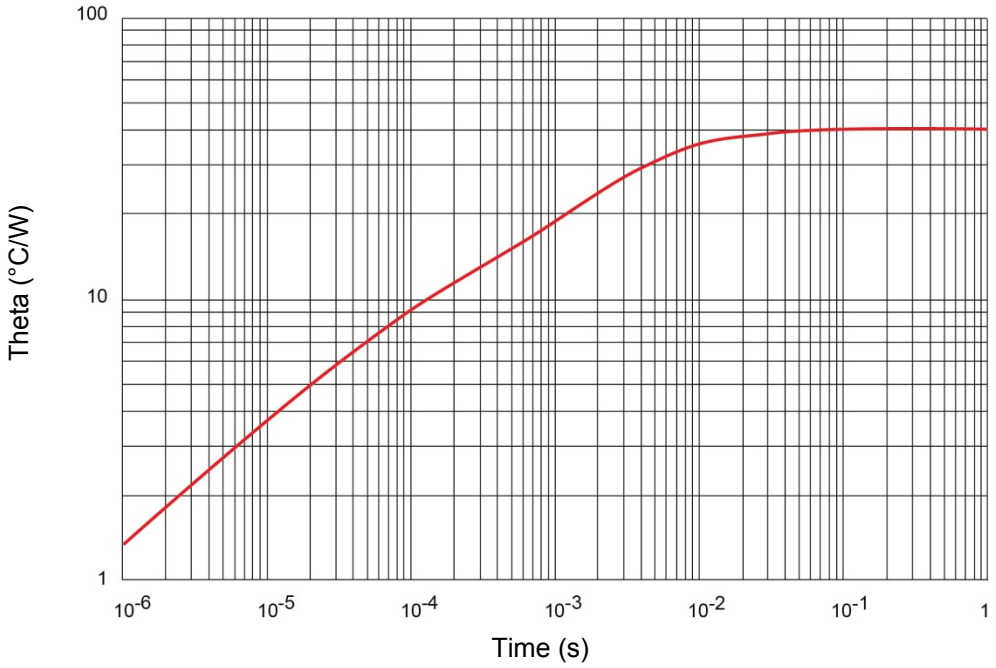


FIGURE 3
Thermal impedance graph ($R_{\Theta JSP(AM)}$) (Dhesive mount to PCB)

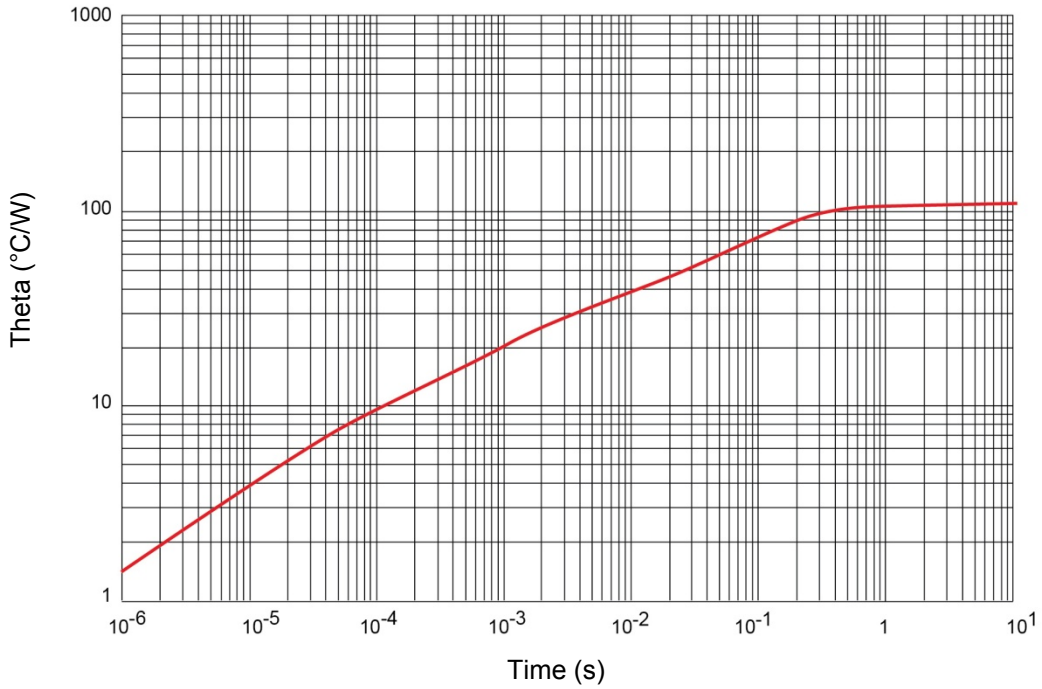


FIGURE 4
Thermal impedance graph ($R_{\Theta JSP(IS)}$) (Infinite Heat Sink to PCB)

Radiation hardness assurance

The MVR series product are guaranteed in radiation with full compliance to MIL-PRF-19500 specification JANTXV(R) level and also guaranteed to meet ESCC 22900 specifications (General specifications).

Radiation assurance MIL-PRF-19500

MVR parts are guaranteed at 100 krad (Si), tested, in full compliancy with the MIL-PRF-19500 specification, specifically the Group D, subgroup 2 inspection, between 50 and 300 rad/s. All test are performed in accordance to MIL-PRF-19500 and test method 1019 of MIL-STD-750 for total Ionizing dose.

– Each wafer of each lot is tested, (note 1). The table below provides for each monitored parameters of the test conditions and the acceptance criteria

ELECTRICAL CHARACTERISTICS @ T_A = +25 °C, unless otherwise noted (continued)

POST RADIATION

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Collector to Base Cutoff Current V_{CB} = 75 V V_{CB} = 60 V	I_{CBO}		 20 20	 µA nA
Emitter to Base Cutoff Current V_{EB} = 6 V V_{EB} = 4 V	I_{EBO}		 20 20	 µA nA
Collector to Emitter Breakdown Voltage I_C = 10 mA	$V_{(BR)CEO}$	50		V
Forward-Current Transfer Ratio (1) I_C = 0.1 mA, V_{CE} = 10 V I_C = 1.0 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 150 mA, V_{CE} = 10 V I_C = 500 mA, V_{CE} = 10 V	$[h_{FE}]$	 [25] [37.5] [50] [50] [15]	 325 300 	
Collector-Emitter Saturation Voltage I_C = 150 µA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA	$V_{CE(sat)}$		 0.35 1.15	 V
Base-Emitter Saturation Voltage I_C = 150 µA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA	$V_{BE(sat)}$	0.6	1.38	V

1. See method 1019 of MIL-STD-750 for how to determine $[h_{FE}]$ by first calculating the delta $(1/h_{FE})$ from the pre- and post-radiation h_{FE}. Notice the $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

ESCC radiation assurance

Each product lot is tested according to the ESCC basic specification 22900, with a minimum of 21 samples per diffusion lot and 10 samples per wafer, one sample being kept as unirradiated sample, all of them being fully compliant with the applicable ESCC generic and/or detailed specification.

- Test of 10 pieces by wafer, 10 biased at least 80% of $V_{(BR)CEO}$, 10 unbiased and 1 kept for reference
- Irradiation at 0.1 rad (Si)/s
- Acceptance criteria of each individual wafer if as 100 krad guaranteed if all 20 samples comply with the post radiation electrical characteristics provided in *Table* 4 (post radiation electrical characteristics for the 2N2222A)
- Delivery together with the parts of the radiation verification test (RVT) report of the particular wafer used to manufacture the products. This RVT includes the value of each parameter at 30, 50, 70 and 100 krad (Si) and after 24 hour annealing at room temperature and after an additional 168 hour annealing at 100°C.

Radiation summary

Radiation test (Note 1)	100 krad ESCC
Wafer test	each
Part tested	10 biased + 10 unbiased
Dose rate	0.1 rad/s
Acceptance	MIL-STD-750 method 1019
Displacement damage	Optional

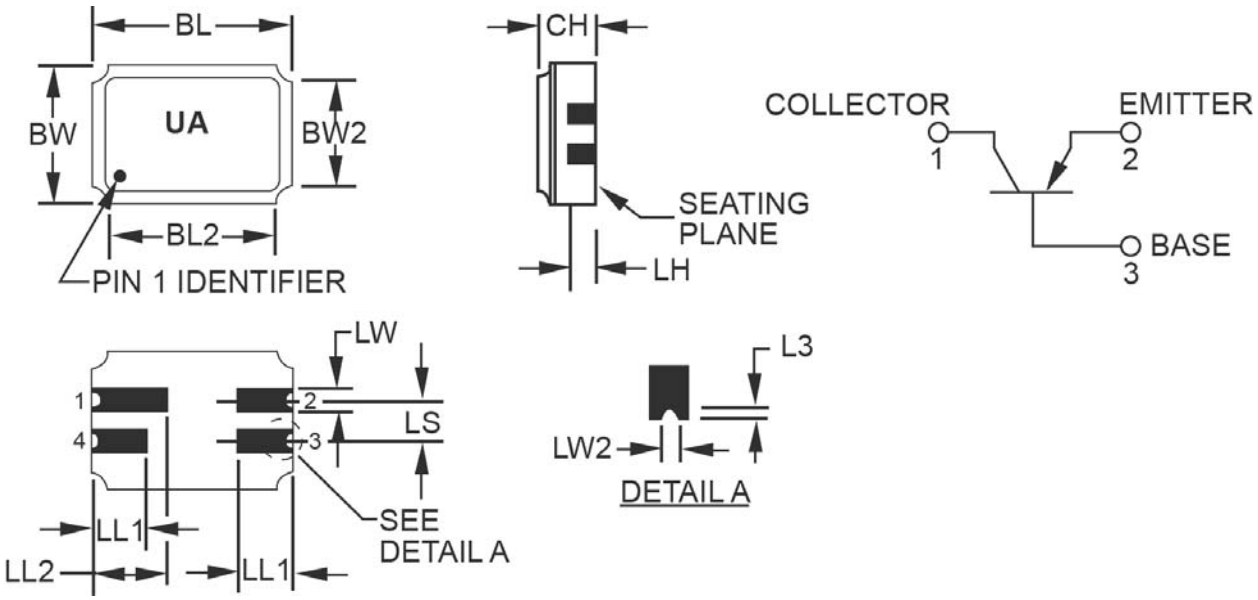
1. Microsemi MVR products will exceed required testing of *ESCC basic specification 22900*

POST RADIATION- Table 4

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Collector to Base Cutoff Current V_{CB} = 75 V V_{CB} = 60 V	I_{CBO}		 20 20	 µA nA
Emitter to Base Cutoff Current V_{EB} = 6 V V_{EB} = 4 V	I_{EBO}		 20 20	 µA nA
Collector to Emitter Breakdown Voltage I_C = 10 mA	$V_{(BR)CEO}$	50		V
Forward-Current Transfer Ratio (1) I_C = 0.1 mA, V_{CE} = 10 V I_C = 1.0 mA, V_{CE} = 10 V I_C = 10 mA, V_{CE} = 10 V I_C = 150 mA, V_{CE} = 10 V I_C = 500 mA, V_{CE} = 10 V	$[h_{FE}]$	 [25] [37.5] [50] [50] [15]	 325 300 	
Collector-Emitter Saturation Voltage I_C = 150 µA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA	$V_{CE(sat)}$		 0.35 1.15	 V
Base-Emitter Saturation Voltage I_C = 150 µA, I_B = 15 mA I_C = 500 mA, I_B = 50 mA	$V_{BE(sat)}$	0.6	1.38	V

2. See method 1019 of MIL-STD-750 for how to determine $[h_{FE}]$ by first calculating the delta $(1/h_{FE})$ from the pre- and post-radiation h_{FE}. Notice the $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Dimension "CH" controls the overall package thickness. When a window lid is used, dimension "CH" must increase by a minimum of 0.010 inch (0.254 mm) and a maximum of 0.040 inch (1.020 mm).
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "LW2" minimum and "L3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension " LW2" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed 0.006 inch (0.15mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

Symbol	Dimensions				Note
	Inch		Millimeters		
	Min	Max	Min	Max	
BL	0.215	0.225	5.46	5.71	
BL2	-	0.225	-	5.71	
BW	0.145	0.155	3.68	3.93	
BW2	-	0.155	-	3.93	
CH	0.061	0.075	1.55	1.90	3
L3	0.003	0.007	0.08	0.18	5
LH	0.029	0.042	0.74	1.07	
LL1	0.032	0.048	0.81	1.22	
LL2	0.072	0.088	1.83	2.23	
LS	0.045	0.055	1.14	1.39	
LW	0.022	0.028	0.56	0.71	
LW2	0.006	0.022	0.15	0.56	5

Pin no.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C