Datasheet

Fully Integrated IPM for Three-Phase HV BLDC Motor

FS9276AS

Fortior Technology (Shenzhen) Co., Ltd

Contents

FS9276AS Fully Integrated IPM for Three-Phase HV BLDC Motor

1 System Introduction

1.1 Overview

FS9276AS is a fully integrated IPM for high-voltage three-phase motor drive applications, incorporating 180 sinusoidal commutation controller chip, high-voltage gate driver chip and fast-recovery power MOS. Due to a high level of integration, few peripheral components are required. The chip supports sensorless FOC, and features with low noise and small torque ripple. Moreover, the chip is secured with a wide range of protection features, including over-current protection (OCP), current-limiting protection (CLP), under-voltage lockout (UVLO), temperature sensor detect (TSD), low temperature protection (LTP), motor lock protection (MLP), configurable maximum speed protection and bus voltage protection. In addition, the chip offers a VSP pin that withstands up to VCC, and supports sleep mode. With strong insulation, high thermal conductivity and low electromagnetic interference, the chip is housed in a compact package and suitable for built-in motors and other space constraint applications.

1.2 Applications

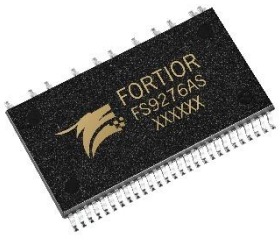
Air conditioner indoor units, high-voltage purifiers, etc.

1.3 Features

- 600V 7A fast-recovery power MOS
- VCC range: 13V ~ 20V
- Sensorless FOC
- Integrated control, drive and high-voltage power MOS
- Forward and reverse direction control
- VSP pin withstanding up to VCC
- FG pulse output (support 8/10-pole motor or 4/12-pulse output)
- PWM, analog voltage and I^2C modes for motor speed regulation
- Soft-on feature protects the motor from abrupt startup and reduces noise during operation
- Support protection features, including OCP, CLP, UVLO, TSD, LTP, MLP, configurable maximum speed protection, bus voltage protection, etc.

1.4 Key Parameters

- MOSFET Output Voltage: 600V
- Drive Current (DC): ± 2.5A (Max.)
- Drive Current (Pulse): ± 7.0A (Max.)
- MOSFET DC Output Resistance: 1.1Ω (Typ.)
- Max. Junction Temperature: +150°C
- Power Dissipation: 3.00W



FS9276AS

1.5 Typical Application Diagram

1.5.1 Sensorless FOC Mode with Single-shunt Differential Sampling

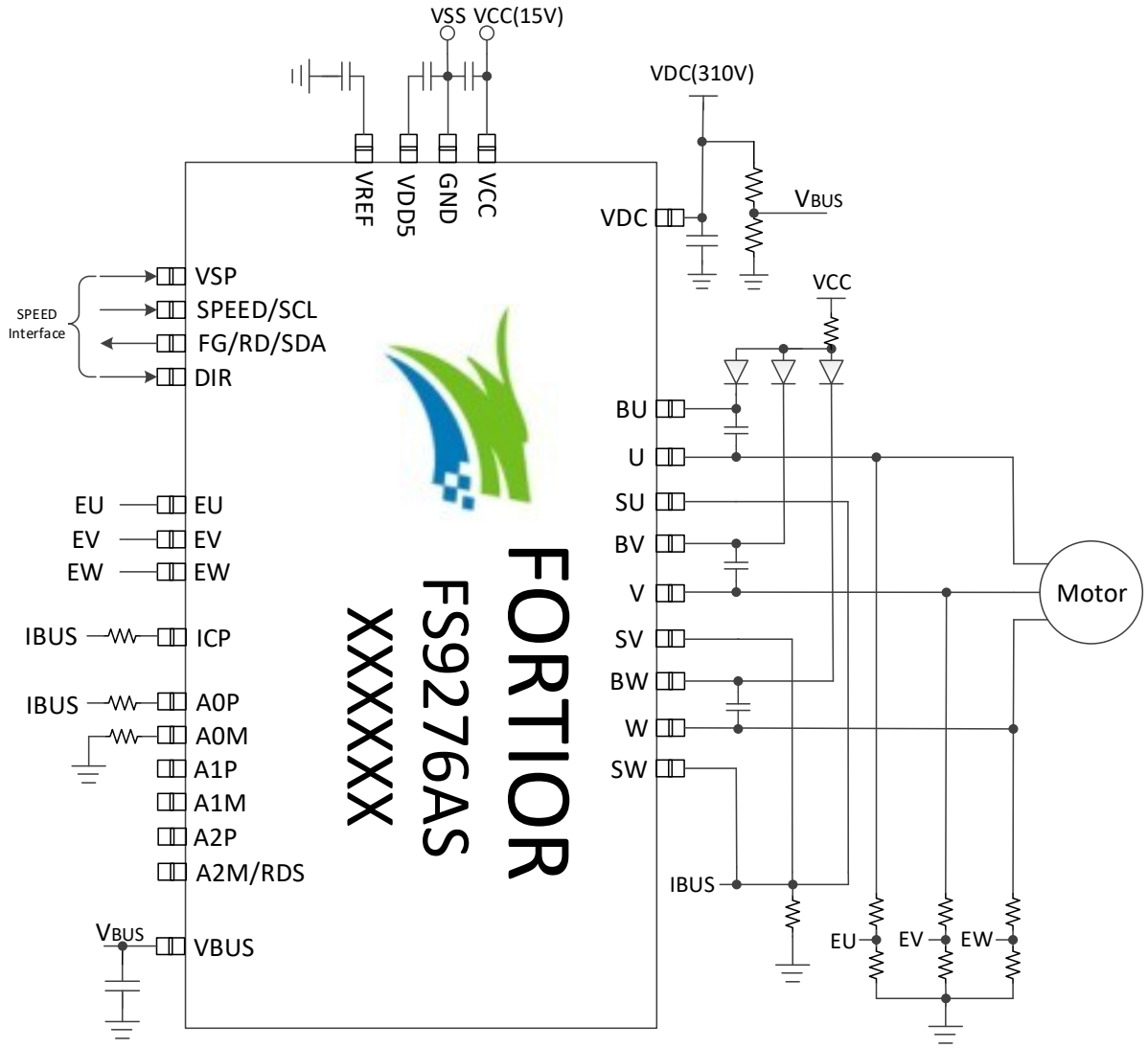


Figure 1-1 Sensorless FOC Mode with Single-shunt Differential Sampling

1.5.2 Sensorless FOC Mode with Dual-shunt Differential Sampling

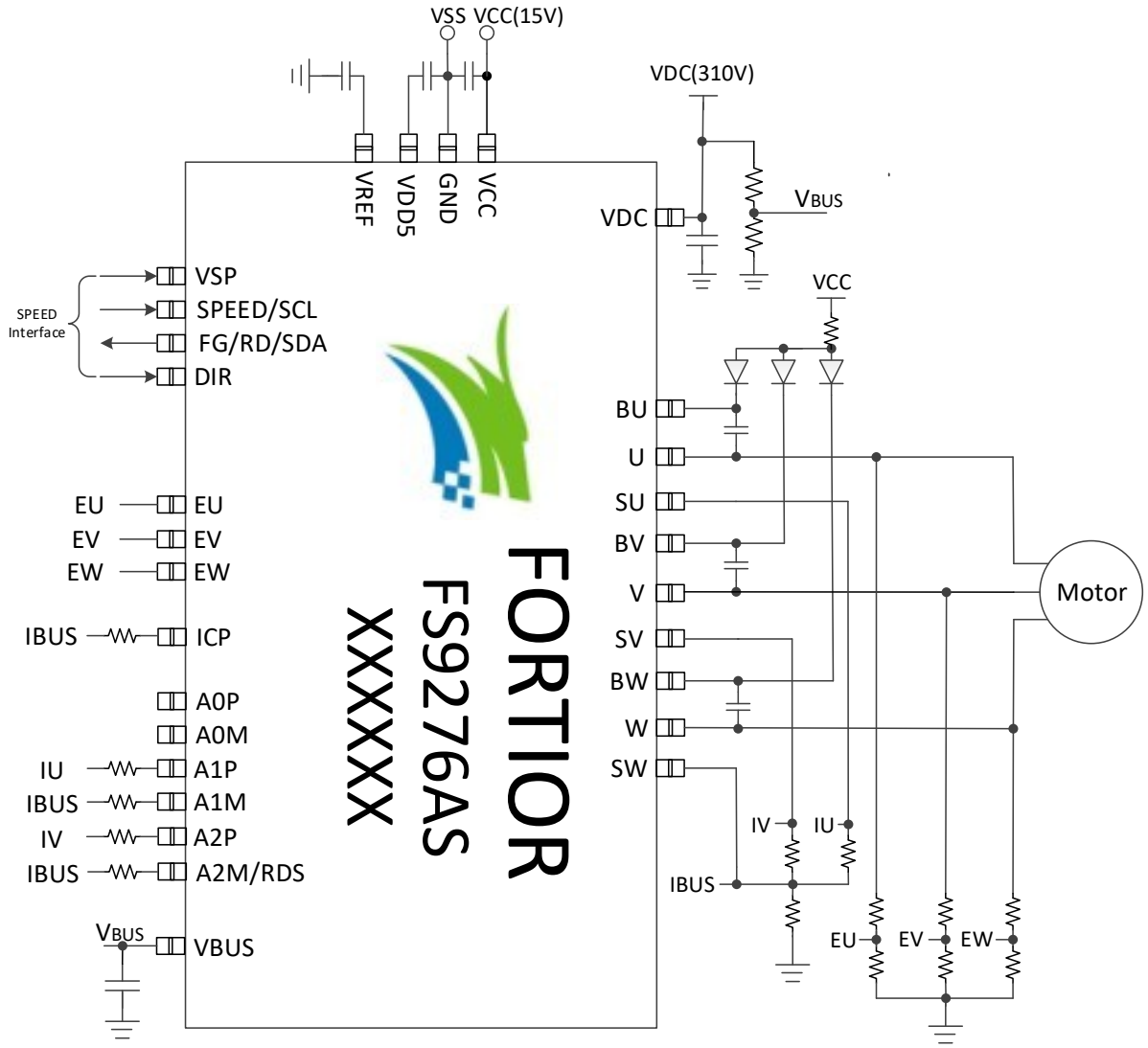


Figure 1-2 Sensorless FOC Mode with Dual-shunt Differential Sampling

1.5.3 Sensorless FOC Mode with Triple-shunt Differential Sampling

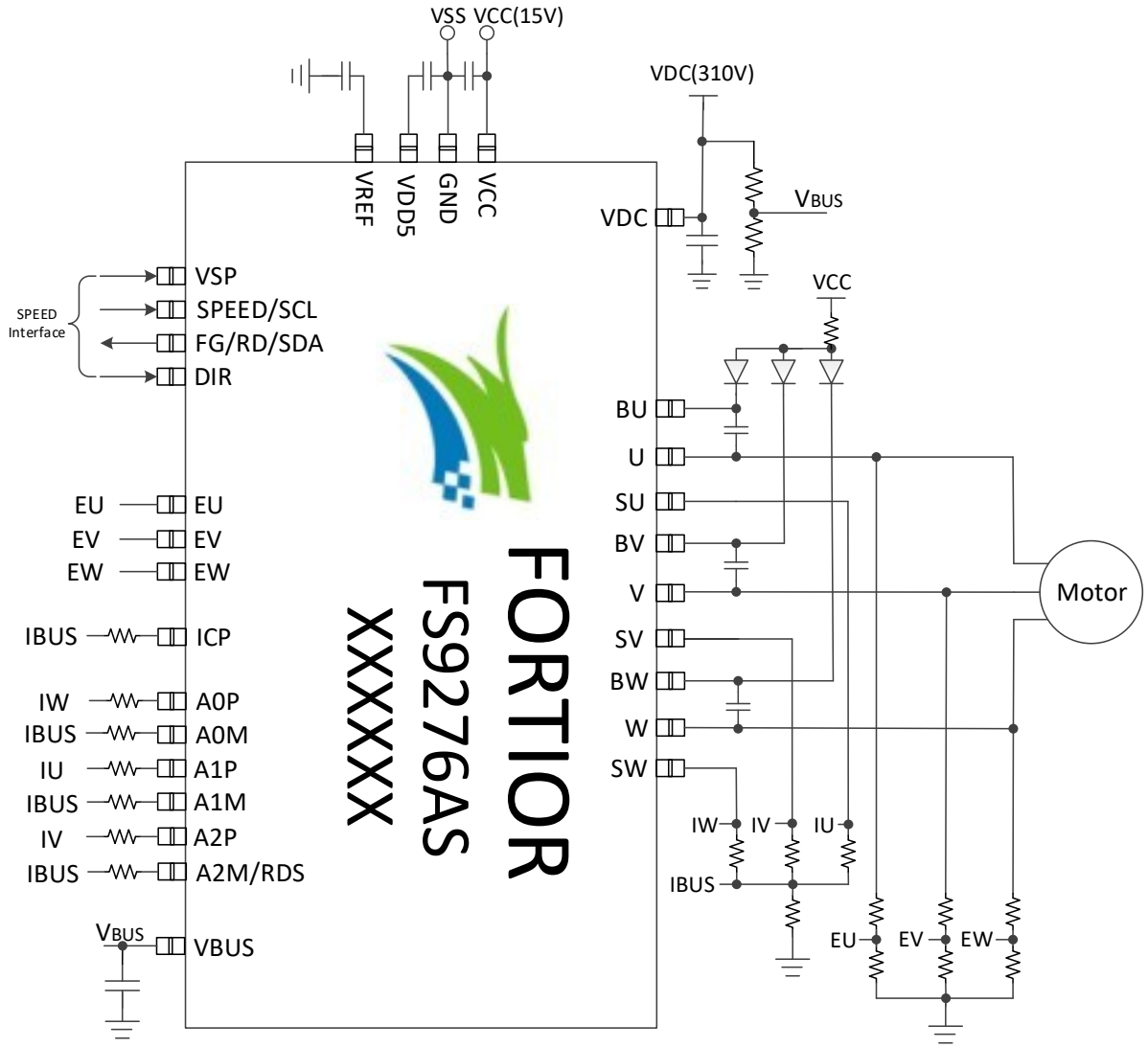


Figure 1-3 Sensorless FOC Mode with Triple-shunt Differential Sampling

1.6 Functional Block Diagram

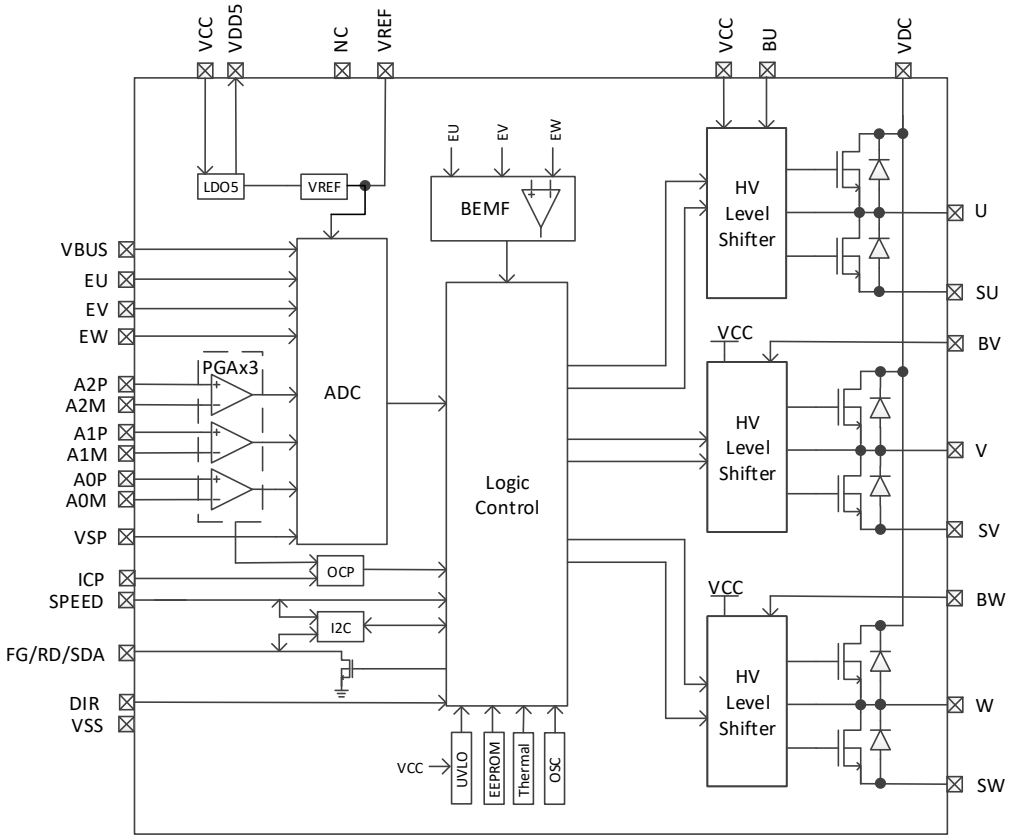


Figure 1-4 FS9276AS Functional Block Diagram

1.7 Pinout Diagram

1.7.1 FS9276AS SSOP A54-38

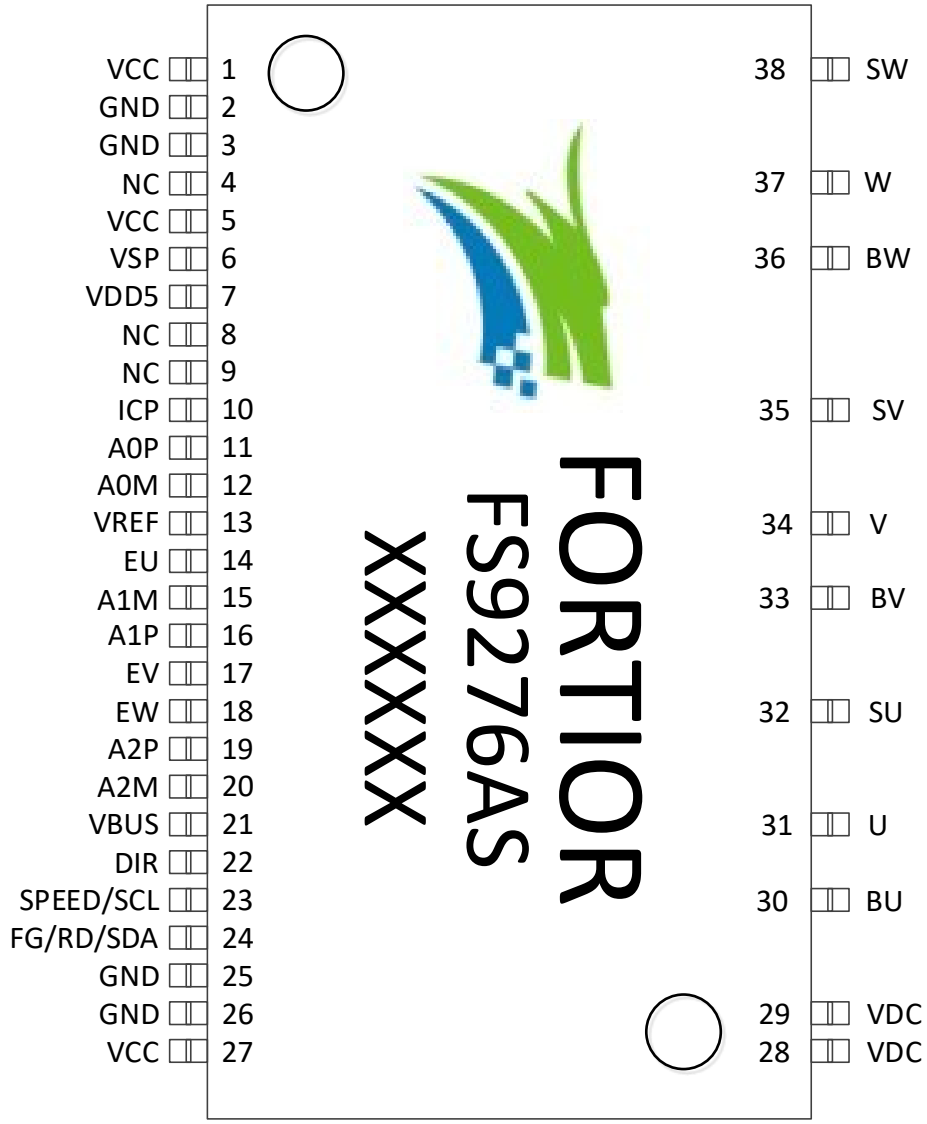


Figure 1-5 FS9276AS SSOP A54-38 Pinout Diagram

1.8 Pin Definitions

The IO types are defined as follows:

- DI = Digital Input
- DO = Digital Output
- DB = Digital Bidirectional
- AI = Analog Input
- AO = Analog Output
- P = Power Supply

1.8.1 FS9276AS SSOP A54-38

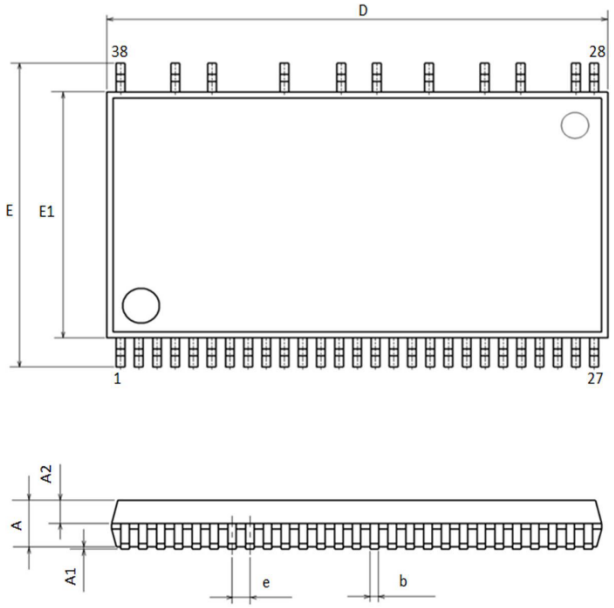
Table 1-1 FS9276AS SSOP A54-38 Pin Descriptions

Pin	FS9276AS SSOP A54-38	IO Type	Description
VCC	1	P	VCC
GND	2	P	Ground
GND	3	P	Ground
NC	4		Not connected
VCC	5	P	VCC
VSP	6	AI	Analog voltage input for motor speed regulation; Voltage range: 2.1V ~ 5.4V
VDD5	7	P	5V LDO output
NC	8		Not connected
NC	9		Not connected
ICP	10	AI	Over-current detection input
A0P	11	AI	AMP0 positive input
A0M	12	AI	AMP0 negative input
VREF	13	AO	ADC reference voltage output, with a 1μF external capacitor connected to ground
EU	14	AI	U-phase BEMF voltage input
A1M	15	AI	AMP1 negative input
A1P	16	AI	AMP1 positive input
EV	17	AI	V-phase BEMF voltage input
EW	18	AI	W-phase BEMF voltage input
A2P	19	AI	AMP2 positive input
A2M	20	AI	AMP2 negative input
VBUS	21	AI	VDC bus voltage input after voltage division
DIR	22	DI	Motor rotation control, with built-in pull-up resistor 1: Forward output phase sequence: U --> V --> W. 0: Reverse output phase sequence: U --> W --> V.

Pin	FS9276AS SSOP A54-38	IO Type	Description
SPEED/ SCL	23	DI/ DB	Speed control input; PWM speed regulation I^2C SCL
FG/ RD/ SDA	24	DO/ DO/ DB	Speed indication output, configured as collector open-drain output Motor block indication output, configured as collector open-drain output I^2C SDA, configured as collector open-drain output
GND	25	P	Ground
GND	26	P	Ground
VCC	27	P	VCC
VDC	28	P	High-voltage power supply
VDC	29	P	High-voltage power supply
BU	30	P	U-phase floating power supply. The voltage floats with respect to U-phase.
U	31	DO	U-phase output
SU	32	P	U-phase ground
BV	33	P	V-phase floating power supply. The voltage floats with respect to V-phase.
V	34	DO	V-phase output
SV	35	P	V-phase ground
W	36	DO	W-phase output
BW	37	P	W-phase floating power supply. The voltage floats with respect to W-phase.
SW	38	P	W-phase ground

2 Package Information

2.1 FS9276AS SSOP A54-38



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.00	2.10	2.20
A1	0.00	0.10	0.20
A2	0.95	1.05	1.25
b	0.37	0.38	0.39
c	0.17	0.27	0.37
D	21.80	22.00	22.20
E	13.80	14.10	14.40
E1	11.20	11.40	11.60
e	0.80(BSC)		
L	0.60	0.80	1.00
θ	0°	4°	10°

Figure 2-1 FS9276AS SSOP A54-38 Package Drawings and Dimensions

3 Ordering Information

Table 3-1 Model Selections

Model	Package	Power Supply (V)	Rdson (High Side + Low Side) (Ω)	Average Drive Current (A)	Control Features						Protection Features					Operation Temperature T_j (℃)	Lead-free
					Driver Type	Speed Regulation			Forward and Reverse Rotation	Initial Position Detection	OCP/CLP	TSD/LTP	Bus OVLO / UVLO	VCC/VB UVLO	MLP		
						I^2C	PWM	Analog Voltage									
FS9276AS	SSOP A54-38	13 ~ 20	2.2	2.5	Sensorless Sine-wave	√	√	√	√	√	√	√	√	√	√	-40 ~ 150	√

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings[1]

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET Drain-to-Source Voltage V_{DSS}		600	-	-	V
Continuous Drain Current $I_{DMAX(DC)}$ of Single MOS	T_C = 25°C	-	-	7[2]	A
Pulsed Drain Current $I_{DMAX(PLS)}$ of Single MOS	T_C = 25°C	-	-	28[2][3]	A
Power Dissipation P_d		-	-	3[4]	W
High-side VDC Supply Voltage V_{DC}		-0.3	-	600[2]	V
U/V/W-phase Output Voltage V_U,V_V,V_W		-0.3	-	600[2]	V
High-side Floating Absolute Voltage V_{BU},V_{BV},V_{BW}		-0.3	-	600[2]	V
High-side Floating Supply Voltage V_{BU} - V_U,V_{BV} - V_V,V_{BW} - V_W		-0.3	-	20	V
Storage Temperature T_{stg}		-55	-	150	℃
VCC to VSS Voltage		-0.3	-	25	V
VDD5 to VSS Voltage		-0.3	5	6.5	V
VSP to VSS Voltage		-0.3	-	VCC + 0.3	V
Other IOs to VSS Voltage (except VSP and VCC pins)		-0.3	-	VDD5 + 0.3	V

Notes:

[1] Stress values greater than "Absolute Maximum Ratings" listed above may cause irremediable damages to the device. These are stress ratings only, and it is NOT recommended to use your device in conditions that go beyond these stress ratings. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

[2] Power dissipation shall not exceed P_d or ASO;

[3] Pw ≤ 10μs and duty cycle ≤ 1%;

[4] The power dissipation is 24mW/°C at operating temperature of 25°C or above when the chip is mounted on a 70mm × 70mm × 1.6mm FR4 glass-epoxy circuit board with less than 3% copper foil.

4.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

(T_A = 25℃ unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage V_{DC}		-	310	400	V
High-side Floating Supply Voltage V_{BU} - V_U, V_{BV} - V_V, V_{BW} - V_W		13.5	15	16.5	V
Low-side Floating Supply Voltage V_{CC}		13.5	15	16.5	V
VREF/VDD5 Bypass Capacitance C_{VREG}		1.0	-	-	μF
Junction Temperature T_j		-	-	125	℃

Note: All voltages are specified with respect to the corresponding GND pin.

4.3 Global Electrical Characteristics

Table 4-3 Global Electrical Characteristics

(T_A = 25℃ and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Driver					
MOSFET Output					
Drain-to-Source Breakdown Voltage $V_{(BR)DSS}$	VSP = 0V	600	-	-	V
Drain-to-Source Leakage Current I_{DSS}	VSP = 0V, Single MOS	-	-	100	μA
Static Drain-to-Source On Resistance $R_{DS(ON)}$	V_{GS} = 10V, I_D = 3.5A	-	1.1	1.5	Ω
Drain-to-Source Diode Forward Voltage V_{SD}	T_j = 25°C, I_s = 7.0A, V_{GS} = 0V	-	-	1.4	V
Power Supply					
VB Quiescent Current I_{BBQ}	VSP = 0V, Single MOS	25	55	100	μA
VB Under-voltage Lockout					
VB Release Voltage V_{BUVH}	V_{BX} – V_X	11.5	10.1	10.7	V
VB Lockout Voltage V_{BUVL}	V_{BX} – V_X	10.5	9.1	9.7	V
Controller					
Power Supply					
VCC Operating Voltage		13	-	20	V
VDD5 Operating Voltage	T_A = -40°C ~ 85°C	4.8	5	5.2	V
VCC Operating Current I_{VCC}	T_A = -40°C ~ 85°C	-	15	25	mA
VDD5 Load Current	T_A = -40°C ~ 85°C	-	-	10	mA
VCC Sleep-mode Current $I_{VCC\text{-}sleep}$	VSP = 0V	-	0.5	1.0	mA
VCC Idling Current I_{Idle}		5	7	10	mA
Voltage Regulator Output Voltage V_{REG}	IO = -30mA	4.5	5.0	5.5	V
Monitor Output – FG					
High-level Output Voltage V_{MONH}	I_O = -2mA	VDD5 - 0.4	-	VDD5	V
Low-level Output Voltage V_{MONL}	I_O = 2mA	0	-	0.4	V
Phase Control					
Minimum Lead Angle P_{MIN}		-	0	-	deg
Maximum Lead Angle P_{MAX}		-	95	-	deg

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Carrier Oscillator					
Carrier Frequency F_{OSC}	Signal wave at 20k	18	20	22	kHz
Under-voltage Lockout (UVLO)					
VCC Release Voltage V_{CCUVH}		11.5	12.1	12.7	V
VCC Lockout Voltage V_{CCUVL}		10.5	11.1	11.7	V

4.4 IO Electrical Characteristics (DIR/SPEED/FG)

Table 4-4 IO Electrical Characteristics (DIR/SPEED/FG)

(T_A = 25℃ and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High-level Input Voltage V_{IH}		0.6*VDD5	-	-	V
Low-level Input Voltage V_{IL}		-	-	0.2*VDD5	V
SPEED/DIR Pull-up Resistor		-	33	-	kΩ
SPEED Pull-down Resistor		-	22	-	kΩ
EW/EV/EU Pull-up Resistor		-	5.6	-	kΩ

4.5 Speed Control with Analog Voltage

Table 4-5 Speed Control with Analog Voltage

(T_A = 25℃ and VCC = 15V unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VSP Speed Control Input Voltage Range		0	-	VCC	V
Control Pin Input Bias Current I_{SP}	V_{IN} = 5V	-	21	-	μA
Duty Cycle Controller Minimum Voltage V_{SPMIN}	V_{SPMIN} at 2.1V	1.8	2.1	2.4	V
Duty Cycle Controller Maximum Voltage V_{SPMAX}	V_{SPMIN} at 5.4V	5.1	5.4	5.7	V

4.6 Package Thermal Resistance

Table 4-6 SSOP A54-38 Package Thermal Resistance

Parameter	Test Conditions	Value	Unit
Junction-to-ambient Temperature Thermal Resistance θ_{JA}[1]		42.5	℃/W
Junction-to-package-top Thermal Resistance Ψ_{JT}		12.5	℃/W

Note:

[1] The actual measurements may vary depending on the conditions.

5 Function Description

5.1 VREF

VREF is applied to internal digital logic and analog circuits only, and cannot be used for external circuits. A capacitor of 1μF or above shall be added at VREF pin to stabilize the power supply.

5.2 DIR

Forward or reverse direction control (DIR) pin is used to reverse motor rotation by changing the DIR level. Pull-ups make the pin state as "High" (or "1") by default.

5.3 VSP

Speed control with analog voltage (VSP) pin can withstand up to VCC. When this feature is enabled, analog voltage is input to control motor speed.

5.4 SPEED

Speed control (SPEED) pin is used to input duty cycle for speed regulation depending on the settings. In addition, SPEED pin serves as the clock line (SCL) for I^2C communication.

5.5 FG

Speed detection and fault indication (FG/RD/SDA) pin is an open-drain output. When this pin is set to FG, it outputs speed feedback signal to indicate rotation speed of the motor, and when it is set to RD, it outputs high-level signal to indicate the fault state. In addition, the pin serves as the data line (SDA) for I^2C communication.

FG pin can implement FG4 (four pulses output in one mechanical cycle) and FG12 (12 pulses output in one mechanical cycle) as needed, and supports 4-pole-pair output conversion of 5-pole-pair motor.

Example: For a 5-pole-pair motor, 4 or 12 FG signals are displayed in one mechanical cycle.

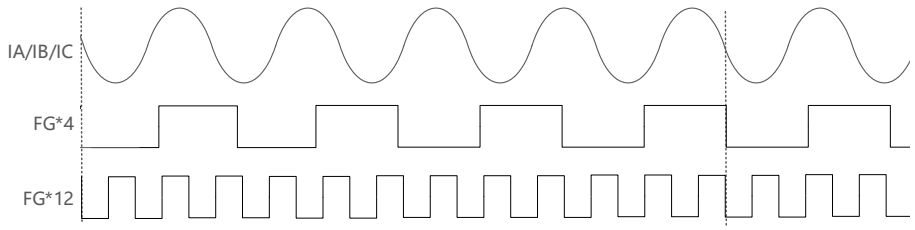


Figure 5-1 FG Output Diagram of 4-pole-pair Output of 5-pole-pair Motor

5.6 Speed Control

5.6.1 Speed Control Modes

The chip supports three types of speed control input interface: PWM, analog voltage and I^2C, and only one of them can be chosen at a time. If analog voltage is selected, voltage value input to the VSP pin controls the speed;

if PWM is selected, duty cycle of the PWM signal input to the SPEED pin controls the speed; and if I²C is selected, SPEED pin serves as the clock line (SCL) and FG pin as the data line (SDA).

5.6.2 Speed Control Curve

The control waveform is presented as below, where x-coordinate refers to the duty cycle of PWM input (In I²C control and analog control modes, the input can be converted to the corresponding PWM duty cycle.), and y-coordinate refers to the output duty cycle, which represents different physical quantities in different control modes.

The speed control curve is configured by setting the output duty cycle at the start and end points. The start point is determined by X_ON and Y_ON, and the end point by X_Max and Y_Max. The output of other points between them increases linearly as the input varies.

The y-coordinate represents Duty in voltage-loop control mode; Speed in speed-loop control mode; and Current in current-loop control mode.

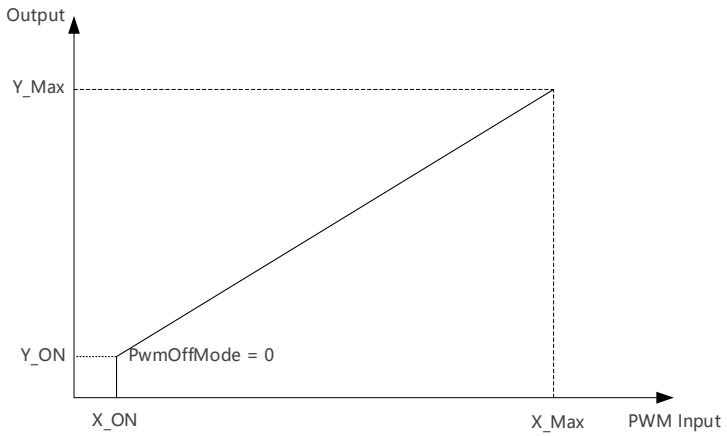


Figure 5-2 Speed Curve in Speed-loop or Current-loop Mode (PwmOffMode = 0)

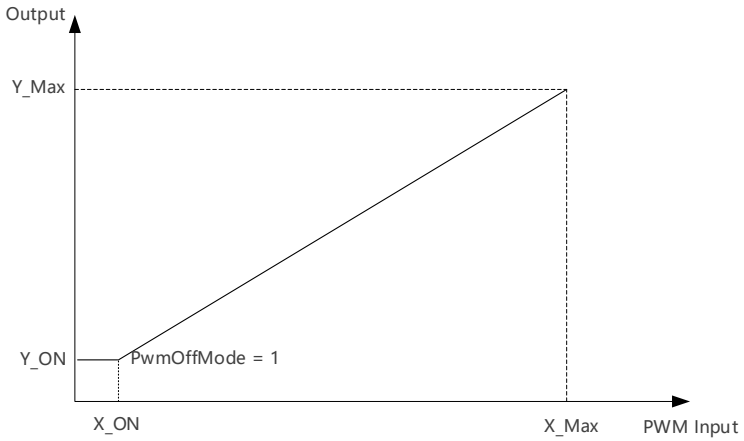


Figure 5-3 Speed Curve in Speed-loop or Current-loop Mode (PwmOffMode = 1)

5.7 Sleep Mode

The motor enters sleep mode in 6s after VSP is set to 0V and SPEED pin is connected to GND.

Wakeup conditions: In I^2C speed control mode, the chip exits sleep mode after receiving the matched I^2C ID. In PWM speed control mode, the chip exits sleep mode when a high-level voltage is input to SPEED pin. In analog voltage control mode, the chip exits sleep mode when the voltage of VSP pin is greater than 1.5V or when a high-level voltage is input to SPEED pin.

5.8 Soft-on

Soft-on feature gradually increases current during the start-up process, protecting the motor from abrupt startup and reducing noise during operation.

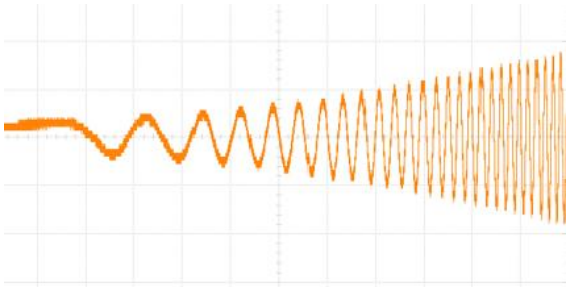


Figure 5-4 Soft-On Phase Current Waveform

5.9 Motor Lock Protection

Motor lock protection circuitry monitors operating state of the motor. When the conditions for motor lock are satisfied, the chip shuts down and waits for 20s to decide whether to restart (depending on software settings).

5.10 Phase Loss Protection

Phase loss protection circuitry monitors operating state of the motor. When the conditions for phase loss are satisfied, the chip shuts down and waits for 20s to decide whether to restart (depending on software settings).

5.11 Current Limiting Protection (CLP)

In sensorless FOC and current-loop control mode, the chip limits the maximum output current. In this mode, the noise is basically the same as that in normal operation mode.

5.12 Over-current Protection (OCP)

When the sampling current exceeds the over-current protection threshold, the chip shuts down and waits for 6s to decide whether to restart (depending on software settings).

5.13 Low Temperature Protection (LTP)

The chip is provided with an internal junction thermal sensor which can be configured to check against the configurable thermal limit. If it is enabled and triggered, the output torque is reduced, thereby reducing the

temperature and achieving thermal protection.

5.14 Temperature Sensor Detect (TSD)

The chip is provided with an internal junction thermal sensor. When it detects junction temperature exceeds the temperature threshold, the chip turns off the outputs unless the junction temperature drops back.

5.15 Configurable Maximum Speed Protection

As a means of protection, the maximum running speed can be clamped at a configurable limit.

This is particularly useful as motors may run at a significantly high speed at no-load condition. By limiting the running speed, the motor is effectively protected.

5.16 VCC Under-voltage Lockout (UVLO)

The chip turns off outputs and enters the under-voltage protection state when VCC voltage is lower than VCC UVLO lock voltage and VSP voltage is higher than the threshold voltage. The chip detects VCC voltage every 6s and releases the protection state until VCC voltage recovers to the normal operating level.

5.17 VDC Under-voltage/Over-voltage Lockout (UVLO/OVLO)

The chip turns off outputs and enters the under-voltage protection state or over-voltage protection state when VDC voltage (VDC bus voltage after voltage division) is lower than VDC UVLO lock voltage or higher than VDC OVLO lock voltage and VSP voltage is higher than the threshold voltage. It releases the protection state until VDC voltage recovers to the normal operating level.

6 Revision History

Rev.	Description	Date	Prepared By
V1.0	First release, translated from Chinese version 1.0	2023/12/07	Eric Deng

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Fortior Technology (Shenzhen) Co., Ltd.

Room 203, 2/F, Building No.11, Keji Central Road 2,
Software Park, High-Tech Industrial Park, Shenzhen, P.R. China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL: http://www.fortiortech.com

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