ISL9307

3MHz Dual 1500mA Step-Down Converters and Dual Low-Input LDOs

FN7931
Rev 3.00
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The ISL9307 is an integrated mini Power Management IC (mini-PMIC) ideal for applications for powering low-voltage microprocessor or multiple voltage rails with a battery as an input source, such as a single Li-ion or Li-polymer. ISL9307 integrates two high-efficiency, 3MHz, synchronous step-down converters (DCD1 and DCD2) and two low-input, low-dropout linear regulators (LDO1 and LDO2).

The 3MHz PWM switching frequency allows the use of very small external inductors and capacitors. Both step-down converters can enter skip mode under light load conditions to further improve efficiency and maximize battery life.

The ISL9307 features EN pins for each channel, thus allowing startup delay for power sequencing.

The ISL9307 also provides two 300mA low-dropout (LDO) regulators. The input voltage range is 1.5V to 5.5V, which allows them to be powered from one of the on-chip step-down converters or directly from a battery. The default LDO power-up output comes with factory pre-set fixed output voltage options between 0.9V and 3.3V.

The ISL9307 is available in a 4mmx4mm 16 Ld TQFN.

Features

- Dual 1500mA, Synchronous Step-down Converters and Dual 300mA, General-purpose LDOs
- Input Voltage Range
  - DCD1/DCD2 . . . . . 2.5V to 5.5V
  - VINLDO . . . . . 1.5V to 5.5V
- Adjustable Output Voltage
  - VODCD1/VODCD2 . . . . . 0.8V to V_{IN}
- 50µA I_Q (Typ) with DCD1/DCD2 in Skip Mode; 20µA I_Q (Typ) for each Enabled LDO
- EN Pins for DCD1/DCD2 and LDO1/LDO2
- Small, Thin, 4mmx4mm TQFN

Applications

- Cellular Phones, Smart Phones
- PDAs, Portable Media Players, Portable Instruments
- Single Li-ion/Li-polymer Battery-Powered Equipment
- DSP Core Power

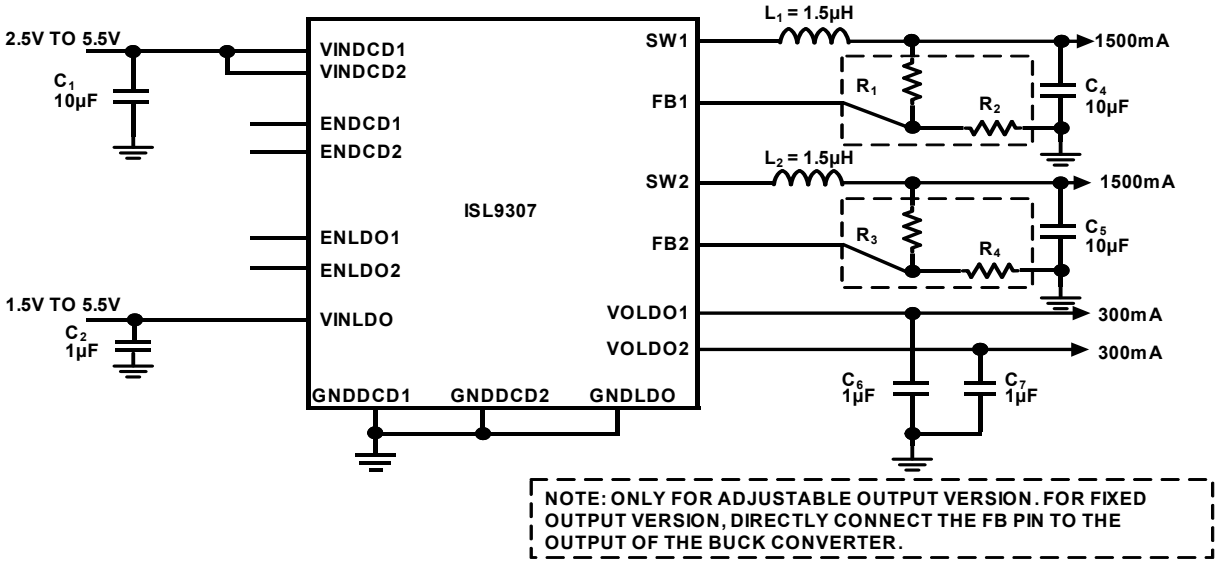
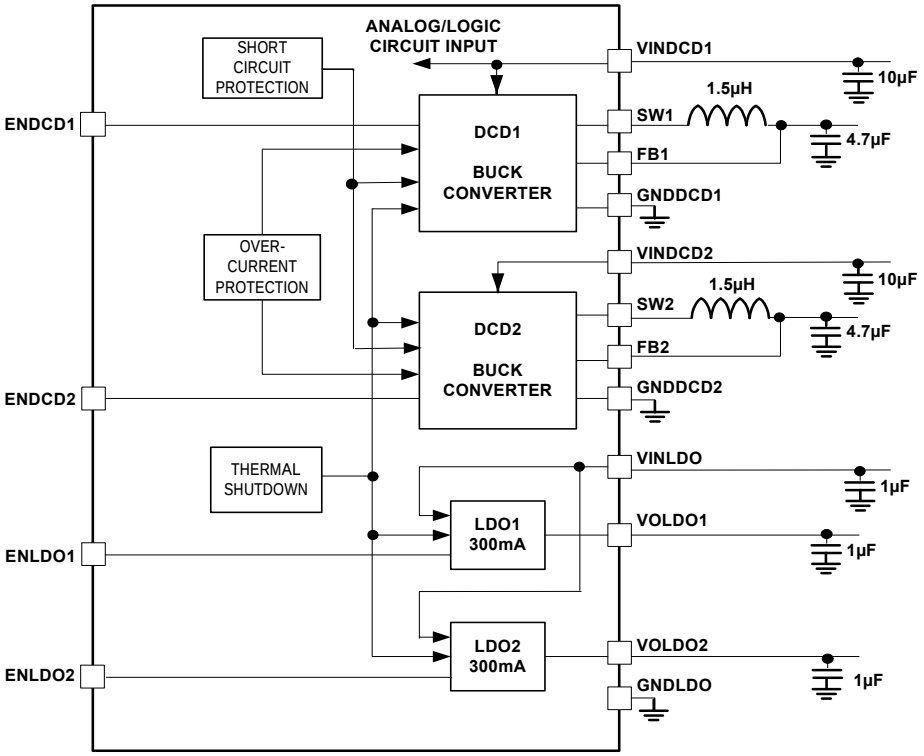


FIGURE 1. TYPICAL APPLICATION DIAGRAM

TABLE 1. TYPICAL APPLICATION PART LIST

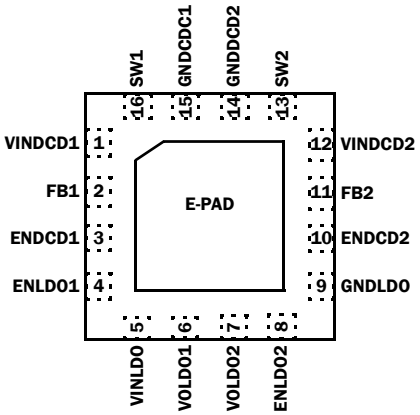
PARTS	DESCRIPTION	MANUFACTURER	PART NUMBER	SPECIFICATIONS	SIZE
L1, L2	Inductor	Sumida	CDRH2D14NP-1R5	1.5µH/1.80A/50mΩ	3.0mmx3.0mmx1.55mm
C1	Input capacitor	Murata	GRM21BR60J106KE19L	10µF/6.3V	0805
C2, C3	Input capacitor	Murata	GRM185R60J105KE26D	1µF/6.3V	0603
C4, C5	Output capacitor	Murata	GRM21BR60J106KE19L	4.7µF/6.3V	0805
C6, C7	Output capacitor	Murata	GRM185R60J105KE26D	10µF/6.3V	0603
R1, R2, R3, R4	Resistor	Various		1%, SMD, 0.1Ω	0603

Block Diagram



Pin Configuration

ISL9307
(16 LD 4X4 TQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER (TQFN)	NAME	DESCRIPTION
1	VINDCD1	Input voltage for buck converter DCD1 and power supply pin for all internal digital/ analog circuits.
2	FB1	Feedback pin for DCD1; connect external voltage divider resistors between DCDC1 output, this pin, and ground. For fixed output versions, connect this pin directly to the DCD1 output.
3	ENDCD1	Enable pin for DCD1. Tie high or low. Do not float.
4	ENLDO1	Enable pin for LDO1. Tie high or low. Do not float.
5	VINLDO	Input voltage for LDO1 and LDO2
6	VOLDO1	Output voltage of LDO1
7	VOLDO2	Output voltage of LDO2
8	ENLDO2	Enable pin for LDO2. Tie high or low. Do not float.
9	GNDLDO	Power ground for LDO1 and LDO2
10	ENDCD2	Enable pin for DCD2. Tie high or low. Do not float.
11	FB2	Feedback pin for DCD2; connect external voltage divider resistors between DCD2 output, this pin, and ground. For fixed output versions, connect this pin directly to the DCD2 output.
12	VINDCD2	Input voltage for buck converter DCD2
13	SW2	Switching node for DCD2; connect to one terminal of the inductor.
14	GNDDCD2	Power ground for DCD2
15	GNDDCD1	Power ground for DCD1
16	SW1	Switching node for DCD1; connect to one terminal of the inductor.
E-pad	E-pad	Exposed pad; connect to system ground.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	FBSEL DCD1 (V)	FBSEL DCD2 (V)	SLV LDO1 (V)	SLV LDO2 (V)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9307IRTAAJBZ-T	9307I AAJBZ	Adj	Adj	2.8	1.5	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJBZ-T7A	9307I AAJBZ	Adj	Adj	2.8	1.5	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJFZ-T	9307I AAJFZ	Adj	Adj	2.8	2.5	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJFZ-T7A	9307I AAJFZ	Adj	Adj	2.8	2.5	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJGZ-T	9307I AAJGZ	Adj	Adj	2.8	2.7	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJGZ-T7A	9307I AAJGZ	Adj	Adj	2.8	2.7	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJLZ-T	9307I AAJLZ	Adj	Adj	2.8	2.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJLZ-T7A	9307I AAJLZ	Adj	Adj	2.8	2.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJYZ-T	9307I AAJYZ	Adj	Adj	2.8	0.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJYZ-T7A	9307I AAJYZ	Adj	Adj	2.8	0.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANCZ-T	9307I AANCZ	Adj	Adj	3.3	1.8	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANCZ-T7A	9307I AANCZ	Adj	Adj	3.3	1.8	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANFZ-T	9307I AANFZ	Adj	Adj	3.3	2.5	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANFZ-T7A	9307I AANFZ	Adj	Adj	3.3	2.5	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANGZ-T	9307I AANGZ	Adj	Adj	3.3	2.7	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANGZ-T7A	9307I AANGZ	Adj	Adj	3.3	2.7	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANLZ-T	9307I AANLZ	Adj	Adj	3.3	2.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANLZ-T7A	9307I AANLZ	Adj	Adj	3.3	2.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANWZ-T	9307I AANWZ	Adj	Adj	3.3	1.2	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANWZ-T7A	9307I AANWZ	Adj	Adj	3.3	1.2	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANYZ-T	9307I AANYZ	Adj	Adj	3.3	0.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAANYZ-T7A	9307I AANYZ	Adj	Adj	3.3	0.9	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTWCNJZ-T	9307I WCNJZ	1.2	1.8	3.3	2.8	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTWCNJZ-T7A	9307I WCNJZ	1.2	1.8	3.3	2.8	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTWCWNZ-T	9307I WCWNZ	1.2	1.8	1.2	3.3	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTWCWNZ-T7A	9307I WCWNZ	1.2	1.8	1.2	3.3	-40 to +85	16 Ld TQFN	L16.4X4G
ISL9307IRTAAJBEV1Z	Evaluation Board							
ISL9307IRTAAJFEV1Z	Evaluation Board							
ISL9307IRTAAJGEV1Z	Evaluation Board							
ISL9307IRTAAJLEV1Z	Evaluation Board							
ISL9307IRTAAJYEV1Z	Evaluation Board							
ISL9307IRTAANCEV1Z	Evaluation Board							
ISL9307IRTAANFEV1Z	Evaluation Board							
ISL9307IRTAANGEV1Z	Evaluation Board							
ISL9307IRTAANLEV1Z	Evaluation Board							
ISL9307IRTAANWEV1Z	Evaluation Board							
ISL9307IRTAANYEV1Z	Evaluation Board							
ISL9307IRTWCNJEV1Z	Evaluation Board							
ISL9307IRTWCWNEV1Z	Evaluation Board							

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL9307. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings (Refer to Ground)

SW1, SW2 ..... -1.5V to 6.5V
FB1, FB2 ..... -0.3V to 3.6V
GNDDCD1, GNDDCD2, GNDLDO ..... -0.3V to 0.3V
All other pins ..... -0.3V to 6.5V
ESD Ratings
Human Body Model (Tested per JESD22-A114F) 3.5kV
Machine Model (Tested per JESD22-A115-A) 225V
Charged Device Model (Tested per JESD22-C101D) 2.2kV
Latch Up (Tested per JESD78B, Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
16 Ld TQFN Package (Note 4)	40.2

Maximum Junction Temperature Range ..... -40°C to +150°C
Recommended Junction Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

Recommended Operating Conditions

VINDCD1 ..... 2.5V to 5.5V
VINDCD2 ..... 2.3V to VINDCD1
VINLDO ..... 1.5V to VINDCD1
DCD1 and DCD2 Output Current ..... 0mA to 1500mA
LDO1 and LDO2 Output Current ..... 0mA to 300mA
Operating Ambient Temperature ..... -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, typical specifications are measured at the following conditions: T_A = +25°C, VINDCD1 = 3.6V, VINDCD2 = 3.3V. For LDO1 and LDO2, VINLDO = VOLDO + 0.5V to 5.5V with VINLDO always no higher than VINDCD1. $L_1 = L_2 = 1.5\mu H$, $C_1 = C_4 = C_5 = 10\mu F$, $C_2 = C_6 = C_7 = 1\mu F$, I_{OUT} = 0A for DCD1, DCD2, LDO1 and LDO2 (see Figure 1 on page 1 for more details). **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
VINDCD1, VINDCD2 Voltage Range			**2.5**	-	**5.5**	V
VINDCD1, VINDCD2 Undervoltage Lockout Threshold	V_{UVLO}	Rising	-	2.2	**2.3**	V
		Falling	**1.9**	2.1	-	V
Quiescent Supply Current on VINDCD1	I_{VIN1}	Only DCD1 enabled; no load and no switching on DCD1	-	40	**60**	µA
	I_{VIN2}	Only DCD1 and LDO1 enabled; no load and no switching on DCD1	-	60	**95**	µA
	I_{VIN3}	Both DCD1 and DCD2 enabled; no load and no switching on both DCD1 and DCD2	-	50	**75**	µA
	I_{VIN4}	Only LDO1 and LDO2 enabled	-	110	**130**	µA
	I_{VIN5}	DCD1, DCD2, LDO1 and LDO2 enabled; no load and no switching on both DCD1 and DCD2	-	135	**160**	µA
Shutdown Supply Current	I_{SD}	VINDCD1 = 5.5V; DCD1, DCD2, LDO1 and LDO2 disabled	-	0.15	**5**	µA
Thermal Shutdown			-	155	-	°C
Thermal Shutdown Hysteresis			-	30	-	°C
DCD1 AND DCD2						
FB1, FB2 Regulation Voltage	V_{FB}		**0.785**	0.8	**0.815**	V
FB1, FB2 Bias Current	I_{FB}	FB = 0.75V	-	0.001	-	µA
Output Voltage Accuracy		$V_{IN} = V_O$ + 0.5V to 5.5V (minimal 2.5V), 1mA load	**-3**	-	**+3**	%
Line Regulation		$V_{IN} = V_O$ + 0.5V to 5.5V (minimal 2.5V)	-	0.1	-	%/V
Maximum Output Current			**1500**	-	-	mA

Electrical Specifications Unless otherwise noted, typical specifications are measured at the following conditions: T_A = +25°C, VINDCD1 = 3.6V, VINDCD2 = 3.3V. For LDO1 and LDO2, VINLDO = VOLDO + 0.5V to 5.5V with VINLDO always no higher than VINDCD1. $L_1 = L_2 = 1.5\mu H$, $C_1 = C_4 = C_5 = 10\mu F$, $C_2 = C_6 = C_7 = 1\mu F$, I_{OUT} = 0A for DCD1, DCD2, LDO1 and LDO2 (see Figure 1 on page 1 for more details). **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
P-Channel MOSFET ON-resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.14	**0.20**	Ω
		V_{IN} = 2.3V, I_O = 200mA	-	0.24	**0.40**	Ω
N-Channel MOSFET ON-resistance		V_{IN} = 3.6V, I_O = 200mA	-	0.11	**0.20**	Ω
		V_{IN} = 2.3V, I_O = 200mA		0.18	**0.34**	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}		**2.1**	2.5	**2.75**	A
SW Maximum Duty Cycle			-	100	-	%
SW Leakage Current		V_{IN} = 5.5V	-	0.005	**1**	µA
PWM Switching Frequency	f_S		**2.6**	3.0	**3.4**	MHz
SW Minimum ON-time		V_{FB} = 0.75V	-	70	-	ns
Bleeding Resistor			-	115	-	Ω
LDO1 AND LDO2						
VINLDO Supply Voltage		No higher than VINDCD1	**1.5**	-	**5.5**	V
VINLDO Undervoltage Lock-out Threshold	V_{UVLO}	VINDCD1 = 2.3V, Rising	-	1.41	**1.46**	V
		VINDCD1 = 2.3V, Falling	**1.33**	1.37	-	V
Internal Peak Current Limit			**350**	425	**540**	mA
Dropout Voltage		I_O = 300mA, VO ≤ 2.1V	-	125	**250**	mV
		I_O = 300mA, 2.1V < VO ≤ 2.8V	-	100	**200**	mV
		I_O = 300mA, VO > 2.8V	-	80	**170**	mV
Power Supply Rejection Ratio		I_O= 300mA @ 1kHz, V_{IN} = 3.6V, VO = 2.6V, T_A = +25°C	-	55	-	dB
Output Voltage Noise		V_{IN} = 4.2V, I_O = 10mA, T_A = +25°C, BW = 10Hz to 100kHz	-	45	-	μV_{RMS}
ENABLE PIN LOGIC						
ENDCD1, ENDCD2, ENLDO1, ENLDO2 Pin Logic High			**1.4**			V
ENDCD1, ENDCD2, ENLDO1, ENLDO2 Pin Logic Low					**0.4**	V
Enable Pin Leakage Current				0.05	1	µA

NOTE:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Theory of Operation

DCD1 and DCD2

Both the DCD1 and DCD2 converters on ISL9307 use the peak-current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Both converters are able to supply up to 1500mA load current.

Under light load conditions, the device enters a pulse-skipping mode to minimize switching loss by reducing switching frequency. Figure 2 illustrates the skip mode operation.

A zero-cross sensing circuit monitors the current flowing through the SW node for zero crossing. When it is detected to cross zero for 16 consecutive cycles, the regulator enters skip mode. During the 16 consecutive cycles, the inductor current could be negative. The counter is reset to zero when the sensed current flowing through the SW node does not cross zero during any cycle within the 16 consecutive cycles.

Once the converter enters skip mode, the pulse modulation is controlled by an internal comparator while each pulse cycle remains synchronized to the PWM clock. The P-channel MOSFET is turned on at the rising edge of the clock and turned off when its current reaches ~20% of the peak current limit.

As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle-over-cycle. When the output voltage is sensed to reach 1.5% above its nominal voltage, the P-channel MOSFET is turned off immediately, and the inductor current is fully discharged to zero and stays at zero.

The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-channel MOSFET turns on again, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage is sensed to drop below 1.5% of its nominal voltage value, as shown in Figure 3.

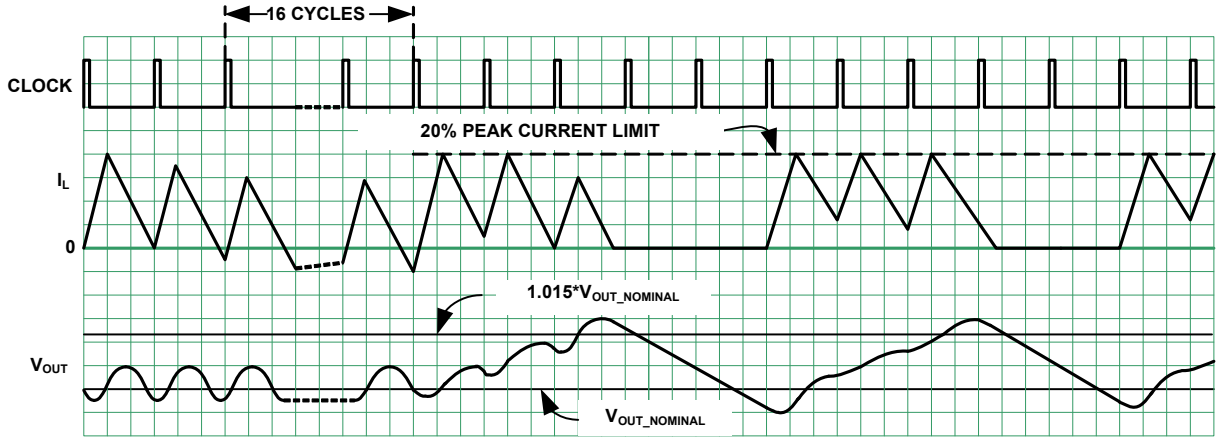


FIGURE 2. SKIP MODE OPERATION WAVEFORMS

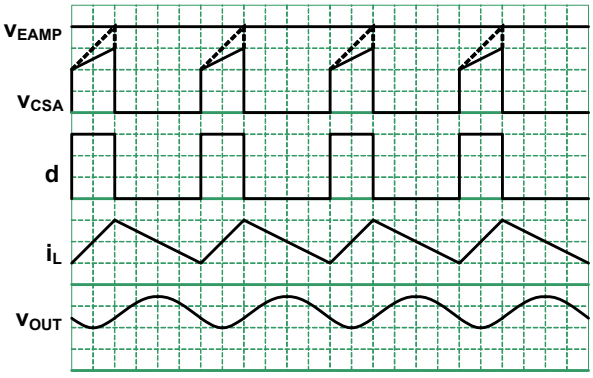


FIGURE 3. PWM OPERATION WAVEFORMS

Soft-Start

Soft-start reduces the in-rush current during the start-up stage. The soft-start block limits the current rising speed so that the output voltage rises in a controlled fashion.

Overcurrent Protection

The ISL9307 provides overcurrent protection for DCD1 and DCD2 for when an overload condition occurs. When the current at P-channel MOSFET is sensed to reach the current limit, the internal protection circuit is triggered to turn off the P-channel MOSFET immediately.

DCD Short-Circuit Protection

The ISL9307 provides short-circuit protection for both DCD1 and DCD2. The feedback voltage is monitored for output short-circuit protection. When the output voltage is sensed to be lower than a certain threshold, the internal circuit will change the PWM oscillator frequency to a lower frequenciy to protect the IC from damage. The P-channel MOSFET peak current limit remains active during this state.

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit is provided on ISL9307. The UVLO circuit block can prevent abnormal operation in the event that the supply voltage is too low to guarantee proper operation. The UVLO on VINDCD1 is set for a typical 2.2V with 100mV hysteresis. VINLDO is set for a typical 1.4V with 50mV hysteresis. When the input voltage is sensed to be lower than the UVLO threshold, the related channel is disabled.

Low Dropout Operation

Both DCD1 and DCD2 converters feature low dropout operation to maximize battery life. When the input voltage drops to a level at which the converter can no longer operate under switching regulation to maintain the output voltage, the P-channel MOSFET is completely turned on (100% duty cycle). The dropout voltage under such a condition is the product of the load current and the ON-resistance of the P-channel MOSFET. Minimum required input voltage (V_{IN}) under such a condition is the sum of output voltage plus voltage drop across the inductor and the P-channel MOSFET switch.

Active Output Voltage Discharge For DCD1, DCD2

The ISL9307 offers a feature to actively discharge the output voltage of DCD1 and DCD2 via an internal bleeding resistor (typical 115Ω) when the channel is disabled.

Thermal Shutdown

The ISL9307 provides a built-in thermal protection function with thermal shutdown threshold temperature set at +155°C with +25°C hysteresis (typical). When the die temperature is sensed to reach +155°C, the regulator is completely shut down, and as the temperature is sensed to drop to +130°C (typical), the device resumes normal operation, starting from soft-start.

Board Layout Recommendations

The ISL9307 is a high frequency switching charger and hence the PCB layout is a very important design practice to ensure a satisfactory performance.

The power loop is composed of the output inductor, L; the output capacitor, C_{OUT}; the SW pin; and the PGND pin. It is important to make the power loop as small as possible, and the connecting traces among them should be direct, short and wide. The same practice should be applied to the connection of the VIN pin; the input capacitor, C_{IN}; and PGND.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the voltage feedback trace and other noise-sensitive traces away from these noisy traces.

The input capacitor should be placed as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible as well. In addition, a solid ground plane is helpful for good EMI performance.

The ISL9307 employs a thermally enhanced TQFN package with an exposed pad. The exposed pad should be properly soldered onto the thermal pad of the board to remove heat from the IC. The thermal pad should be big enough for nine vias, as shown in Figure 4.

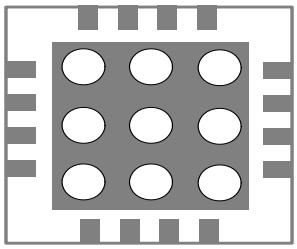


FIGURE 4. EXPOSED THERMAL PAD

Typical Operating Conditions

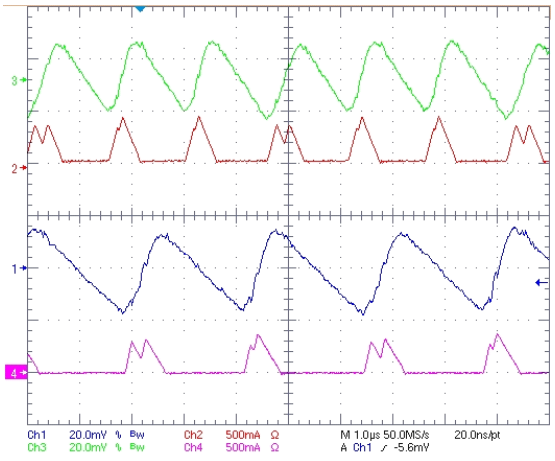


FIGURE 5. DCD OUTPUT RIPPLE (V_{IN} = 4.2V, PFM, TIME SCALE = 1µs) CH1: VODCD1 (20mV/DIV), CH2: IL1 (500mA/DIV), CH3: VODCD2 (20mV/DIV), CH4: IL2 (500mA/DIV)

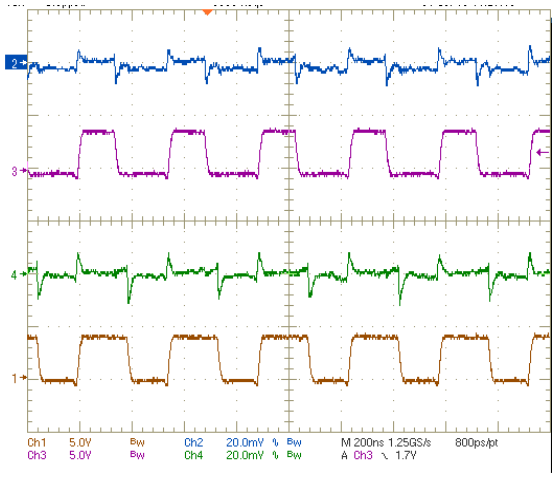


FIGURE 6. DCD OUTPUT RIPPLE (V_{IN} = 4.2V, FULL LOADING @ VODCD1 AND VODCD2, TIME SCALE = 200ns) CH1: SW1 (5V/DIV), CH2: VODCD1 (20mA/DIV), CH3: SW2 (5V/DIV), CH4: VODCD2 (20mA/DIV)

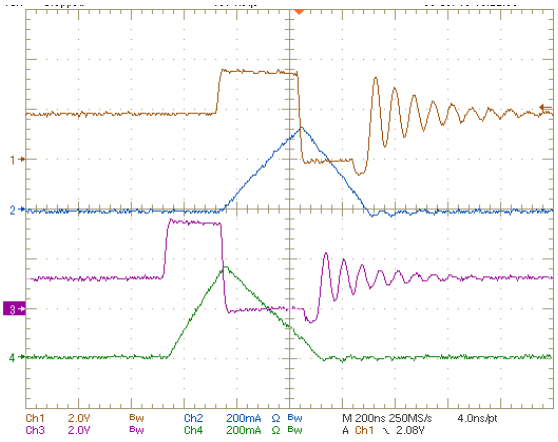


FIGURE 7. INDUCTOR CURRENT RIPPLE (V_{IN} = 3.6V, PFM, TIME SCALE = 200ns) CH1: SW1 (2V/DIV), CH2: IL1 (200mA/DIV), CH3: SW2 (2V/DIV), CH4: IL2 (200mA/DIV)

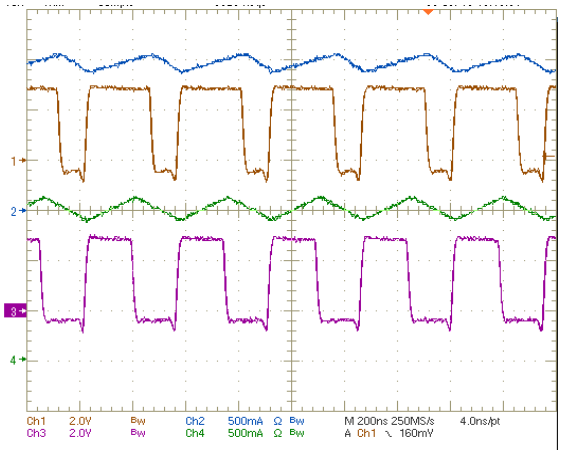


FIGURE 8. INDUCTOR CURRENT RIPPLE (V_{IN} = 3.6V, FULL LOADING, PWM, TIME SCALE = 200ns) CH1: SW1 (2V/DIV), CH2: IL1 (500mA/DIV), CH3: SW2 (2V/DIV), CH4: IL2 (500mA/DIV)

Typical Operating Conditions (Continued)

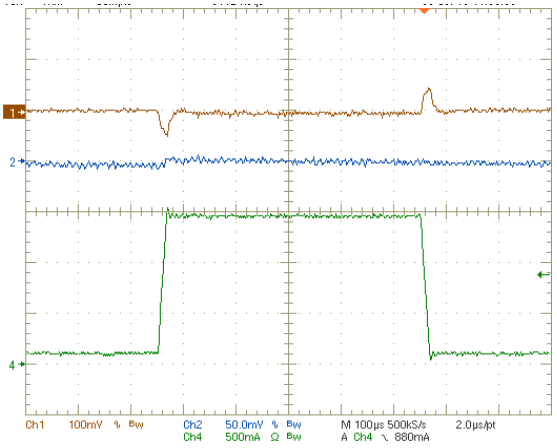


FIGURE 9. DCD1 TRANSIENT RESPONSE (V_{IN} = 3.6V, STEP LOAD: 150mA TO 1500mA) CH1: VODCD1 (100mV/DIV, AC), CH2: VODCD2 (50mV/DIV, AC, CH4: IL4 (500mA/DIV)

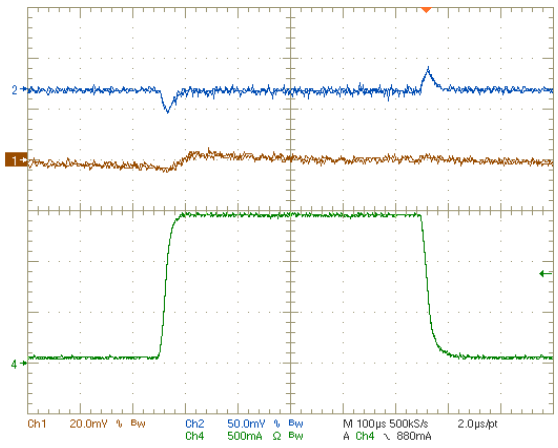


FIGURE 10. DCD2 TRANSIENT RESPONSE (V_{IN} = 3.6V, STEP LOAD: 150mA TO 1500mA) CH1: VODCD1 (100mV/DIV, AC), CH2: VODCD2 (50mV/DIV, AC, CH4: IL4 (500mA/DIV)

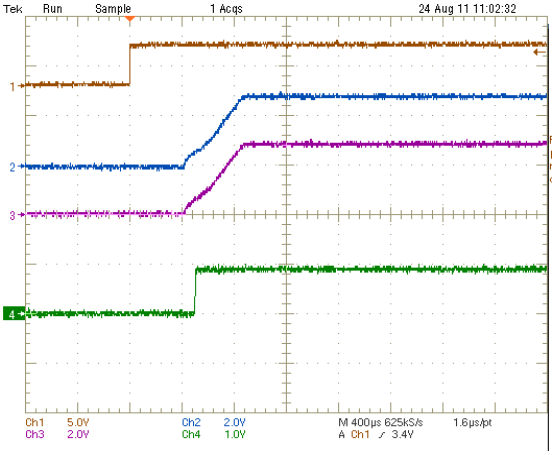


FIGURE 11. ENABLE WAVEFORM CH1: ENDCD1/ENDCD2/ENLD01/ENLD02 (5V/DIV), CH2: VODCD1: (2V/DIV), CH3: VODCD2 (2V/DIV), CH4: VOLD01 (1V/DIV)

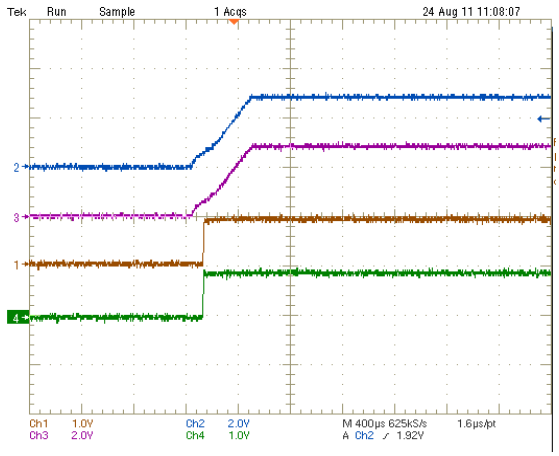


FIGURE 12. 4-CHANNEL POWER-UP AFTER ENABLE CH1: VOLD01 (1V/DIV), CH2: VODCD1 (2V/DIV), CH3: VODCD2 (2V/DIV), CH4: VOLD02 (1V/DIV)

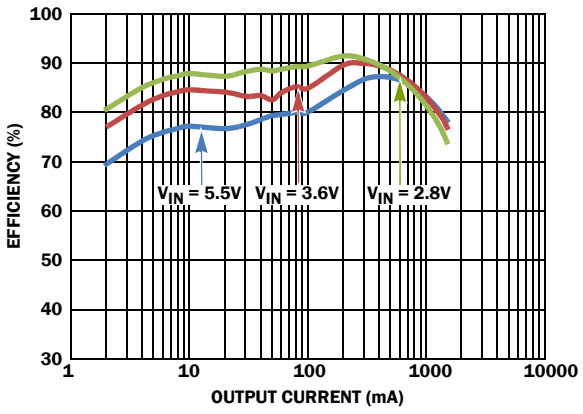


FIGURE 13. EFFICIENCY vs LOAD (V_{OUT} = 1.8V, PFM/PWM)

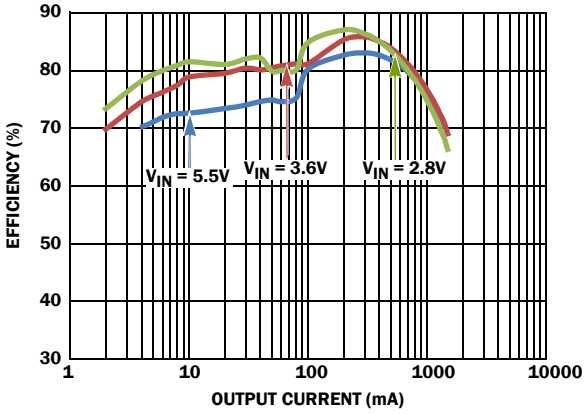


FIGURE 14. EFFICIENCY vs LOAD (V_{OUT} = 1.2V, FORCED PWM)

Typical Operating Conditions (Continued)

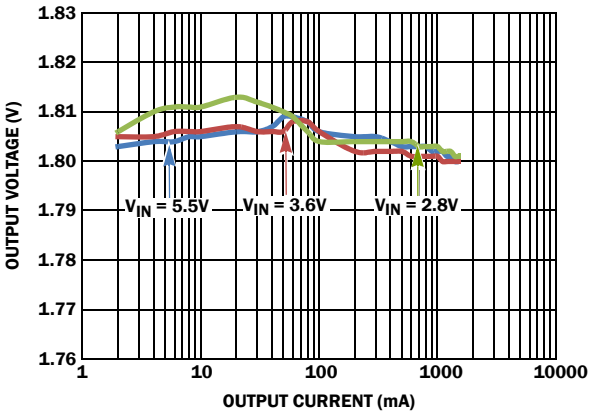


FIGURE 15. DCD OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{OUT} = 1.8V, PFM/PWM)

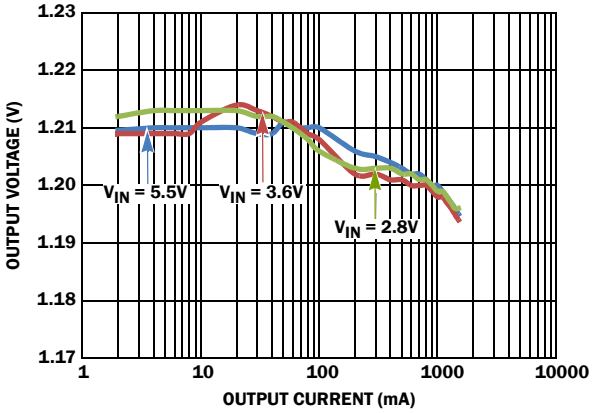


FIGURE 16. DCD OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{OUT} = 1.2V, PFM/PWM)

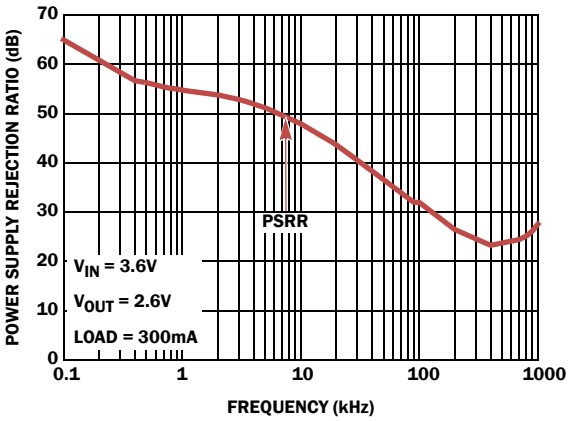


FIGURE 17. RIPPLE REJECTION RATIO vs FREQUENCY

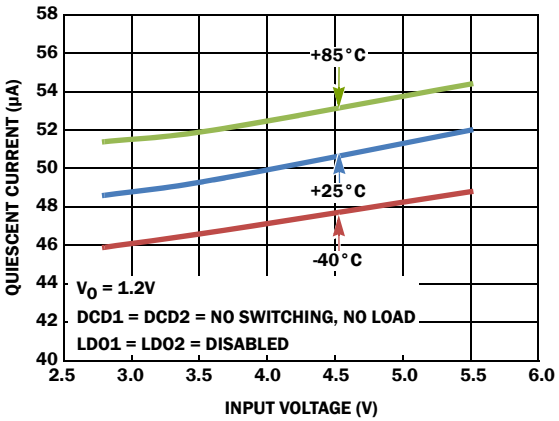


FIGURE 18. QUIESCENT CURRENT vs INPUT VOLTAGE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 24, 2012	FN7931.3	Page 5 - Abs Max Ratings, ESD Ratings changed from: Machine Model (Tested per JESD22-A115-A). . . . . .2.2kV Charged Device Model (Tested per JESD22-C101D). . .225V to: Machine Model (Tested per JESD22-A115-A). . . . . .225V Charged Device Model (Tested per JESD22-C101D). . .2.2kV
February 24, 2012	FN7931.2	Initial Release to web.

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Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

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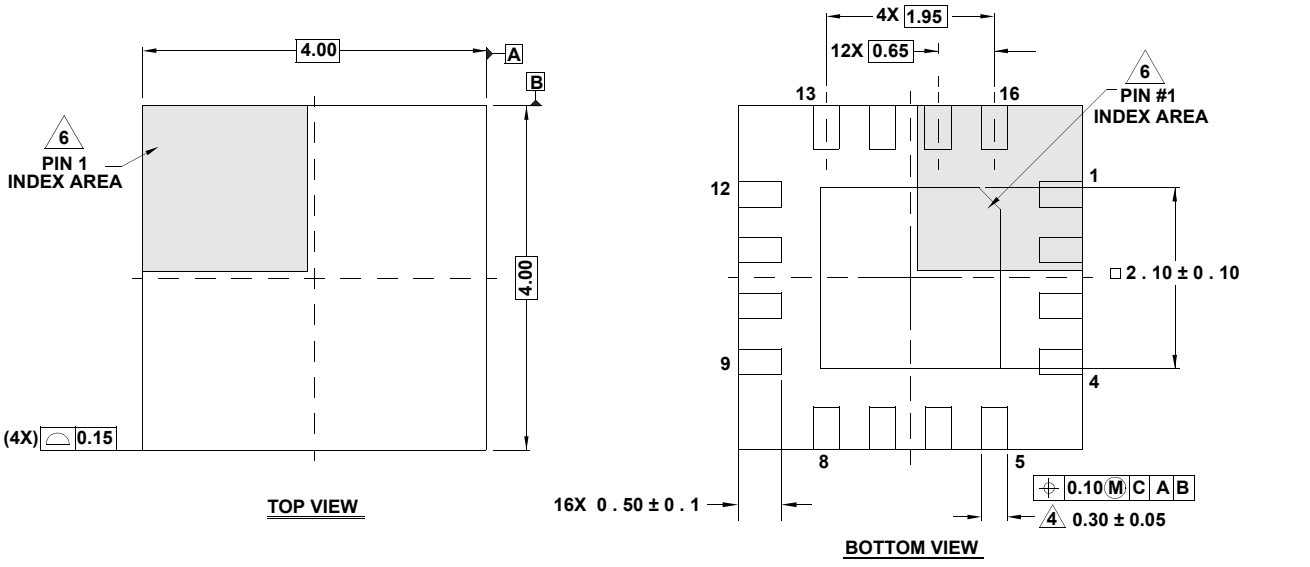
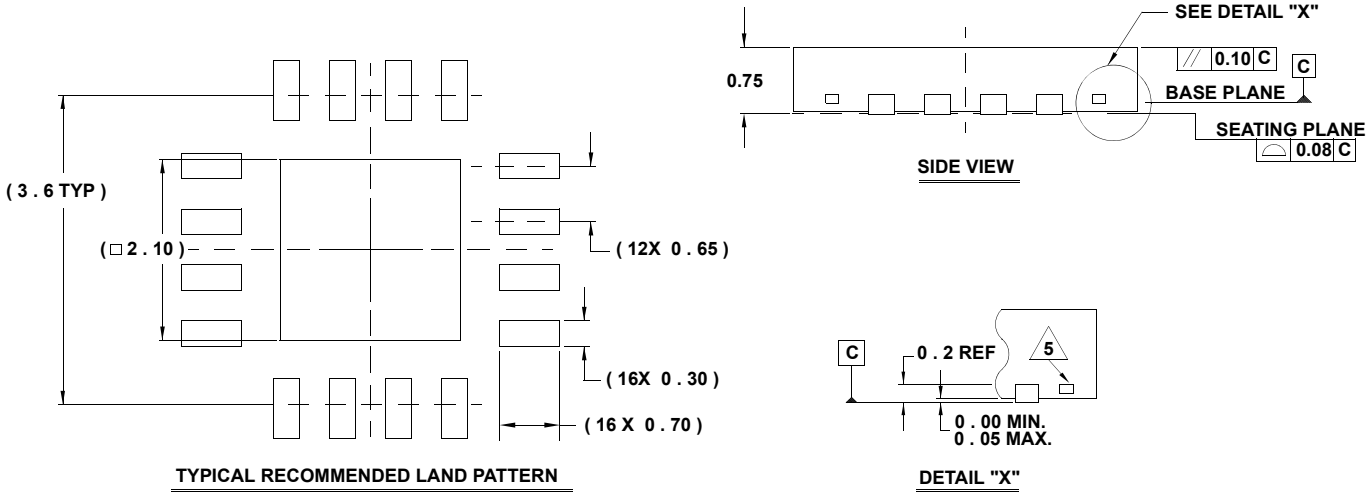
FITs are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing

L16.4x4G

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 4/10





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO220K.