LC05732ARA

Battery Protection IC, Integrated Power MOSFET, 1-Cell Lithium-Ion Battery

Overview

The LC05732ARA is a protection IC for 1−cell lithium−ion batteries with integrated power MOS FET. Also it integrates highly accurate detection circuits and detection delay circuits to prevent batteries from over−charging, over−discharging, over−current discharging and over−current charging.

In addition, main system can execute the power−on reset of itself by turning off the charge FET and discharge FET of LC05732ARA for a certain time period, with a reset signal.

A battery protection system can be made by only LC05732ARA and few external parts.

Features

- Charge−and−Discharge Power MOSFET are Integrated at $T_A = 25°C$, $V_{CC} = 4.0$ V
  - ON Resistance (Total of Charge and Discharge) 4.8 mΩ (typ)
- Highly Accurate Detection Voltage/Current at $T_A = 25°C$, $V_{CC} = 3.7$ V

♦ Over−Charge Detection	±25 mV
♦ Over−Discharge Detection	±50 mV
♦ Charge Over−Current Detection	±0.7 A
♦ Discharge Over−Current Detection	±0.7 A

- Delay Time for Detection and Release (Fixed Internally)
- Discharge/Charge Over−Current Detection is Compensated for Temperature Dependency of Power FET
- 0 V Battery Charging: "Inhibit"
- Auto Wake−up Function Battery Charging: "Inhibit"
- Forcible Charge−FET and Discharge−FET OFF Mode
  RSTB>VDD*0.9: Charge−FET and Discharge−FET = ON
  RSTB<VDD*0.1: Charge−FET and Discharge−FET = OFF
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Smart Phone
- Tablet
- Wearable Device

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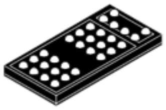


ECP30, 1.97x4.01
SUFFIX
CASE 971BC

MARKING DIAGRAM

XXXXX
AYYWW

A = Assembly Location
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LC05732A02RATBG	ECP30 (Pb−Free)	5000 / Tape & Reel
LC05732A03RATBG	ECP30 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C (Notes 1, 2, 3, 5)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VCC	Between PAC+ and VCC : R1 = 680 Ω	–0.3 to 12.0	V
S1 − S2 voltage	VS1−S2		20.0	V
CS terminal Input voltage	CS		V_{CC}–20.0 to V_{CC}+0.3	V
RSTB input voltage	RSTB		–0.3 to 7	V
Storage temperature	Tstg		–55 to +125	°C
Operating ambient temperature	Topr		–40 to +100	°C
Allowable power dissipation	Pd	(Note 4)	800	mW
Junction temperature	T_J		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute maximum ratings represent the values which cannot be exceeded at any given time
2. If you intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for confirmation
3. This device is made for power applications.
4. JESD 51−3 (1S)
5. Please execute appropriate test and take safety measures on your board.

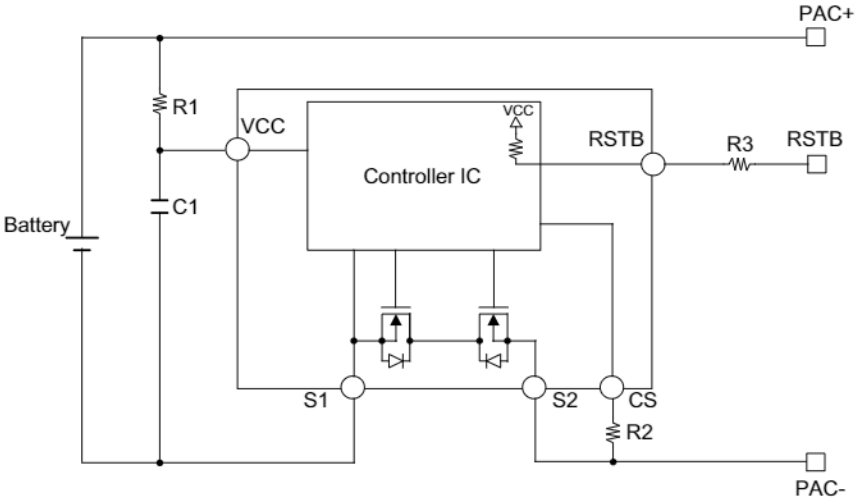


Figure 1. Example of Application Circuit

Components	Min	Recommended Value	Max	Unit	Description
R1	330	680	1k	Ω	
R2	680	1k	2k	Ω	
R3	680	1k	2k	Ω	
C1	0.1μ	1.0μ	2.2μ	F	

*We don't guarantee the characteristics of the circuit shown above.

ELECTRICAL CHARACTERISTICS (Notes 6, 7, 8, 9)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
DETECTION VOLTAGE							
Over−charge detection voltage	Vov	R1 = 680 Ω	TA = 25°C	Vov_set −25	Vov_set	Vov_set +25	mV
			TA = −30 to 70°C	Vov_set −30	Vov_set	Vov_set +30	
Over−charge release voltage	Vovr	R1 = 680 Ω	TA = 25°C	Vovr_set −40	Vovr_set	Vovr_set +40	mV
			TA = −30 to 70°C	Vovr_set −70	Vovr_set	Vovr_set +70	
Over−discharge detection voltage	Vuv	R1 = 680 Ω	TA = 25°C	Vuv_set −50	Vuv_set	Vuv_set +50	mV
			TA = −30 to 70°C	Vuv_set −80	Vuv_set	Vuv_set +80	
Over−discharge release voltage	Vuvr	R1=680 Ω CS =0V	TA = 25°C	Vuvr_set −100	Vuvr_set	Vuvr_set +100	mV
			TA = −30 to 70°C	Vuvr_set −120	Vuvr_set	Vuvr_set +120	
Discharge over−current detection current	Ioc	R2 = 1 kΩ	TA = 25°C V_{CC} = 3.7 V	Ioc_set −0.7	Ioc_set	Ioc_set +0.7	A
			TA = −30 to 70°C V_{CC} = 3.7 V	Ioc_set −1.2	Ioc_set	Ioc_set +1.2	
Discharge over−current detection current2 (Short circuit)	Ioc2	R2 = 1 kΩ	TA = 25°C V_{CC} = 3.7 V	Ioc2_set*0.8	Ioc2_set	Ioc2_set*1.2	A
			TA = −30 to 70°C V_{CC} = 3.7 V	Ioc2_set*0.6	Ioc2_set	Ioc2_set*1.8	
Charge over−current detection current	Ioch	R2 = 1 kΩ	TA = 25°C V_{CC} = 3.7 V	Ioch_set −0.7	Ioch_set	Ioch_set +0.7	A
			TA = −30 to 90°C V_{CC} = 3.7 V	Ioch_set −1.2	Ioch_set	Ioch_set +1.2	
RESET TERMINAL							
High−Level Input Voltage	VIH		TA = −30 to 90°C	0.9*V_{CC}			V
Low−Level Input Voltage	VIL		TA = −30 to 90°C			0.1*V_{CC}	V
High−Level Input Leakage Current	IIH	V_{CC} = RSTB	TA = −30 to 90°C			1	μA
Low−Level Input Leakage Current	IIL	V_{CC} = 3.7 V RSTB = 0 V	TA = −30 to 90°C	20	34	48	μA
Reset pulse width	Tw_res	V_{CC} = 2.2 to 4.3 V	TA = −30 to 90°C	10	20	30	ms
INPUT VOLTAGE							
0 V battery charging inhibition battery voltage	Vinh		TA = 25°C	0.4	0.9	1.4	V
CURRENT CONSUMPTION							
Operating current	ICC	At normal state	TA = 25°C V_{CC} = 3.7 V		3	6	μA
Shut down current	Ishut	At shut down state	TA = 25°C V_{CC} = 2.0 V			0.1	μA
RESISTANCE							
ON resistance 1 of integrated power MOSFET	Ron1	V_{CC} = 3.1 V I = ±2.0 A	TA = 25°C	4.4	5.4	6.9	mΩ
ON resistance 2 of integrated power MOS FET	Ron2	V_{CC} = 3.8 V I = ±2.0 A	TA = 25°C	4	4.9	5.8	mΩ
ON resistance 3 of integrated power MOSFET	Ron3	V_{CC} = 4.0 V I = ±2.0 A	TA = 25°C	3.9	4.8	5.7	mΩ

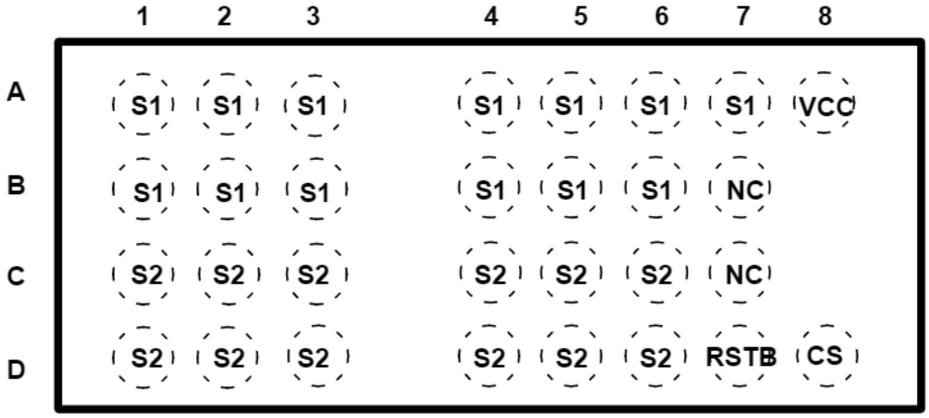
ELECTRICAL CHARACTERISTICS (Notes 6, 7, 8, 9)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
RESISTANCE							
ON resistance 4 of integrated power MOSFET	Ron4	V_{CC} = 4.5V I = ±2.0 A	TA = 25°C	3.8	4.7	5.6	mΩ
Internal resistance (VCC−CS)	Rcsu	V_{CC} = Vuv_set CS = 0 V	TA = 25°C		300		kΩ
Internal resistance (VSS−CS)	Rcsd	V_{CC} = 3.7 V CS = 0.1 V	TA = 25°C		10		kΩ
Forward Source to Source Voltage	Vf(s−s)	V_{CC} = 2.0 V Is = 0.25 A	TA = 25°C		0.67	1.06	V
DETECTION AND RELEASE DELAY TIME							
Over−charge detection delay time	Tov		TA = 25°C	0.8	1	1.2	s
			TA = −30 to 70°C	0.6	1	1.5	
Over−charge release delay time	Tovr		TA = 25°C	12.8	16	19.2	ms
			TA = −30 to 70°C	9.6	16	24	
Over−discharge detection delay time	Tuv		TA = 25°C	14	20	26	ms
			TA = −30 to 70°C	12	20	30	
Over−discharge release delay time	Tuvr		TA = 25°C	0.9	1.1	1.3	ms
			TA = −30 to 70°C	0.6	1.1	1.5	
Discharge over−current detection delay time 1	Toc1	V_{CC} = 3.7 V	TA = 25°C	9.6	12	14.4	ms
			TA = −30 to 70°C	7.2	12	18	
Discharge over−current release delay time 1	Tocr1	V_{CC} = 3.7 V	TA = 25°C	3.2	4	4.8	ms
			TA = −30 to 70°C	2.4	4	6	
Discharge over−current detection delay time 2 (Short circuit)	Toc2	V_{CC} = 3.7 V	TA = 25°C	230	300	420	μs
			TA = −30 to 70°C	200	300	450	
Charge Over−current detection delay time	Toch	V_{CC} = 3.7 V	TA = 25°C	12.8	16	19.2	ms
			TA = −30 to 90°C	9.6	16	24	
Charge Over−current release delay time	Tochr	V_{CC} = 3.7 V	TA = 25°C	3.2	4	4.8	ms
			TA = −30 to 90°C	2.4	4	6	
Reset release time	Tres	V_{CC} = 3.7 V	TA = 25°C	0.8	1	1.2	s
			TA = −30 to 70°C	0.6	1	1.5	

6. This device is made for power applications.
7. Please execute appropriate test and take safety measures on your board.
8. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
9. The specification in this parameter and all specification at high and low temperature are guaranteed by design.

SELECTION GUIDE

Device	Vov (V)	Vovr (V)	Vuv (V)	Vuvr (V)	Ioc (A)	Ioch (A)	Ioc2 (A)	Tuv (ms)	Reset Function
LC05732A02RATBG	4.475	4.475	2.1	2.1	7.0	9.0	25.0	20	Enable
LC05732A03RATBG	4.500	4.300	2.3	2.3	9.0	6.0	15.0	20	Disable



TOP VIEW

Figure 2. Pin Functions

Pin No.	Symbol	Pin Function	Description
A1−7 B1−6	S1	Source 1	Negative power input
A8	VCC	VCC terminal	
C1−6 D1−6	S2	Source 2	
D7	RSTB	Charge and discharge off control terminal (“L” = Reset)	Connected to VCC with 100 kΩ
D8	CS	Charger minus voltage input terminal	
B7,C7	NC	Non connection	

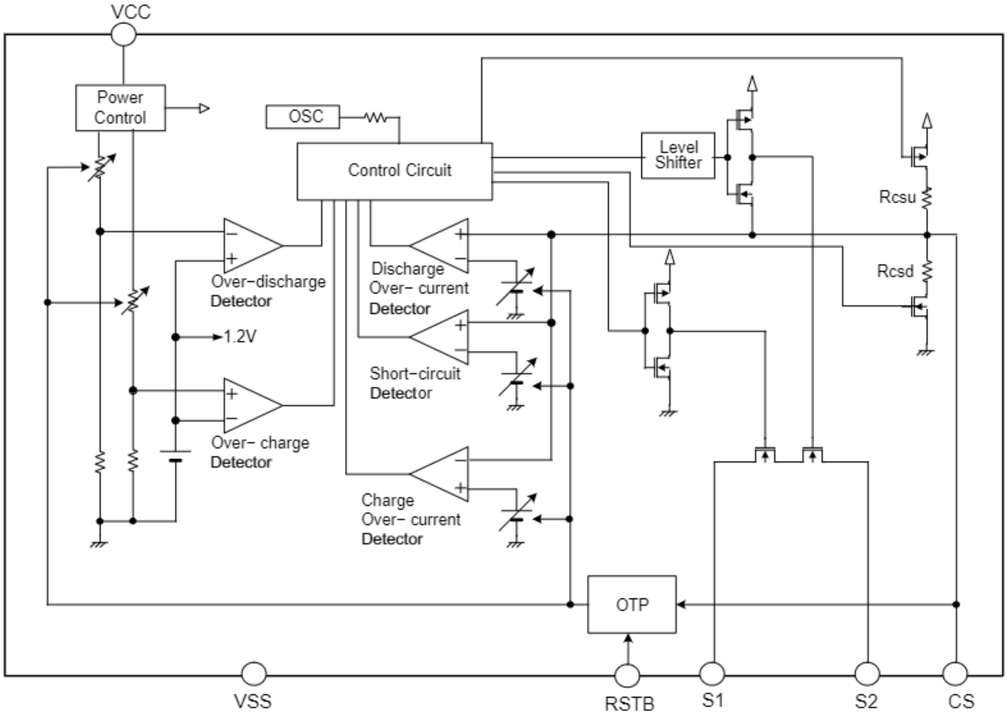


Figure 3. Block Diagram

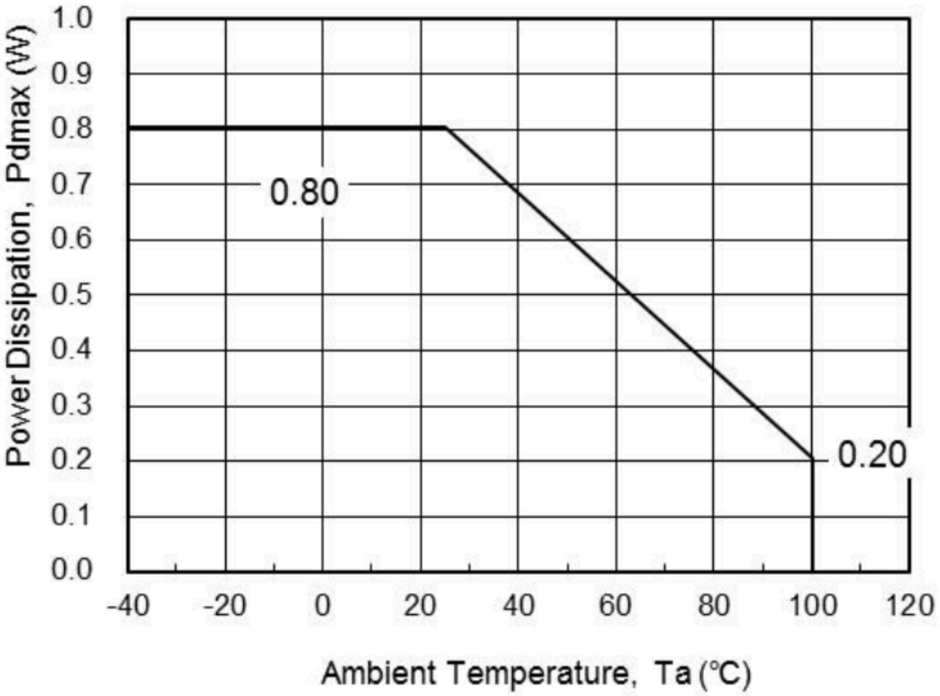


Figure 4. Pdmax vs T_A

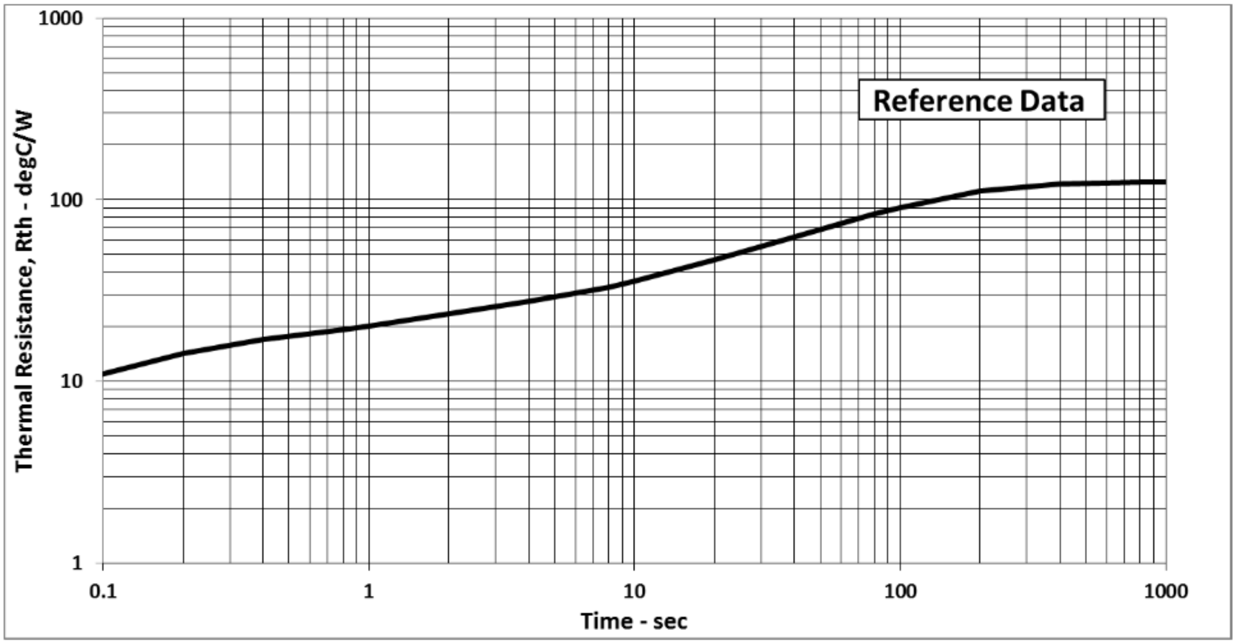


Figure 5. Thermal Resistance vs Time

DESCRIPTION OF OPERATION

1. Normal mode

- LC05732ARA controls charging and discharging by detecting cell voltage (VCC) and controls S2−S1 current. In case that cell voltage is between over−discharge detection voltage (Vuv) and over−charge detection voltage (Vov), and S2−S1 current is between charge over−current detection current (Ioch) and discharge over−current detection current (Ioc), internal power MOS FETs as CHG_SW, DCHG_SW are both turned ON.
  This is the normal mode, and it is possible to be charged and discharged.

2. Over−charging mode

- Internal power MOSFET CHG_SW turns off if cell voltage becomes greater than or equal to over−charge detection voltage (Vov) over the delay time of over−charging (Tov).
  This is the over−charging detection mode.
- The recovery from over−charging will be made after the following two conditions are satisfied.
  1. Charger is removed from IC.
  2. Cell voltage decreases under over−charge release voltage (Vovr) over the delay time of over−charging releasing (Tovr) due to discharging through a load.
  Consequently, internal power MOS FET as CHG_SW will be turned on and normal mode will be resumed.
- In over−charging mode, discharging over−current detection is made only when CS pin increases more than discharging over−current detection current 2(Ioc2), because discharge current flows through parasitic diode of CHG_SW FET.
  If CS pin voltage increases more than discharging over−current detection current 2 (Ioc2) over the delay time of discharging over−current 2 (Toc2), discharging will be shut off, because internal power FETs as DCHG_SW is turned off. (short−circuit detection mode)
  After detecting short−circuit, CS pin will be pulled down to VSS by internal resistor Rcsd.
- The recovery from short circuit detection in over−charging mode will be made after the following two conditions are satisfied.
  1. Load is removed from IC.
  2. CS pin voltage becomes less than or equal to discharging over−current detection current 2 (Ioc2) due to CS pin pulled down through Rcsd.
  Consequently, internal power MOS FET as DCHG_SW will be turned on, and over−charging detection mode will be resumed.

3. Over−discharging mode without Auto Wake Up function

- If cell voltage drops lower than over−discharge detection voltage (Vuv) over the delay time of over−discharging (Tuv), discharging will be shut off, internal power FETs as DCHG_SW is turned off.
  This is the over−discharging mode.
  After detecting over−discharging, CS pin will be pulled up to VCC by an internal resistor Rcsu and the bias of internal circuits will be shut off. (Shut−down mode)
  In shut−down mode, operating current is suppressed under 0.1 uA (max).
- The recovery from stand−by mode will be made by internal circuits biased after the connecting charger.
- By continuing to be charged, if cell voltage increases more than over−discharge detection voltage (Vuvr) over the delay time of over−discharging (Tuvr), internal power MOS FETs as DCHG_SW is turned on and normal mode will be resumed.
- In over−discharge detection mode, charging over−current detection does not operate.
  By continuing to be charged, charging over−current detection starts to operate after cell voltage goes up more than over−discharge release voltage (Vuvr).

4. Discharging over−current detection mode 1

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over−current detection current (Ioc) over the delay time of discharging over−current (Toc1).
  This is the discharging over−current detection mode 1.
  In discharging over−current detection mode 1, CS pin will be pulled down to VSS with internal resistor Rcsd.
- The recovery from discharging over−current detection mode will be made after the following two conditions are satisfied.
  1. Load is removed from IC.
  2. CS pin voltage becomes less than or equal to discharging over−current release current (Iocr) over the delay time of discharging over−current release (Tocr1) due to CS pin pulled down through Rcsd.
  Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

5. Discharging over−current detection mode 2 (short circuit detection)

- Internal power MOS FET as DCHG_SW will be turned off and discharging current will be shut off if CS pin voltage becomes greater than or equal to discharging over−current detection current2 (Ioc2) over the delay time of discharging over−current 2 (Toc2).
  This is the short circuit detection mode.

- In short circuit detection mode, CS pin will be pulled down to VSS by internal resistor Rcsd.
  The recovery from short circuit detection mode will be made after the following two conditions are satisfied.
  a. Load is removed from IC.
  b. CS pin voltage becomes less than or equal to discharging over−current release current (Iocr) over the delay time of discharging over−current release (Tocr1) due to CS pin pulled down through Rcsd.
  Consequently, internal power MOS FET as DCHG_SW will be turned on, and normal mode will be resumed.

6. Charging over−current detection mode

- Internal power MOS FET as CHG_SW will be turned off and charging current will be shut off if CS pin voltage becomes less than or equal to charging over−current detection current (Ioch) over the delay time of charging over−current (Toch).
  This is the charging over−current detection mode.
- The recoveries from charging over−current detection mode will be made after the following two conditions are satisfied.
  1. Charger is removed from IC and CS pin will increase by load connection.
  2. CS pin voltage becomes greater than or equal to charging over−current release current (Iochr) over the delay time of charging over−current release (Tocrh).
  Consequently, internal power MOS FET as CHG_SW will be turned on, and normal mode will be resumed.
  *Internal current flows out through CS and S2 terminals.
  After charger is removed, it flows through parasitic diode of CHG_SW FET.
  Therefore, CS pin voltage will go up more than charging over−current release current (Iochr).
  So CS pin voltage is not an indispensable condition for recovery from charging over−current detection.

7. 0 V Battery Protection Function

This function protects the battery when a short circuit in the battery (0 V battery) is detected, at which point charging will be prohibited.
When the voltage of a battery is below 1.4 V (max), the gate of the charging control FET is fixed to the PAC−Terminal voltage, at which point charging will be prohibited.
If the voltage of the battery is greater than the 0 V battery prohibit voltage (Vinh), charging will be enabled.

8. Reset mode

- In case of normal mode, internal power MOS FET as CHG_SW and DCHG_SW will be turned off and charging and discharging current will be shut off if RSTB pin voltage becomes less than or equal to low−level input voltage (VIL) over the delay time of reset pulse width(Tw_res).
  This is the reset mode.
- The recovery from reset mode will be made itself after the reset release time (Tres).
  Consequently, internal power MOS FET as CHG_SW and DCHG_SW will be turned on, and normal mode will be resumed.

TIMING CHART

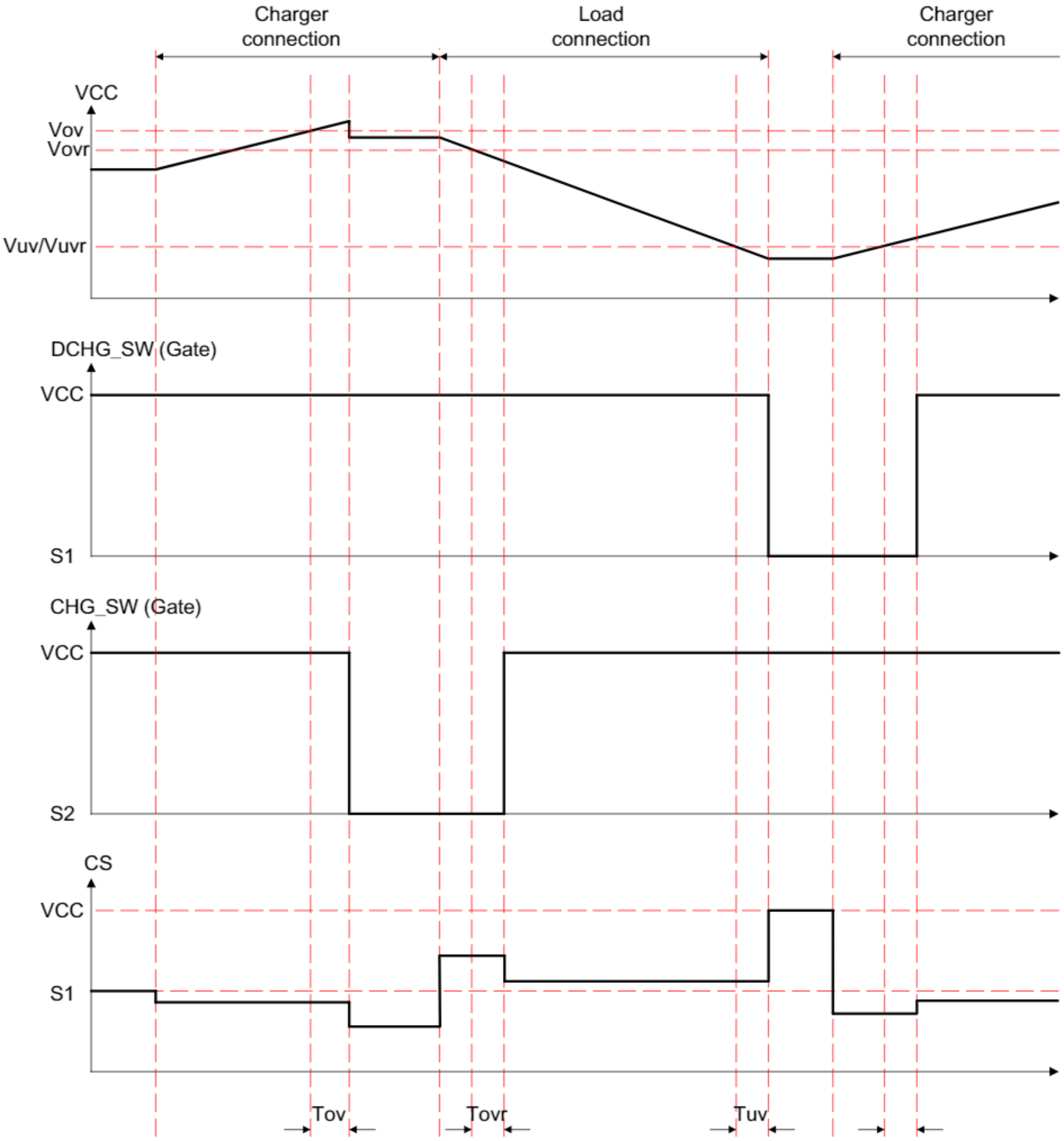


Figure 6. Over−charge Detection/Release, Over−discharge Detection/Release (Connect Charger)

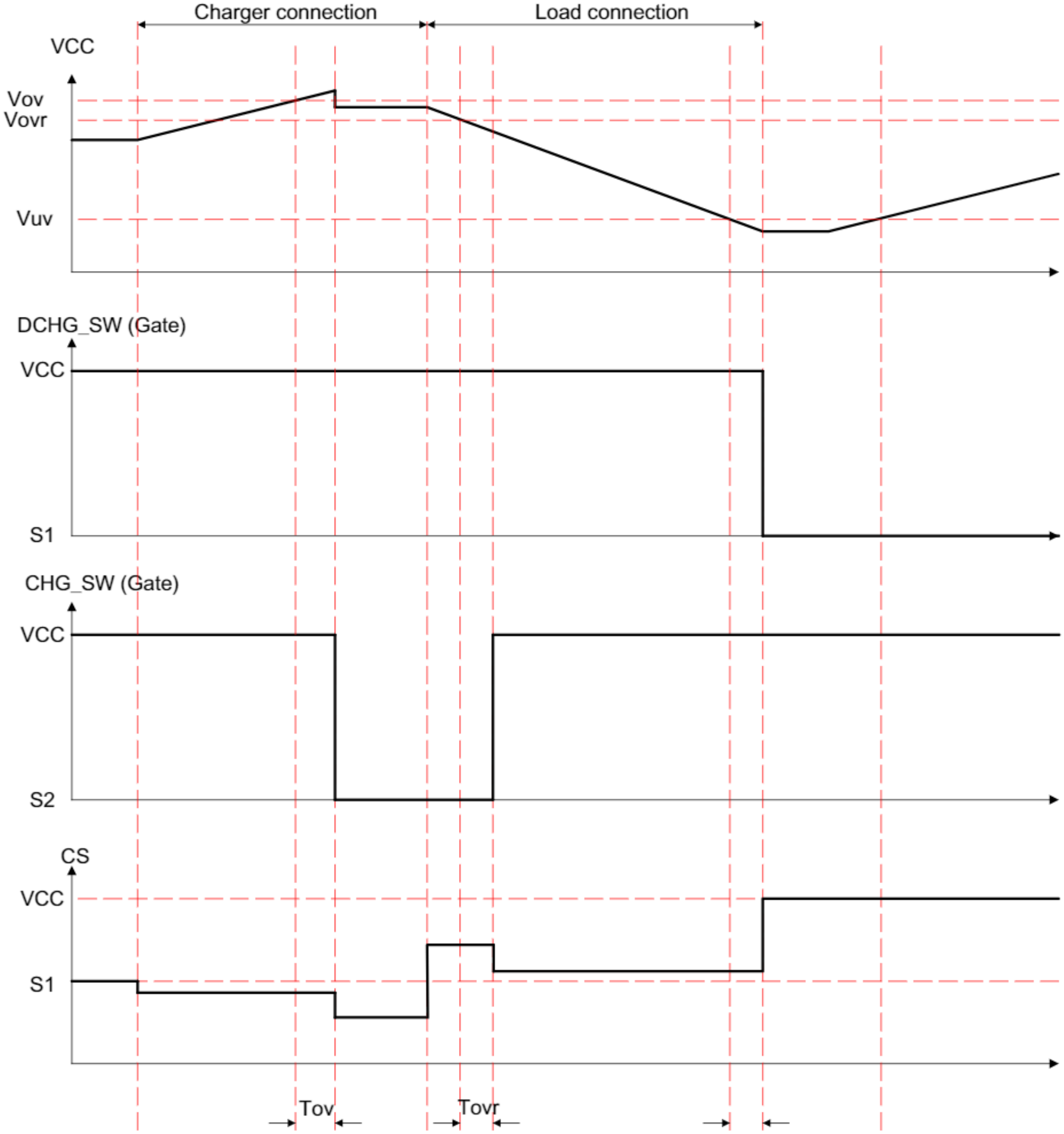


Figure 7. Over−charge Detection/Release, Over−discharge Detection/Release (Non−connect Charger)

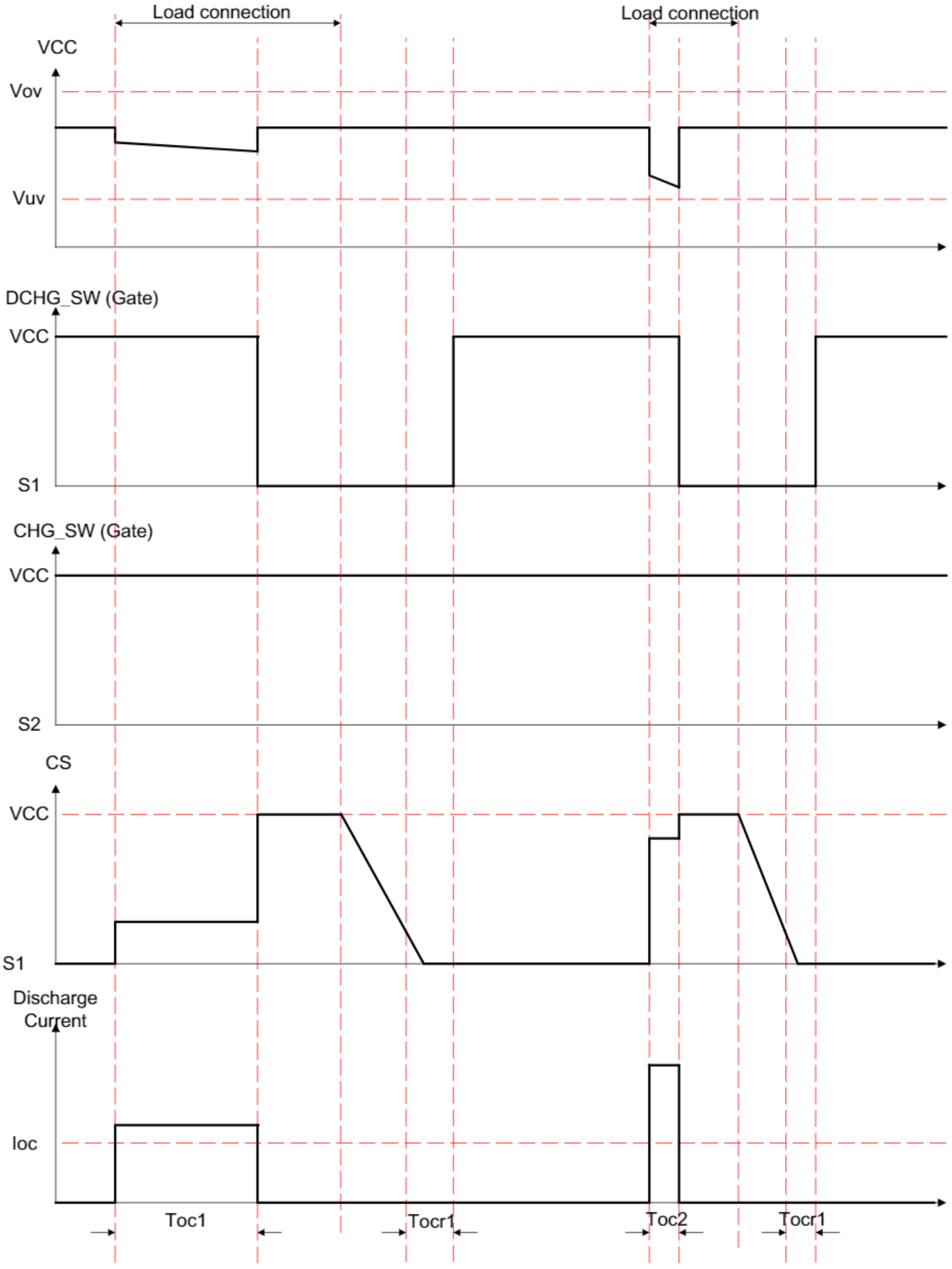


Figure 8. Discharge Over−Current Detection1, Discharge Over−current Detection2 (Short Circuit)

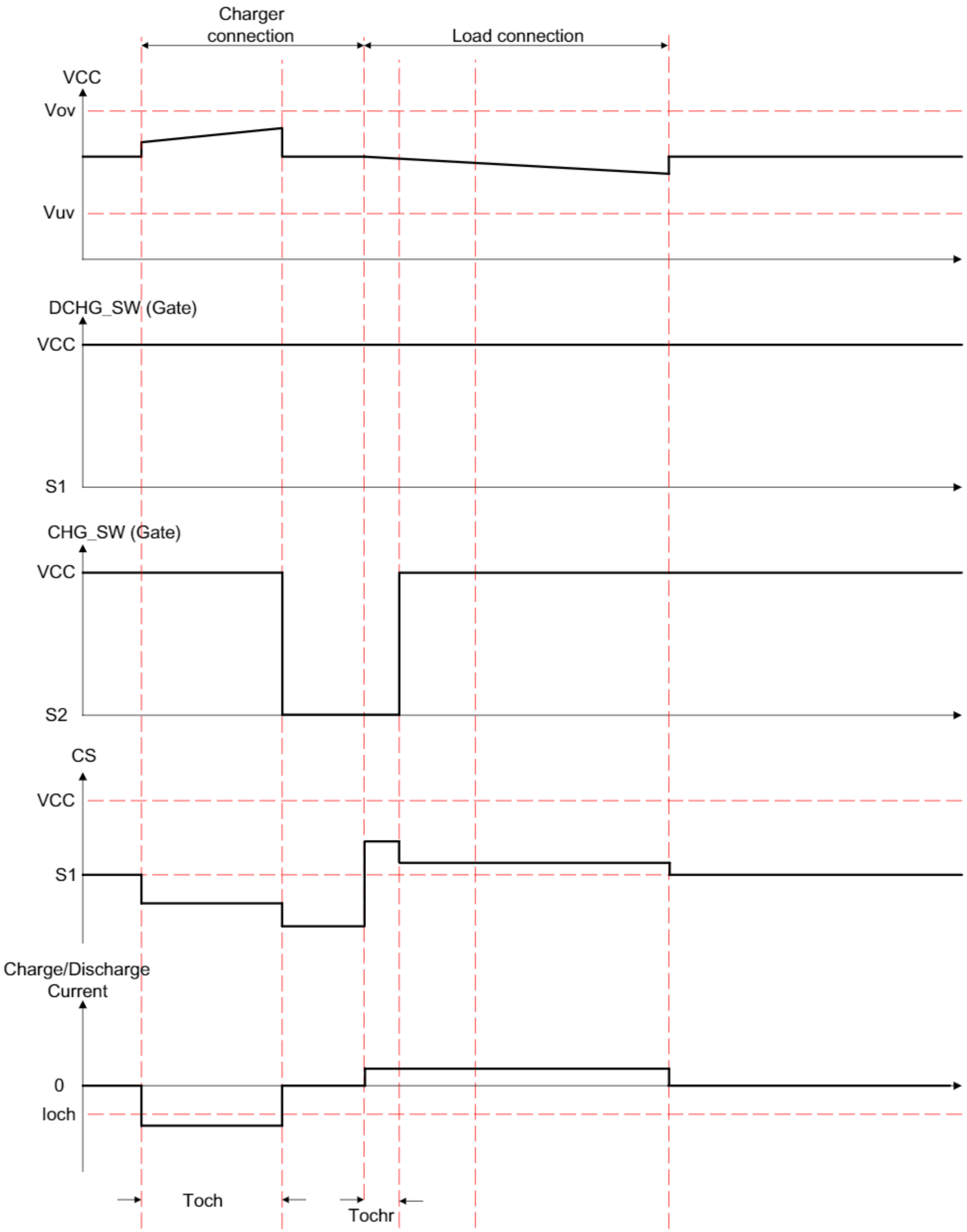


Figure 9. Charge Over−current Detection

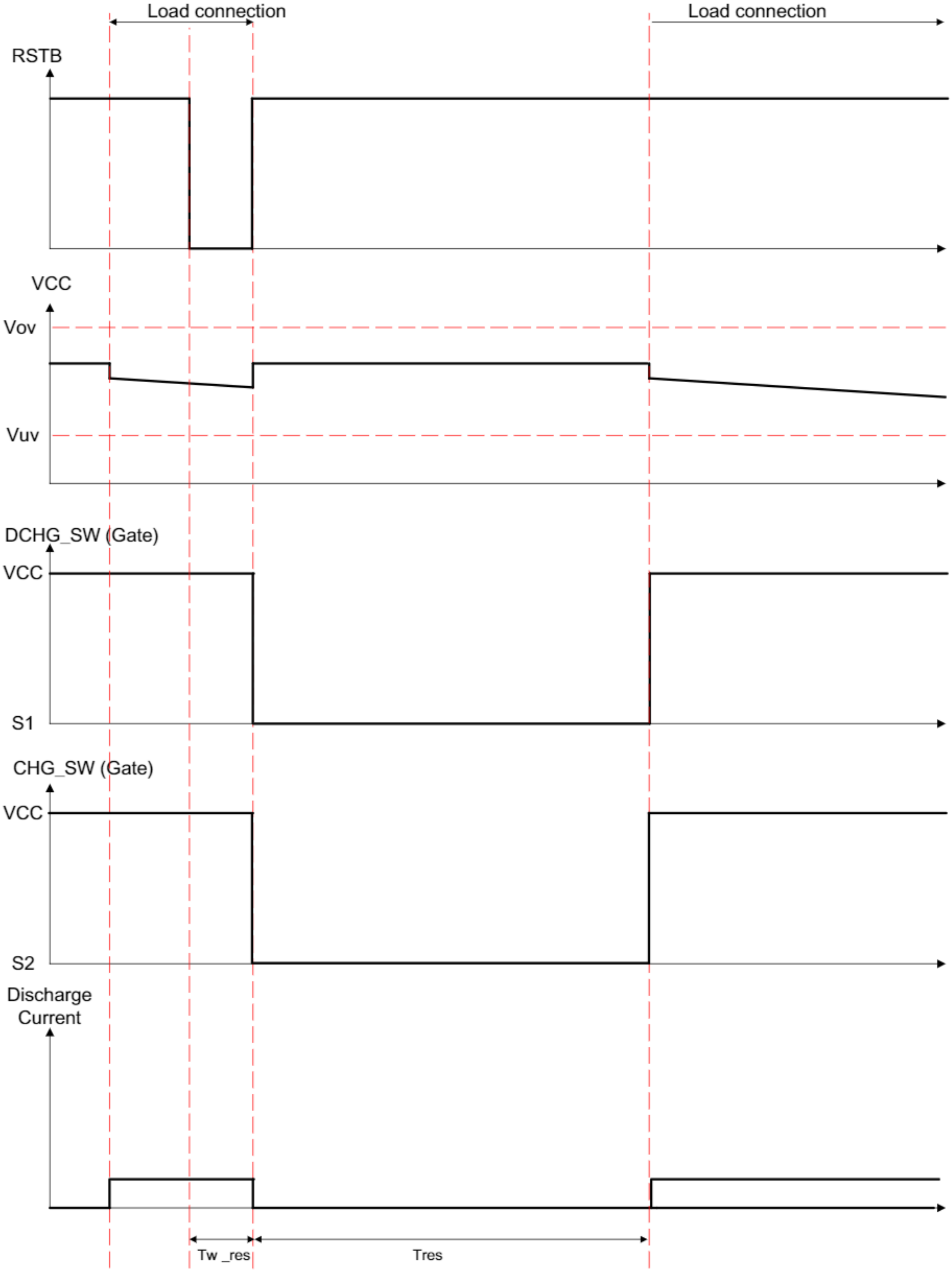
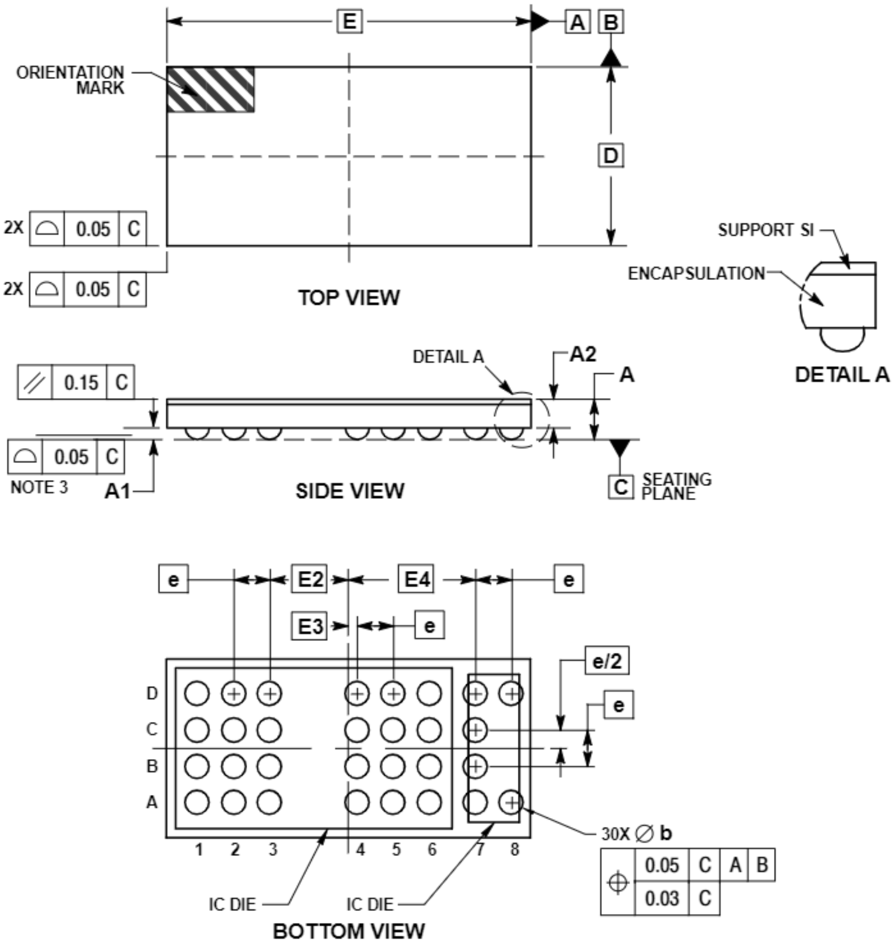


Figure 10. Reset Function

PACKAGE DIMENSIONS

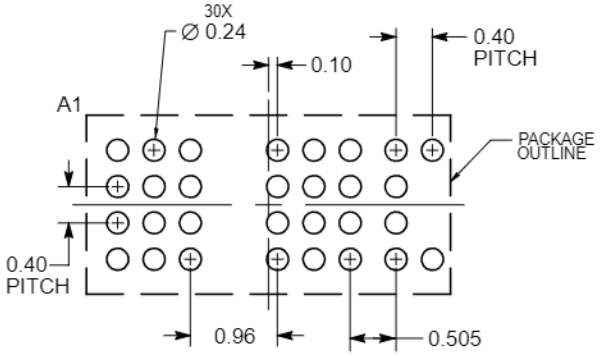
ECP30, 1.97x4.01
CASE 971BC
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS	
DIM	MIN	MAX
A	0.545	0.625
A1	0.165	0.205
A2	0.380	0.420
b	0.245	0.285
D	1.970 BSC	
E	4.010 BSC	
E2	0.860 BSC	
E3	0.100 BSC	
E4	1.405 BSC	
e	0.400 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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