The documentation and process conversion measures necessary to comply with this revision shall be completed by:
21 December 2018.

INCH-POUND

MIL-PRF-19500/498F
24 August 2018
SUPERSEDING
MIL-PRF-19500/498E
12 May 2005

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, POWER,
TYPES 2N6306 AND 2N6308, CASE MOUNT PACKAGES,
QUALITY LEVELS JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN silicon, power transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each device type as specified in MIL-PRF-19500.

1.2 Package outlines. The device packages for the encapsulated device types are as follows: Case mount TO-204AA (formerly TO-3) in accordance with figure 1; case mount TO-254AA in accordance with figure 2; and case mount TO-257AA in accordance with figure 3.

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

1.3.1 Ratings applicable to all Part or Identifying Numbers (PIN). $T_J = T_{STG}$ = –65°C to +200°C.

1.3.2 Ratings applicable to individual types.

Type	P_T	P_T T_C = +25°C (1)	$R_{\theta JC}$ (3)	V_{CBO}	V_{CEO}	V_{EBO}	I_B	I_C
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc
2N6306	5	125	1.4	500	250	8.0	4.0	8.0
2N6306T1	6	175	1.0	500	250	8.0	4.0	8.0
2N6306T3	4	125 (2)	1.3	500	250	8.0	4.0	8.0
2N6308	5	125	1.4	700	350	8.0	4.0	8.0
2N6308T1	6	175	1.0	700	350	8.0	4.0	8.0
2N6308T3	4	125 (2)	1.3	700	350	8.0	4.0	8.0

(1) See figures 4 through 6 for temperature-power derating curves.
(2) For TO-257 devices with typical mounting and small footprint, conservatively rated at 125 W and 1.3°C/W only.
(3) See figures 7 through 9 for thermal impedance graphs.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.dla.mil.

1.4 Primary electrical characteristics. T_A = +25°C, unless otherwise specified.

Type	h_{FE1} V_{CE} = 5 V dc I_C = 3 A dc		h_{FE2} V_{CE} = 5 V dc I_C = 8 A dc		$V_{BE(sat)}$ (1) I_C = 8 A dc I_B = (2)		$V_{CE(sat)1}$ (1) I_C = 8 A dc I_B = (2)		$V_{CE(sat)2}$ (1) I_C = 3 A dc I_B = 0.6 A dc	
	Min	Max	Min	Max	Min V dc	Max V dc	Min V dc	Max V dc	Min V dc	Max V dc
2N6306	15	75	4			2.3		5		0.8
2N6306T1	15	75	4			2.3		5		0.8
2N6306T3	15	75	4			2.3		5		0.8
2N6308	12	60	3			2.5		5		1.5
2N6308T1	12	60	3			2.5		5		1.5
2N6308T3	12	60	3			2.5		5		1.5

Limit	$\|h_{fe}\|$ V_{CE} = 10 V dc I_C = 0.3 A dc f = 1 MHz	C_{obo} V_{CB} = 10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	Switching (3)	
			t_{on}	t_{off}
		pF	µs	µs
Min	5			
Max	30	250	0.6	3.0

(1) Pulsed (see 4.5.1).
(2) 2N6306, 2N6306T1, 2N6306T3 (I_B) = 2.0 A dc; 2N6308, 2N6308T1, 2N6308T3 (I_B) = 2.67 A dc.
(3) See figure 10 (pulse response circuit).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

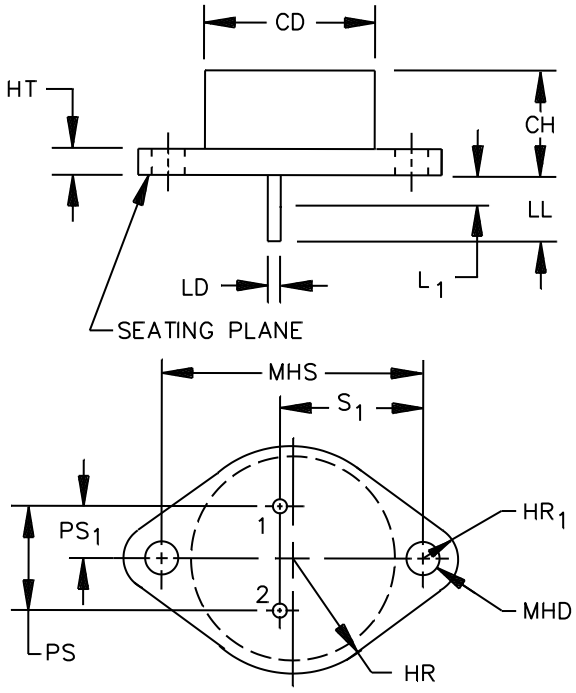
1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are "6306" and "6308".

1.5.3 Suffix symbols. The following suffix symbol(s) are incorporated into the PINs for this specification sheet.

blank	A blank suffix indicates a TO–204AA package configuration as shown on figure 1.
T1	The T1 suffix indicates a TO-254AA package configurations as shown on figure 2.
T3	The T3 suffix indicates a TO-257AA package configurations as shown on figure 3.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

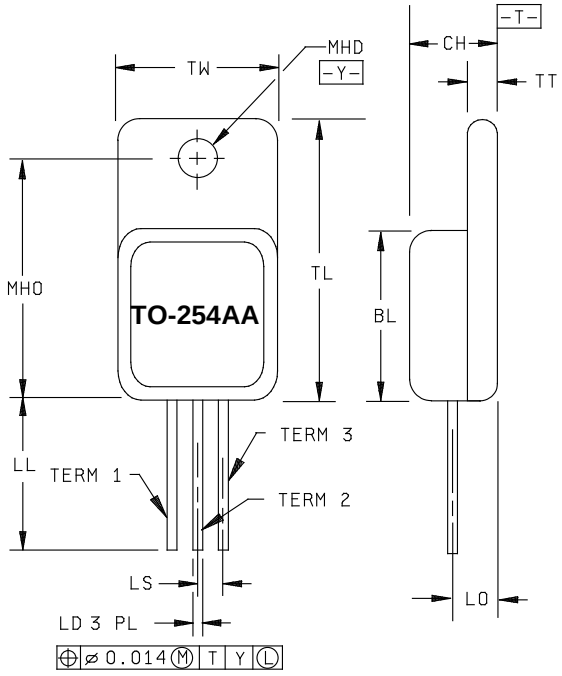
Ltr	Dimension				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.22	5
CH	.250	.450	6.35	11.43	
HR	.495	.525	12.57	13.34	6
HR_1	.131	.188	3.33	4.78	6
HT	.060	.135	1.52	3.43	
LD	.038	.053	0.97	1.35	7, 8, 9
LL	.312	.500	7.92	12.70	7, 8, 9
L_1		.050		1.27	7
MHD	.151	.165	3.84	4.19	10
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	8
PS_1	.205	.225	5.21	5.72	7, 8
S_1	.655	.675	16.64	17.15	7, 8



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Terminal 1 is the emitter and terminal 2 is the base. The collector shall be electrically connected to the case.
3. Mounting holes shall be deburred on the seating plane side.
4. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
5. Body contour is optional within zone defined by dimension CD.
6. Applies to all sides (dimension HR) or both ends (dimension HR_1).
7. Applies to both terminals.
8. Measurement for this dimension shall be taken at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below the seating plane. When gauge is not used, measurement shall be made at seating plane.
9. Dimension LD applies between dimension L_1 and dimension LL. Lead diameter shall not exceed twice dimension LD within dimension L_1.
10. Applies to both holes.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

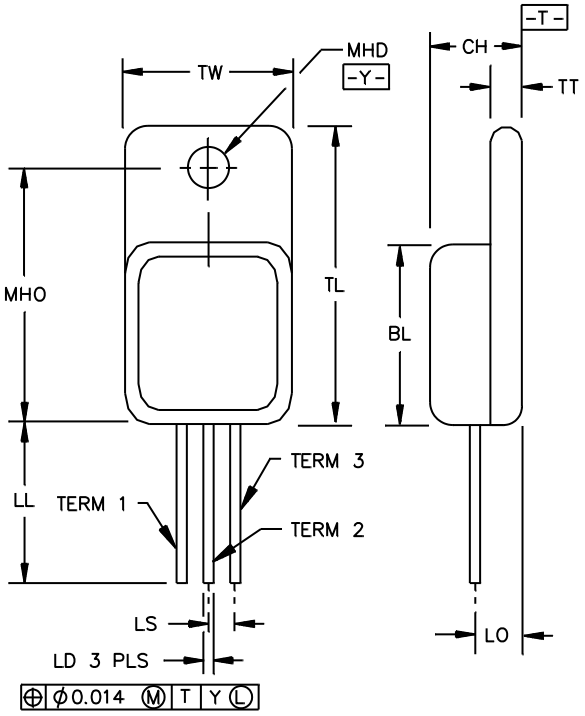
FIGURE 1. Physical dimensions for TO–204AA (similar to TO-3) (2N6306 and 2N6308).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.530	.550	13.46	13.97
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Term 1 is base; term 2 is the collector; and term 3 is the emitter.
3. All terminals are isolated from case.
4. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Dimensions and configuration for TO-254AA package (2N6306T1 and 2N6308T1).



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.500	.750	12.70	19.05
LO	.120 typ		3.05 typ	
LS	.100 bsc		2.54 bsc	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.63
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. Term 1 is the base, term 2 is the collector, and term 3 is the emitter.
3. All terminals are isolated from case. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent AL_2O_3 (ceramic).
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Dimensions and configuration for TO-257AA package (2N6306T3 and 2N6308T3).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods For Semiconductor Devices.

(Copies of these documents are available online at http://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO–204AA, similar to TO-3), figure 2 (TO-254AA), and figure 3 (TO-257AA).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin-out. The pin-out of the device shall be as shown on figures 1, 2 and 3.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be table I as specified herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANTX and JANTXV only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements
	Quality levels JANTX and JANTXV
3c (1)	Thermal impedance (transient), method 3131 of MIL-STD-750 (see 4.3.2)
7	Optional.
11	I_{CEX1} and h_{FE3}
12	See 4.3.1
13	Subgroup 2 of table I herein; ΔI_{CEX1} ≤ 100 percent of initial value or 500 nA dc, whichever is greater. Δh_{FE3} ≤ 25 percent of initial value.
14	Required.
17	Required for TO-254AA and TO-257AA packages only (see 4.3.3).

(1) Thermal impedance ($Z_{\theta JX}$) limits shall not exceed figures 7, 8, or 9. This test shall be performed anytime after temperature cycling, screen 3a, and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. The power burn-in conditions shall be as follows: T_J = + 175°C minimum, V_{CB} = 10 - 30 V dc; T_A = +30°C maximum.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit used in screen 3c of 4.3 herein and table I shall comply with the thermal impedance graph in figures 7, 8, or 9 (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.3.3 Dielectric withstanding voltage. The dielectric withstanding voltage test for case isolated TO-254AA and TO-257AA packages shall be in accordance with test method 1081 of MIL-STD-750. After the test, end-point electrical measurements in accordance with subgroup 2 of table I herein shall be taken.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1037	V_{CB} ≥ 10 V dc; ΔT_J between cycles ≥ +100°C; $t_{on} = t_{off}$ ≥ 1 minute.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	For 2N6306 and 2N6308, test condition A, weight = 10 lbs (4.5 Kg), t = 15 seconds; for 2N6306T1 and 2N6308T1, test condition A, weight = 10 lbs (4.5 Kg), t = 10 seconds; for 2N6306T3 and 2N6308T3, test condition A, weight = 10 lbs (4.5 Kg), t = 10 seconds;
C5	3131	See 1.3.
C6	1037	V_{CB} ≥ 10 V dc; ΔTJ between cycles ≥ +100°C; ton = t_{off} 1 minute. No heat sink or forced-air cooling on device shall be permitted.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to base breakdown voltage	3011	Bias condition D, I_C = 100 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N6306 3/				250		V dc
2N6308 3/				300		V dc
Collector to emitter cutoff current	3041	Bias condition D	I_{CEO}		50	µA dc
2N6306 3/		V_{CE} = 250 V dc				
2N6308 3/		V_{CE} = 350 V dc				
Emitter-base cutoff current	3061	Bias condition D; V_{EB} = 8 V dc	I_{EBO}		5.0	A dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 1.5 V dc	I_{CEX1}			
2N6306 3/		V_{CE} = 500 V dc			5.0	µA dc
2N6308 3/		V_{CE} = 700 V dc			5.0	µA dc
Base emitter voltage	3066	Test condition A; I_C = 8.0 A dc; pulsed (see 4.5.1)	$V_{BE(sat)}$			
2N6306 3/		I_B = 2.0 A dc			2.3	V dc
2N6308 3/		I_B = 2.67 A dc			2.5	V dc
Base emitter voltage	3066	Test condition B; I_C = 3.0 A dc; V_{CE} = 5.0 V dc; pulsed (see 4.5.1)	$V_{BE(on)}$			
2N6306 3/					1.3	V dc
2N6308 3/					1.5	V dc
Collector to emitter saturated voltage	3071	I_C = 8.0 A dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		5.0	V dc
2N6306 3/		I_B = 2.0 A dc				
2N6308 3/		I_B = 2.67 A dc				
Collector to emitter saturated voltage	3071	I_C = 3.0 A dc; I_B = 0.6 A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$			
2N6306 3/					0.8	V dc
2N6308 3/					1.5	V dc
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 3.0 A dc; pulsed (see 4.5.1)	h_{FE1}			
2N6306 3/				15	75	
2N6308 3/				12	60	

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued.						
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 8.0 A dc; pulsed (see 4.5.1)	h_{FE2}			
2N6306 3/				4		
2N6308 3/				3		
Forward-current transfer ratio	3076	V_{CE} = 5 V dc; I_C = 0.5 A dc; pulsed (see 4.5.1)	h_{FE3}			
2N6306 3/				15		
2N6308 3/				12		
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 1.5 V dc	I_{CEX2}		300	µA dc
2N6306 3/		V_{CE} = 450 V dc				
2N6308 3/		V_{CE} = 650 V dc				
Low-temperature operation:		T_A = –55°C				
Forward-current transfer ratio	3076	V_{CE} = 5.0 V dc; I_C = 3.0 A dc; pulsed (see 4.5.1)	h_{FE4}			
2N6306 3/				6		
2N6308 3/				5		
Subgroup 4						
Pulse response: Transfer ratio	3251	Test condition A, except test circuit and pulse requirements in accordance with figure 10.				
Turn-on time		V_{CC} = 125 V dc; I_C = 3.0 A dc; I_B = 0.6 A dc	t_{on}		0.6	µs
Turn-off time		V_{CC} = 125 V dc; I_C = 3.0 A dc; I_{B1} = 0.6 A dc; I_{B2} = 1.5 A dc	t_{off}		3.0	µs
Magnitude of common emitter small-signal short-circuit forward- current transfer ratio	3306	V_{CE} = 10 V dc; I_C = 0.3 A dc; f = 1 MHz	$\|h_{fe}\|$	5	30	
Open capacitance (open circuit)	3236	V_{CB} = 10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1.0 MHz	C_{obo}		250	pF
Small-signal short- circuit forward- current transfer ratio	3206	V_{CE} = 4.0 V dc; I_C = 0.5 A dc; f = 1.0 kHz	h_{fe}	5		

See footnotes at end of table.

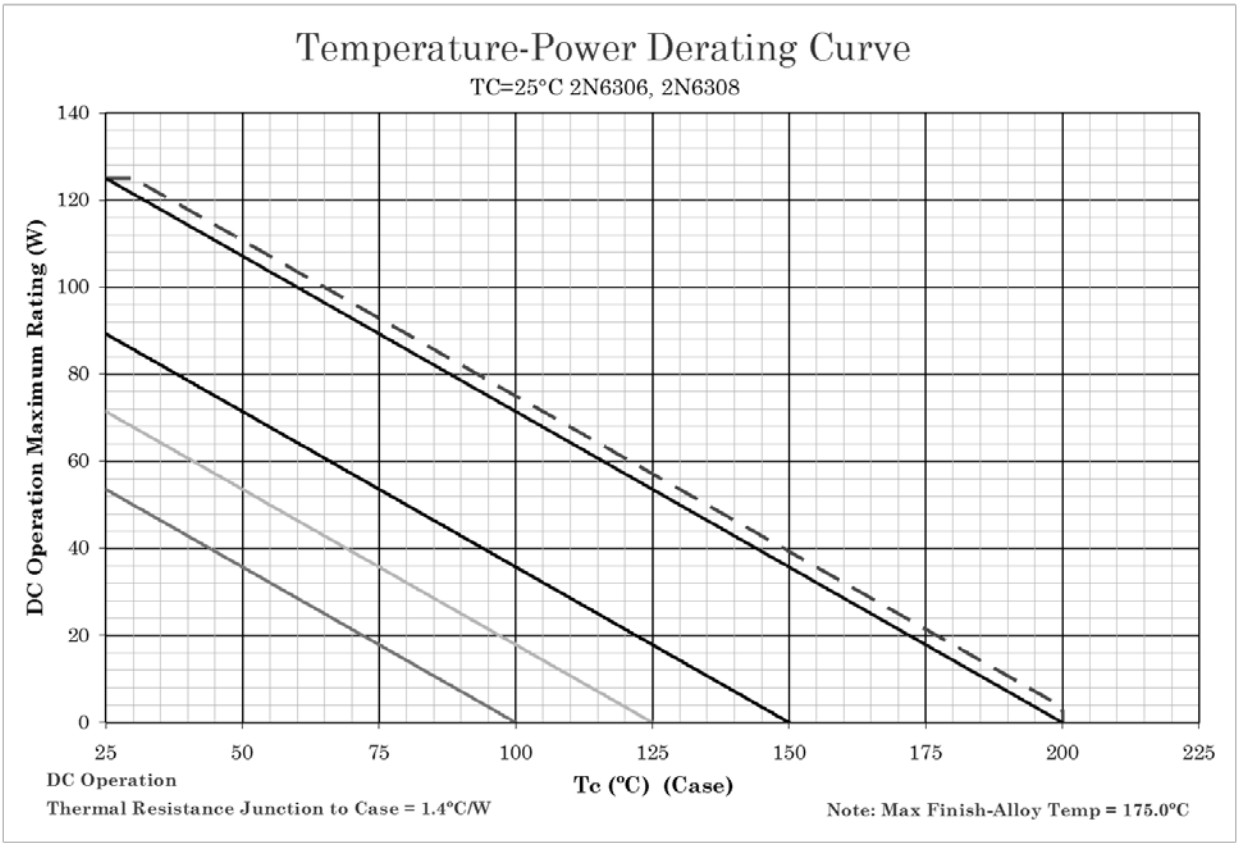
TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area (dc operation)	3051	T_C = +25°C t = 1 s; 1 cycle; (See figures 11 and 12)				
Test 1 (All device types)		V_{CE} = 15.6 V dc; I_C = 8 A dc				
Test 2 (All device types)		V_{CE} = 37 V dc; I_C = 3.4 A dc				
Test 3						
2N6306 3/		V_{CE} = 200 V dc; I_C = 65 mA dc				
2N6308 3/		V_{CE} = 300 V dc; I_C = 25 mA dc				
Electrical measurements		Table I, subgroup 2 herein				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ For end-point electrical measurements, this test required for the following:
Group B, subgroups 2 and 3.
Group C, subgroups 2 and 6.
Group E, subgroup 1.
3/ Includes device types with T1 and T3 suffix symbols.

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

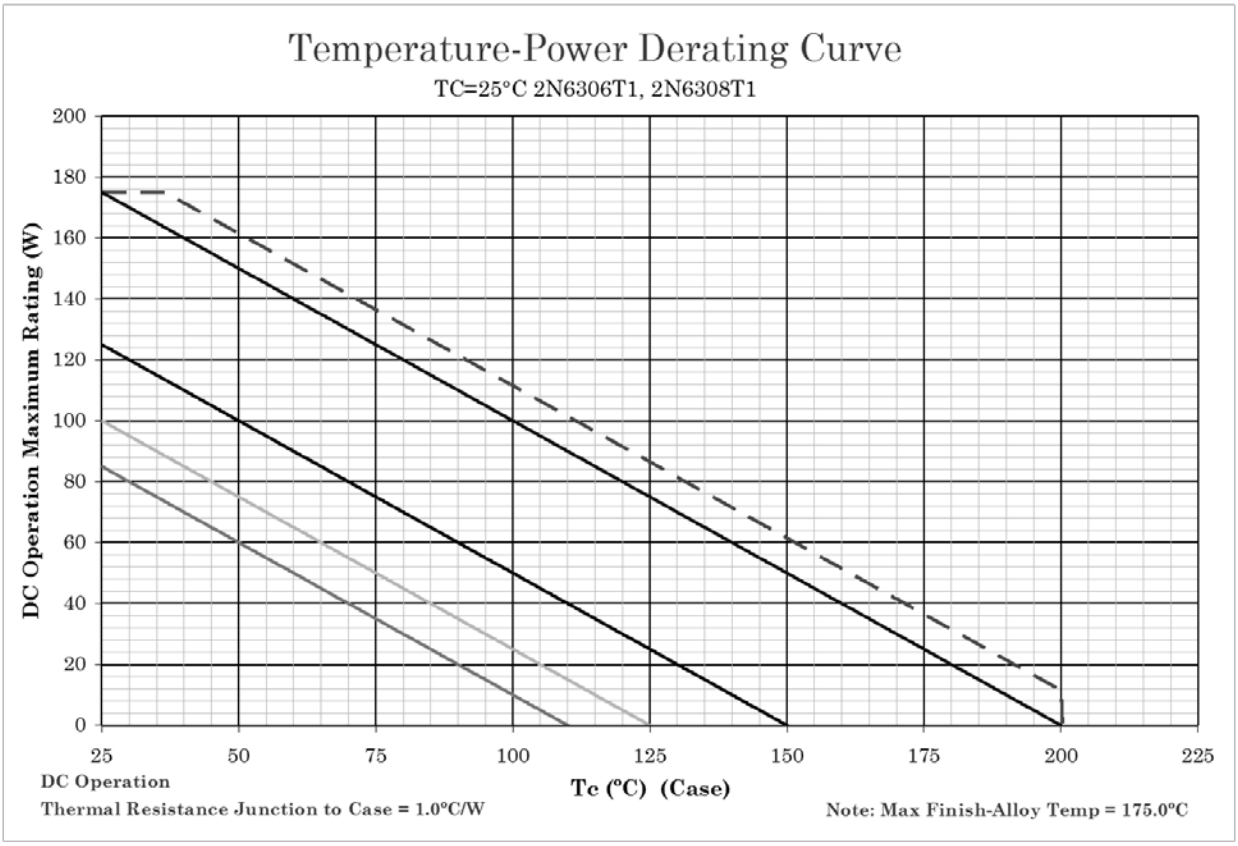
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	500 cycles.	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
Blocking life	1048	1,000 hours minimum, T_A = +150°C, V_{CB} = 80 percent of rated.	
Electrical measurements		See table I, subgroup 2 herein (except for thermal impedance).	
Subgroup 4			Sample size N/A
Thermal impedance curves		Each supplier shall submit their qual-lot average and design maximum thermal impedance curves to the qualifying activity. In addition, the optimal test conditions and thermal impedance limit shall be provided to the qualifying activity in the qualification report.	
Subgroup 5			15 devices c = 0
Barometric pressure	1001	Condition C; see 1.3.	
Subgroup 6			
ESD	1020	Testing is not required for class 3 listing. Testing is required for a nonsensitive listing to prove capability.	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A.	



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

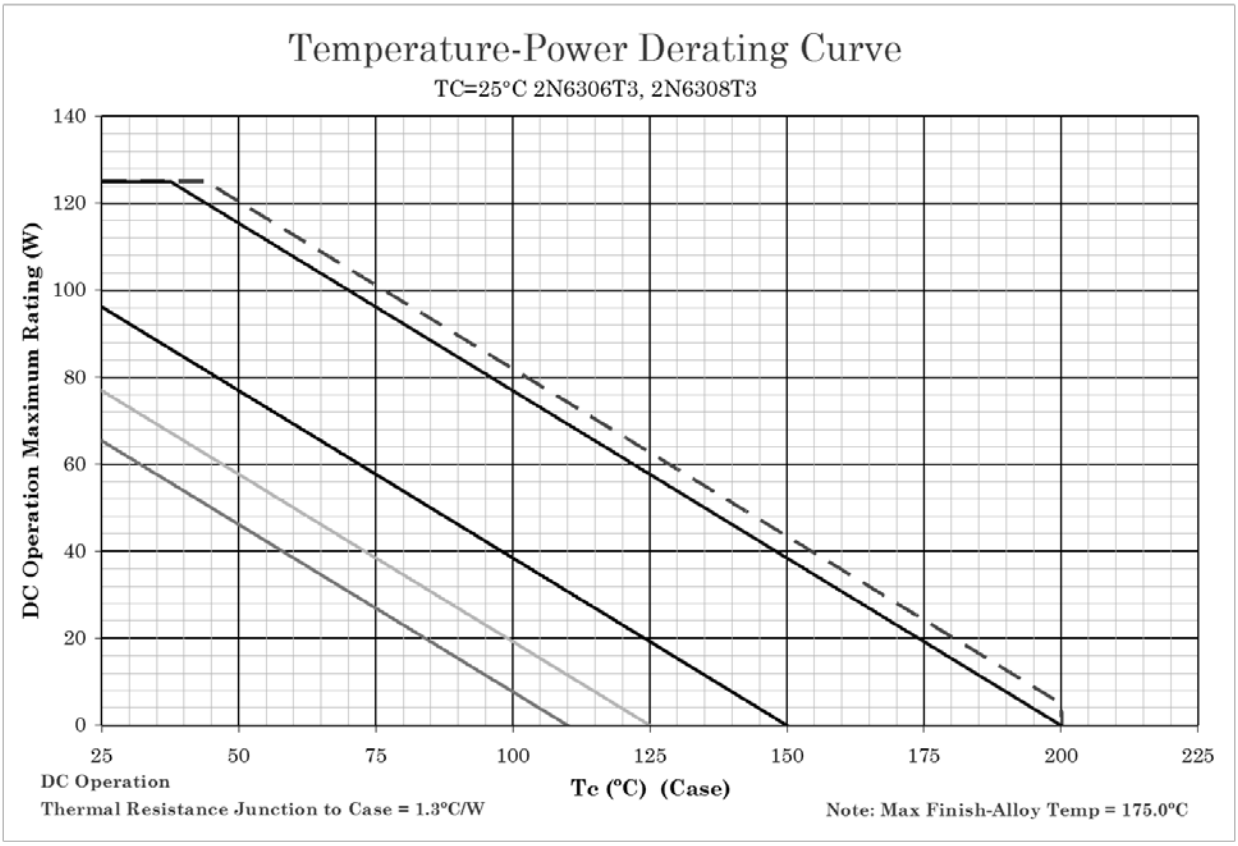
FIGURE 4. Temperature-power derating graph (2N6306, 2N6308, TO-204AA package).



NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Temperature-power derating graph (2N6306T1, 2N6308T1, TO-254AA package).



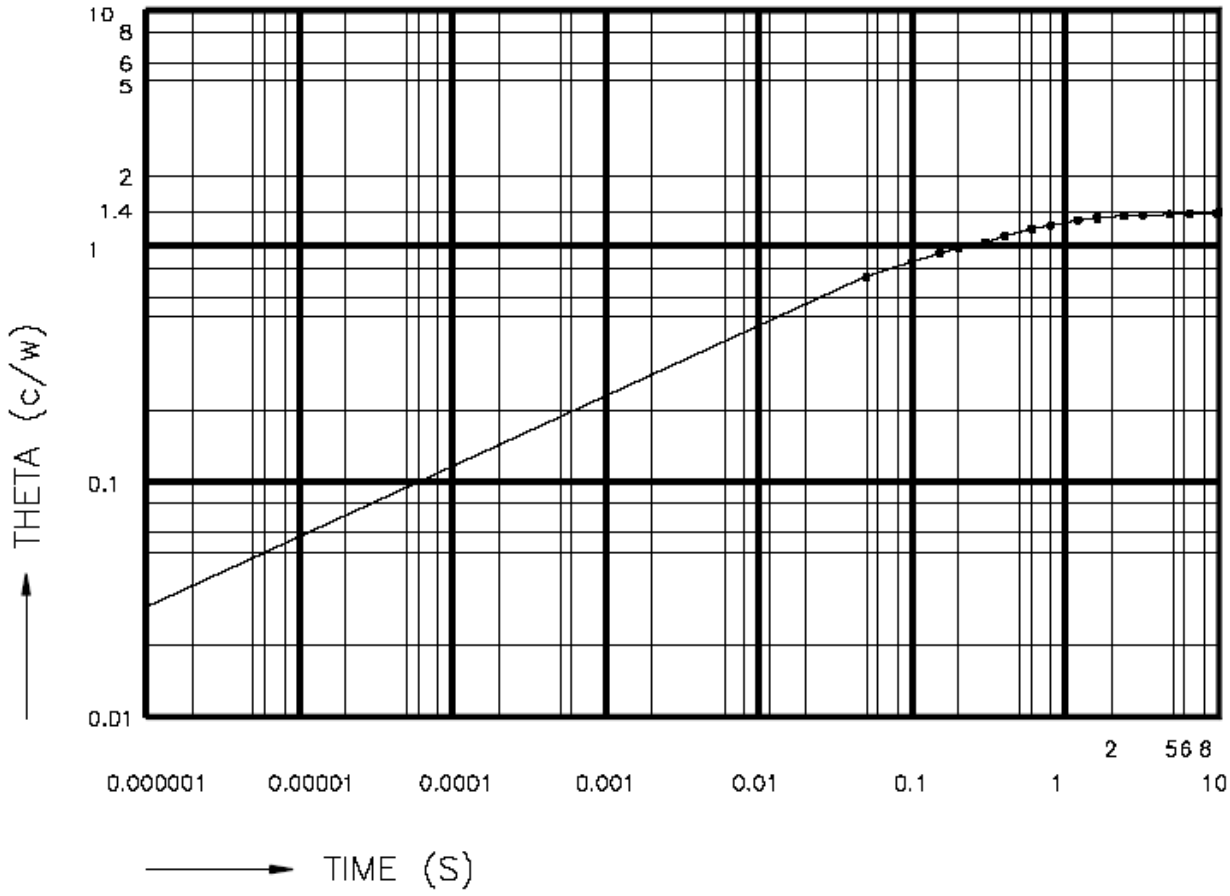
NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125°C$, and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 6. Temperature-power derating graph (2N6306T3, 2N6308T3, TO-257AA package).

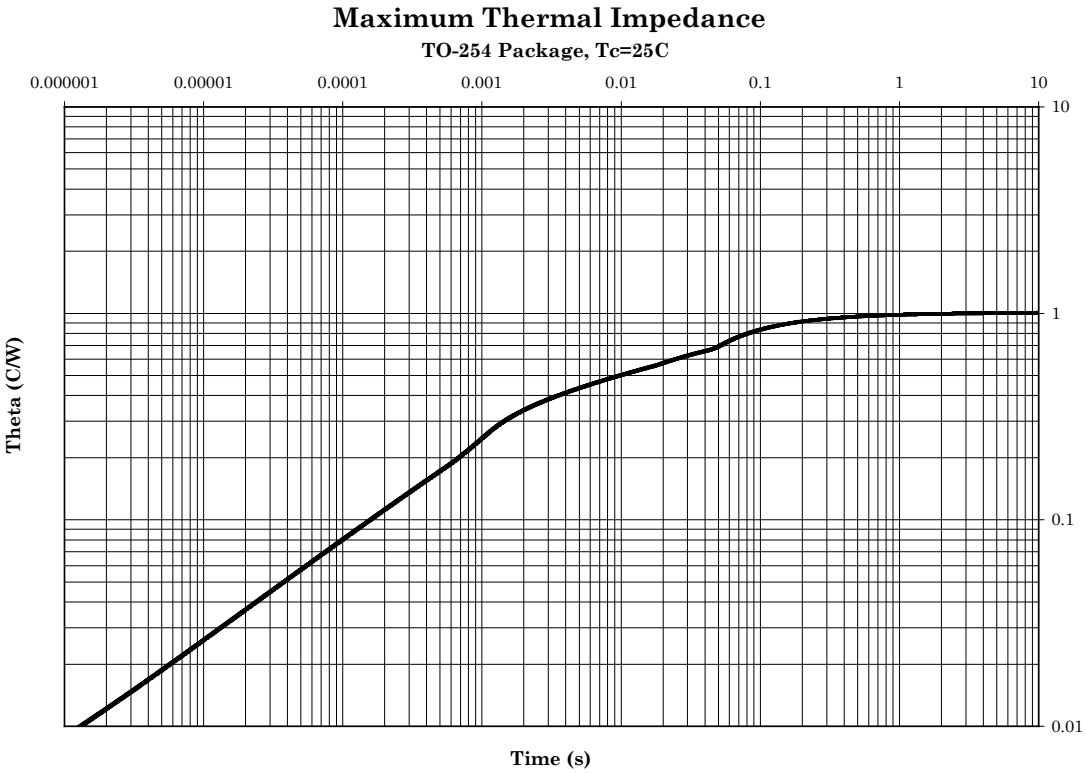
Maximum Thermal Impedance

TO-204AA package, T_C = +25°C



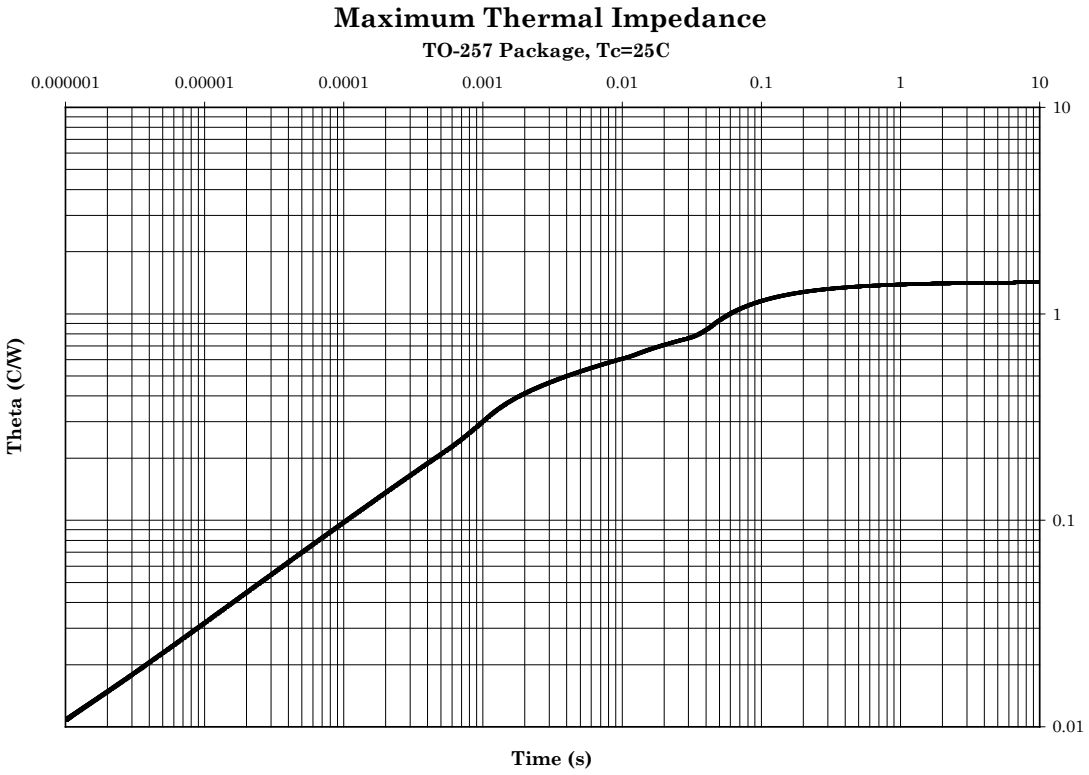
$R_{\theta JC}$ = 1.4 °C/W max.

FIGURE 7. Thermal impedance graphs (2N6306 and 2N6308).



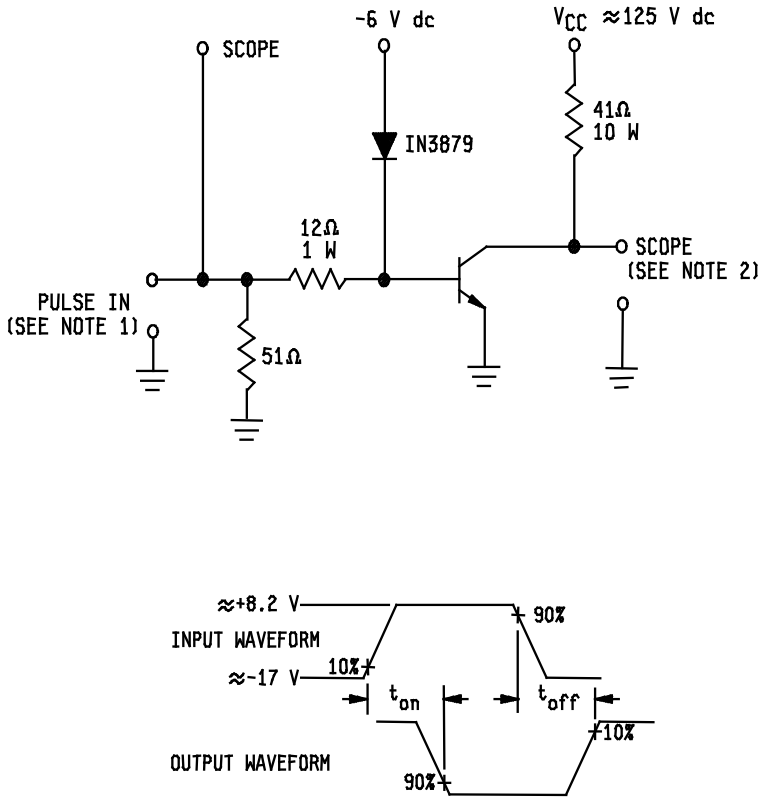
$R_{\theta JC}$ = 1.0 °C/W max.

FIGURE 8. Thermal impedance graphs (2N6306T1 and 2N6308T1).



$R_{\theta JC}$ = 1.3 °C/W max.

FIGURE 9. Thermal impedance graphs (2N6306T3 and 2N6308T3).



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 2 ns; duty cycle ≤ 1 percent; generator source impedance shall be 50Ω; pulse width = 30 µs.
2. Output sampling oscilloscope: Z_{IN} ≥ 20 kΩ; C_{IN} ≤ 50 pF; rise time ≤ 0.2 ns.

FIGURE 10. Pulse response test circuit and waveforms.

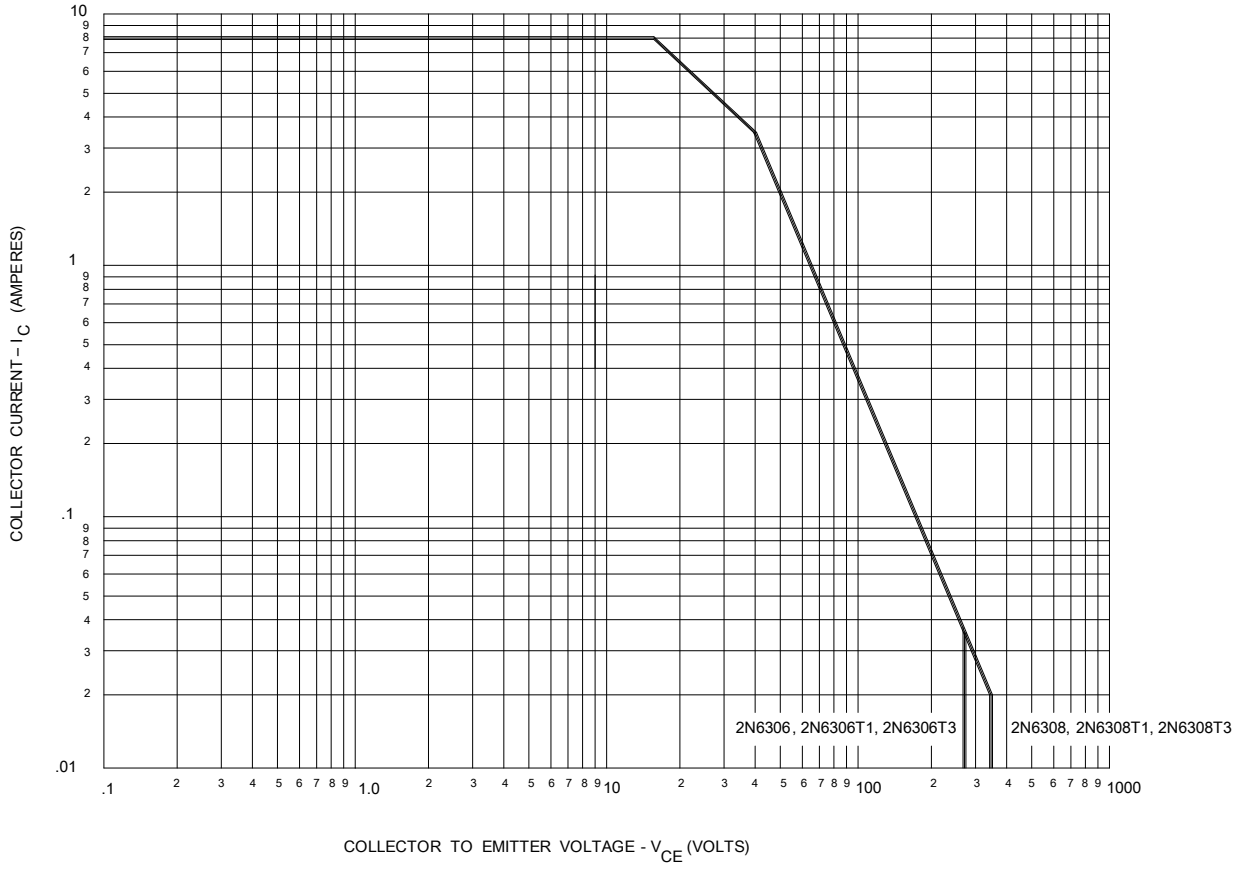


FIGURE 11. Maximum safe operating area graph (continuous dc).

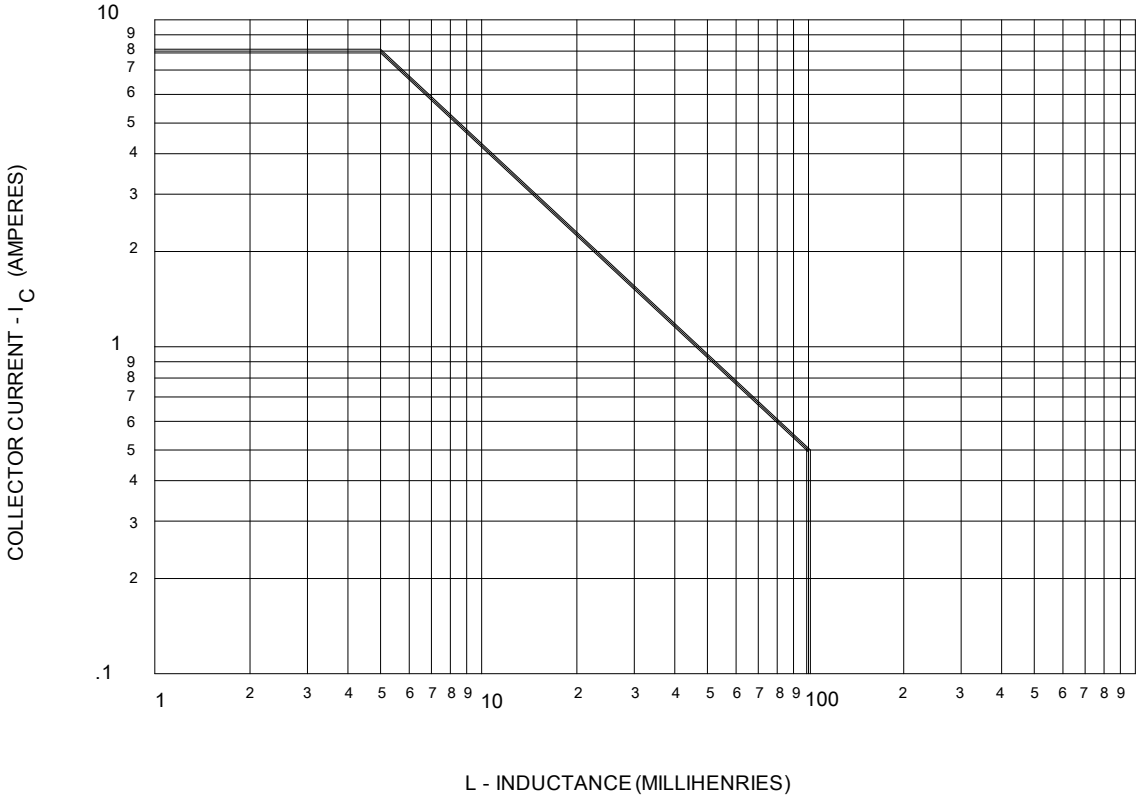


FIGURE 12. Safe operating area for switching between saturation and cutoff (unclamped inductive load).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

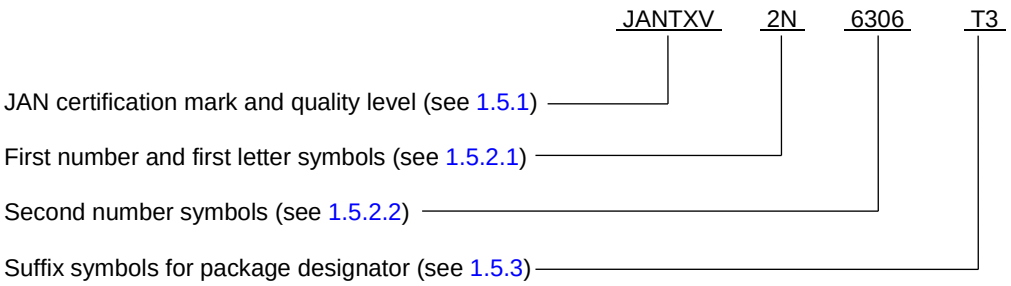
b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at http://qpldocs.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

JAN quality level	JANTX quality level	JANTXV quality level
JAN2N6306	JANTX2N6306	JANTXV2N6306
JAN2N6306T1	JANTX2N6306T1	JANTXV2N6306T1
JAN2N6306T3	JANTX2N6306T3	JANTXV2N6306T3
JAN2N6308	JANTX2N6308	JANTXV2N6308
JAN2N6308T1	JANTX2N6308T1	JANTXV2N6308T1
JAN2N6308T3	JANTX2N6308T3	JANTXV2N6308T3

6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.7 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army – CR
Air Force – 85
NASA – NA
DLA – CC

Review activities:
Army – MI
Air Force – 19

Preparing activity:
DLA – CC

(Project 5961–2018–063)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.