

The documentation and process conversion measures necessary to comply with this document shall be completed by 14 August 2021.

INCH-POUND

MIL-PRF-19500/263B  
W/AMENDMENT 2  
14 May 2021  
SUPERSEDING  
MIL-PRF-19500/263B  
AMENDMENT 1  
19 January 2016

## PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, NPN, SILICON, HIGH POWER,  
THROUGH-HOLE MOUNT, TYPES 2N1714 THROUGH 2N1717,  
QUALITY LEVELS JAN, JANTX, AND JANTXV

Inactive for new design after 7 June 1999.

This specification is approved for use by all Departments  
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of  
this specification sheet and [MIL-PRF-19500](#).

### 1. SCOPE

\* 1.1 Scope. This specification covers the performance requirements for NPN, silicon, transistors for relatively high-power applications. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for all encapsulated device type as specified in [MIL-PRF-19500](#).

1.2 Package outlines. The device package outlines is a modified TO-5 (without a suffix symbol) or a modified TO-39 (with suffix S, see [1.5.3](#)) in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified,  $T_A = +25^\circ\text{C}$ .

Types	$P_c$ (1) $T_A = +25^\circ\text{C}$	$P_c$ (2) $T_c = +100^\circ\text{C}$	$V_{EB}$	$I_c$	$R_{\theta JX}$	$T_J$	$T_{STG}$	Alt.
	mW	W	V dc	A dc	$^\circ\text{C}/\text{W}$	$^\circ\text{C}$	$^\circ\text{C}$	Ft.
All	800	10	6.0	0.75	7.5	+175	-65 to +200	100,000

- (1) This power dissipation at ambient, free-air temperature of  $+25^\circ\text{C}$ . For ambient, free-air temperatures between  $+25^\circ\text{C}$  and  $+175^\circ\text{C}$ , derate linearly at rate of  $5.33 \text{ mW}/^\circ\text{C}$ .
- (2) This power dissipation at case temperature of  $+100^\circ\text{C}$ . For case temperatures between  $+100^\circ\text{C}$  and  $+175^\circ\text{C}$ , derate linearly at rate of  $134 \text{ mW}/^\circ\text{C}$ .

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



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1.4 Primary electrical characteristics. Unless otherwise specified,  $T_A = +25^\circ\text{C}$ .

Limits	h <sub>FE</sub> (1) V <sub>CE</sub> = 5 V dc I <sub>C</sub> = 10 mA dc		h <sub>FE</sub> (1) V <sub>CE</sub> = 5 V dc I <sub>C</sub> = 200 mA dc		V <sub>EBF</sub> V <sub>CB</sub> = 60 V dc	V <sub>EBF</sub> V <sub>CB</sub> = 100 V dc	V <sub>(BR)CEO</sub> (1) I <sub>C</sub> = 30 mA dc, I <sub>B</sub> = 0	
	2N1714 2N1715	2N1716 2N1717	2N1714 2N1715	2N1716 2N1717	2N1714 2N1716	2N1715 2N1717	2N1714 2N1716	2N1715 2N1717
Minimum	10	20	20	40	V dc ---	V dc ---	V dc 60	V dc 100
Maximum			60	120	1.0	2.0		

Limits	I <sub>CES</sub> V <sub>CE</sub> = 60 V dc V <sub>BE</sub> = 0		I <sub>CES</sub> V <sub>CE</sub> = 90 V dc V <sub>BE</sub> = 0	I <sub>CES</sub> V <sub>CE</sub> = 150 V dc V <sub>BE</sub> = 0
	2N1714 2N1715	2N1716 2N1717	2N1714 2N1716	2N1715 2N1717
Minimum	μA dc	μA dc	μA dc	μA dc
Maximum	2.0	2.0	50	50

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".

1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "1714", "1715", "1716", and "1717".

1.5.3 Suffix symbols. The suffix letter "S" is used on devices that have a shortened lead length: 0.5 inch (12.7 mm) minimum to .75 inch (19.1 mm) maximum. Devices with standard length leads (see figure 1) use no suffix symbol.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

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2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements for the transistor shall be as specified in MIL-PRF-19500 and as specified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML-19500) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I <sub>bc</sub>	Forward biased, base-collector current, dc, emitter open (current flow in forward direction).
P <sub>c</sub>	Collector power dissipation.

3.4 Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and herein. The device package style is either a modified TO-5 or a modified TO-39 in accordance with figure 1 for all device types.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein. Where a choice of lead finish or formation is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin-out. The pin-out of the device types shall be as shown on figure 1. Terminal 1 is the emitter, terminal 2 is the base, and terminal 3 is the collector. The collector shall be electrically connected to the case.

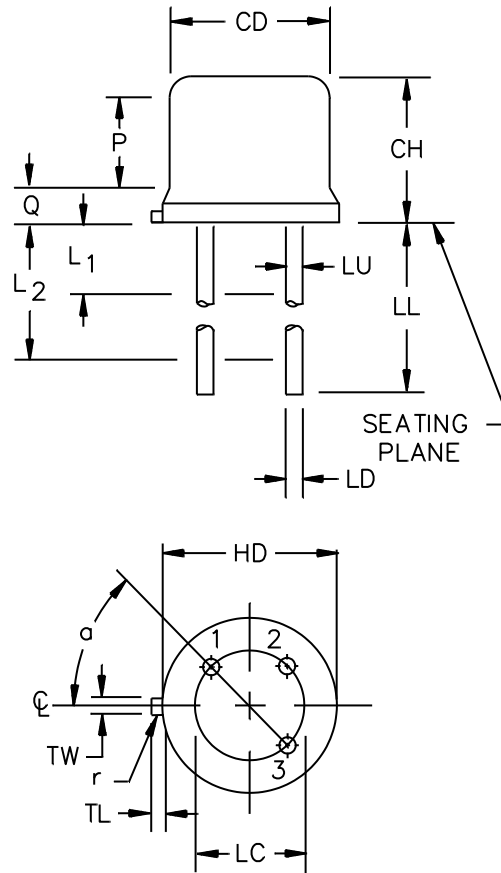
3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics shall be as specified in 1.3, 1.4, and table I herein.

3.7 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

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Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	3
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		4
LD	.016	.021	0.41	0.53	5, 6
LL	See notes 6, 7, and 8				
LU	.016	.019	0.41	0.48	5, 6
L <sub>1</sub>		.050		1.27	5, 6
L <sub>2</sub>	.250		6.35		5, 6
P	.100		2.54		9
Q		.050		1.27	
TL	.029	.045	0.74	1.14	10, 11
TW	.028	.034	0.71	0.86	10
r		.010		0.25	12
α	45° TP		45° TP		4



NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Lead 1 = emitter, lead 2 = base, lead 3 = collector. The collector shall be internally connected to the case.
3. Dimension CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
4. Leads at gauge plane .054 +.001 –.000 inch (1.37 +0.03 –0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
5. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between dimensions L<sub>2</sub> and LL minimum. Diameter is uncontrolled in and beyond dimension LL minimum.
6. All three leads.
7. For the modified TO-5 package (PINs without the S suffix), dimension LL is 1.500 inch (38.10 mm) minimum and 1.750 inch (44.45 mm) maximum.
8. For the modified TO-39 package (PINs with the S suffix), dimension LL is .500 inch (12.70 mm) minimum and .750 inch (19.05 mm) maximum.
9. Body contour optional within zone defined by dimensions HD, CD, and Q.
10. Beyond dimension r (radius) maximum, dimension TW shall be held for a minimum length of .011 (0.28 mm).
11. Dimension TL measured from maximum dimension HD.
12. Dimension r (radius) applies to both inside corners of tab.
13. In accordance with ASME Y14.5, diameters are equivalent to  $\Phi$ x symbology.

FIGURE 1. Physical dimensions and configuration of modified TO-5 or TO-39 package.

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#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANTX and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement
3c (1)	Transient thermal impedance, method 3131 of MIL-STD-750 (see 4.5.5)
10	48 hours minimum
11	ICBO <sub>2</sub> ; hFE <sub>2</sub>
12	Burn-in, see 4.3.1
13	Subgroup 2 of table I herein; $\Delta I_{CBO} = 100$ percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE2} = \pm 15$ percent

(1) Shall be performed anytime after temperature cycling (screen 3a). Does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:  $V_{CB} = 10$  to 30 V dc. Power shall be applied to achieve  $T_J = +135^\circ\text{C}$  minimum using a minimum  $P_D = 75$  percent of  $P_T$  maximum,  $T_A$  ambient rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions,  $T_J$ , and mounting conditions) may be used for quality levels JANTX and JANTXV. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

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4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIC (small die flow) of [MIL-PRF-19500](#) and herein.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state operating life: 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in 1.3. $n = 45$ devices, $c = 0$ . The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, $T_A = +150^\circ\text{C}$ , $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$ .
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$ . $n = 22$ , $c = 0$ .

4.4.2.1 Sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. Samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot.
- b. Samples shall be selected from an inspection lot that has been submitted to and passed [table I](#), subgroup 2, conformance inspection. When the final lead finish is solder, or any plating prone to oxidation at high temperature, the samples for life test may be tested prior to the application of final lead finish.
- c. Separate samples may be used for each step.

4.4.2.2 Failures. In the event of a lot failure, the resubmission requirements of [MIL-PRF-19500](#) shall apply. In addition, all catastrophic failures during conformance inspection shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows herein.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition E.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

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4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse response measurements. The conditions for pulse response measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Pulse conditions for particular tests. The following tests shall be performed in the necessary circuit with a pulse width = 300  $\mu$ sec and a duty cycle = 2.0 percent applied:

- Collector-to-emitter breakdown voltage
- Static forward-current transfer ratio
- Base-to-emitter voltage
- Collector-to-emitter, saturation voltage

4.5.3 Base-to-emitter voltage test. The specified currents shall be applied to applicable terminals under the conditions specified (see 4.5.2 herein), and the base-to-emitter voltage shall then be measured. (The data in method 3066, test condition A, of [MIL-STD-750](#) may be referred to as a guide for test procedure.)

4.5.4 Case-temperature control for  $|h_{fe}|$  test. To maintain the case temperature at less than +40°C for this test, the specified d-c collector current should be applied for not longer than 10 seconds without employing a heat sink.

4.5.5 Transient thermal impedance. The transient thermal impedance measurements shall be performed in accordance with test method 3131 of [MIL-STD-750](#) using the guidelines in that test method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{sw}$ , (and  $V_H$  where appropriate). See [table II](#), subgroup 4 herein.

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\* TABLE I. Group A inspection.

Inspection <a href="#">1/</a>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u> <a href="#">2/</a>						
Visual and mechanical examination	2071					
Solderability <a href="#">3/</a>	2026	n = 15 leads, c = 0				
Resistance to solvents <a href="#">3/</a>	1022	n = 15 devices, c = 0				
Salt atmosphere	1041	n = 6, c = 0 (for laser marked devices only)				
Temp cycling <a href="#">3/</a>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal Fine leak Gross leak	1071	n = 22 devices, c = 0				
End-point electrical measurements		Table I, subgroup 2				
Bond strength <a href="#">3/</a>	2037	Precondition T <sub>A</sub> = +250°C at t = 24 hrs or T <sub>A</sub> = 300°C at t = 2 hrs n = 11 wires, c = 0				
<u>Subgroup 2</u>						
Transient thermal impedance <a href="#">5/</a>	3131	See <a href="#">4.5.5</a>	R <sub>θJX</sub>		7.5	°C/W
Collector to emitter cutoff current	3041	Bias condition C, V <sub>CE</sub> = 60 V dc, V <sub>EB</sub> = 0	I <sub>CES</sub>		2.0	μA dc
Collector to emitter cutoff current 2N1714, 2N1716 2N1715, 2N1717	3041	Bias condition C, V <sub>EB</sub> = 0  V <sub>CE</sub> = 90 V dc, V <sub>CE</sub> = 150 V dc,	I <sub>CES</sub> I <sub>CES</sub>		50 50	μA dc μA dc
Collector to emitter cutoff current 2N1714, 2N1716 2N1715, 2N1717	3041	Bias condition D, I <sub>B</sub> = 0  V <sub>CE</sub> = 50 V dc V <sub>CE</sub> = 90 V dc	I <sub>CEO</sub> I <sub>CEO</sub>		50 50	μA dc μA dc

See footnotes at end of table.



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\* TABLE I. Group A inspection – Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2 - continued</u>						
Collector to base, cutoff current	3036	Bias condition D, $V_{CB} = 3 \text{ V dc}$ , $I_E = 0$	$I_{CBO}$		1.0	$\mu\text{A dc}$
Emitter to base, cutoff current	3061	Bias condition D, $V_{EB} = 3 \text{ V dc}$ , $I_C = 0$	$I_{EBO}$		10	$\mu\text{A dc}$
Emitter to base, cutoff current	3061	Bias condition D, $V_{EB} = 6 \text{ V dc}$ , $I_C = 0$	$I_{EBO}$		10	$\mu\text{A dc}$
Collector to emitter breakdown voltage 2N1714, 2N1716 2N1715, 2N1717	3011	Bias condition D, $I_C = 30 \text{ mA dc}$ , $I_B = 0$ , (see 4.5.2)	$V_{(BR)CEO}$ $V_{(BR)CEO}$		60 100	V dc V dc
Floating potential  2N1714, 2N1716 2N1715, 2N1717	3020	Voltmeter input resistance $\geq 10$ Meg. $V_{CB} = 60 \text{ V dc}$ $V_{CB} = 100 \text{ V dc}$	$V_{EBF}$ $V_{EBF}$		1.0 2.0	V dc V dc
Forward-current transfer ratio 2N1714, 2N1715 2N1716, 2N1717	3076	$V_{CE} = 5 \text{ V dc}$ , $I_C = 10 \text{ mA dc}$ ; (see 4.5.2)	$h_{FE1}$ $h_{FE1}$	10 20		
Forward-current transfer ratio 2N1714, 2N1715 2N1716, 2N1717	3076	$V_{CE} = 5 \text{ V dc}$ , $I_C = 200 \text{ mA dc}$ ; (see 4.5.2)	$h_{FE2}$ $h_{FE2}$	20 40	60 120	
Base emitter voltage (saturated)	3066	Test condition A, $I_C = 200 \text{ mA dc}$ , $I_B = 20 \text{ mA dc}$ (see 4.5.2 and 4.5.3)	$V_{BE}$		1.6	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 200 \text{ mA dc}$ , $I_B = 20 \text{ mA dc}$ (see 4.5.2)	$V_{CE(sat)}$	---	2.0	V dc
<u>Subgroup 3</u>						
High temperature operation		$T_A = +175^\circ\text{C}$ , $+5^\circ\text{C}$ , $-0^\circ\text{C}$				
Collector to emitter cutoff current	3041	Bias condition C; $V_{CE} = 60 \text{ V dc}$ , $V_{EB} = 0$	$I_{CES}$		500	$\mu\text{A dc}$
Low temperature operation		$T_A = -55^\circ\text{C}$ , $-5^\circ\text{C}$ , $+0^\circ\text{C}$				
Forward-current transfer ratio 2N1714, 2N1715 2N1716, 2N1717	3076	$V_{CE} = 5 \text{ V dc}$ , $I_C = 200 \text{ mA dc}$ , (see 4.5.2)	$h_{FE3}$ $h_{FE3}$	10 20		

See footnotes at end of table.

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\* TABLE I. Group A inspection – Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Magnitude of common emitter small-signal, short-circuit forward-current transfer ratio	3306	$f = 16 \text{ MHz}$ , $V_{CE} = 10 \text{ V dc}$ , $I_C = 100 \text{ mA dc}$ (see <a href="#">4.5.4</a> )	$ h_{FE} $		1.0	
Output capacitance (open circuit, common base)	3236	$f = 1 \text{ MHz}$ , $V_{CB} = 10 \text{ V dc}$ , $I_E = 0$	$C_{ob}$		50	pf
<u>Subgroups 5, 6 and 7</u>						
Not applicable						

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in subgroup 1 of table I shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for laser marked devices.

5/ For end-point measurements, this test is required for the following subgroups:

Group B, step 1 for quality levels JAN, JANTX, JANTXV.

Group C, subgroups 2 and 6 for all quality levels.

Group E, subgroup 1 for all quality levels.

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TABLE II. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071		
End-point electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Steady-state operating life	1027	T <sub>A</sub> = 25°C, P <sub>T</sub> = 0.8 W, V <sub>CE</sub> = 40 V dc, t = 340 hours.	
End-point electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See <a href="#">MIL-PRF-19500</a> .	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	
<u>Subgroup 9</u>			
Burnout by pulsing	3005	Pre-pulse condition: T <sub>C</sub> = 100°C, I <sub>BC</sub> = 0, I <sub>E</sub> = 0.  Pulse condition: T <sub>C</sub> ≤ 100°C, I <sub>BC</sub> = 750 mA dc, I <sub>E</sub> = 0, tp = 30 ± 5 seconds, 1 cycle.	

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## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of material is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

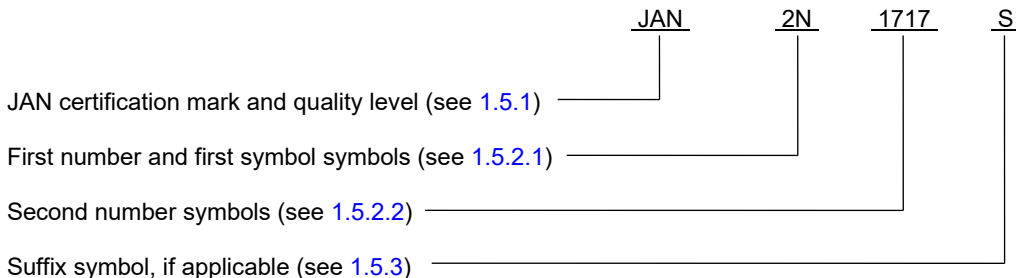
6.1 Intended use. Transistors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5, 6.4, and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML-19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil).

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



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6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices in a modified TO-5 package (standard lead lengths)			PINs for devices in a modified TO-39 package (short lead lengths)		
JAN2N1714	JANTX2N1714	JANTXV2N1714	JAN2N1714S	JANTX2N1714S	JANTXV2N1714S
JAN2N1715	JANTX2N1715	JANTXV2N1715	JAN2N1715S	JANTX2N1715S	JANTXV2N1715S
JAN2N1716	JANTX2N1716	JANTXV2N1716	JAN2N1716S	JANTX2N1716S	JANTXV2N1716S
JAN2N1717	JANTX2N1717	JANTXV2N1717	JAN2N1717S	JANTX2N1717S	JANTXV2N1717S

6.6 Supersession information and superseded PINs.

6.6.1 Lead length. The original issue of this specification through MIL-S-19500/263(EL) with amendment 3 (26 June 1978) did not contain a suffix to designate lead length. MIL-S-19500/263(ER) with amendment 4 (5 May 1980) introduced the "S" suffix option with the associated TO-39 package. When applicable, PINs covering devices with a shortened lead length now shall include a suffix "S" to designate this package configuration (see 1.2, 1.5, and figure 1.)

\* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:  
Army - CR  
Air Force - 85  
\* NASA - NA  
DLA - CC

Preparing activity:  
DLA - CC  
  
(Project 5961-2021-040)

Review activities:  
Army - EA, MI  
\* Air Force - 70, 170

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.