The documentation and process conversion measures necessary to comply with this document shall be completed by 27 May 2024.

INCH-POUND
MIL-PRF-19500/496F
w/AMENDMENT 1
27 February 2024
SUPERSEDING
MIL-PRF-19500/496F
21 October 2018

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, UNITIZED DUAL, PNP, SILICON, TYPES 2N5795 AND 2N5796, RADIATION HARDNESS ASSURANCE, QUALITY LEVELS JAN, JANTX, JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for two electrically isolated, PNP silicon transistors as one dual unit for high speed saturated switching applications. Both matched and unmatched types are covered. Four levels of product assurance (JAN, JANTX, JANTXV and JANS) are provided for each device type as specified in MIL-PRF-19500. Provisions for radiation hardness assurance (RHA) are provided for JANTXV and JANS product assurance levels. RHA level designators "M", "D", "P", "L", "R", "F", "G" and "H" are appended to the device prefix to identify devices, which have passed RHA requirements.

1.2 Package outlines. The device package outlines are as follows: through hole mount TO-78 package in accordance with figure 1, surface mount LCC in accordance with figure 2 and ceramic lid surface mount LCC in accordance with figure 3.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

P_T (1) (2) T_A = +25°C		I_C	V_{CBO}	V_{CEO}	V_{EBO}	T_J and T_{STG}
One section	Total device					
W	W	mA dc	V dc	V dc	V dc	°C
0.5	0.6	-600	-60	-60	5.0	-65 to +175

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A

FSC 5961

1.3 Maximum ratings. - Continued.

Types	$R_{\theta JA}$ (2)		$R_{\theta JSP}$ (2)		$R_{\theta JPCB}$ (2)	
	One section	Both sections	One section	Both sections	One section	Both sections
	°C/W	°C/W	°C/W	°C/W	°C/W	°C/W
2N5795, 2N5796	350	290				
2N5795A, 2N5796A	350	290				
2N5796U, 2N5796UC			110	90	350	290
2N5796AU, 2N5796AUC			110	90	350	290

(1) For $T_A \geq 25°C$, derate linearly 2.86 mW/°C one section, 3.43 mW/°C total.
(2) For thermal impedance curves see figures 4, 5, and 6.

1.4 Primary electrical characteristics. Unless otherwise specified, T_A = +25°C.

1.4.1 Unmatched characteristics of each individual section.

	C_{obo} V_{CB} = -10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	$\lvert h_{fe} \rvert$ V_{CE} = -20 V dc I_C = 20 mA dc f = 100 MHz	Switching	
			t_{on}	t_{off}
	pF		ns	Ns
Minimum		2.0		
Maximum	8.0	10.0	50	140

Limits	h_{FE1} V_{CE} = -10 V dc I_C = -100 µA dc		h_{FE4} (1) V_{CE} = -10 V dc I_C = -150 mA dc		$V_{CE(SAT)1}$ (1) I_C = -150 mA dc I_B = -15 mA dc	$V_{CE(SAT)2}$ (1) I_C = -500 ma dc I_B = -50 mA dc	$V_{BE(SAT)1}$ (1) I_C = -150 mA dc I_B = -15 mA dc
	Min	Max	Min	Max	V dc	V dc	V dc
* 2N5795, 2N5795A	40		40	150	-0.4	-1.6	-1.3
* 2N5796, U, UC 2N5796A, AU, AUC	75		100	300	-0.4	-1.6	-1.3

(1) Pulsed see 4.5.1.

1.4.2 Matching characteristics of each individual section.

Limit	$\frac{h_{FE2-1}}{h_{FE2-2}}$	$\frac{h_{FE3-1}}{h_{FE3-2}}$	$\lvert V_{BE1} - V_{BE2} \rvert$
* 2N5795A 2N5796A, AU, AUC	V_{CE} = -10 V dc; I_C = -1 mA dc (1)	V_{CE} = -10 V dc; I_C = -10 mA dc (1)	V_{CE} = -10 V dc; I_C = -1 mA dc
			mV dc
Min	0.9	0.9	
* Max	1.1	1.1	-10

(1) The larger number will be replaced in the denominator

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

1.5.2 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.2.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are "5795" and "5796".

1.5.3 Suffix symbols. The following suffix symbol(s) are incorporated into the PINs for this specification sheet.

	A blank designator identifies that the package is a TO-78 in accordance with figure 1. The two individual sections are not matched.
A	The "A" designator indicates a version of the transistor that have matching characteristics of the individual sections and are packaged in a TO-78 in accordance with figure 1.
U	The "U" designator identifies devices that are packaged in a 6 terminal LLC (see figure 2). The two individual sections are not matched.
AU	The "AU" designator indicates a version of the transistor that have matching characteristics of the individual sections and are packaged in a 6 terminal LLC (see figure 2).
UC	The "UC" designator identifies that the package is a ceramic lid 6 terminal LCC (see figure 3). The two individual sections are not matched.
AUC	The "AUC" designator indicates a version of the transistor that have matching characteristics of the individual sections and are packaged in a ceramic lid 6 terminal LLC (see figure 3).

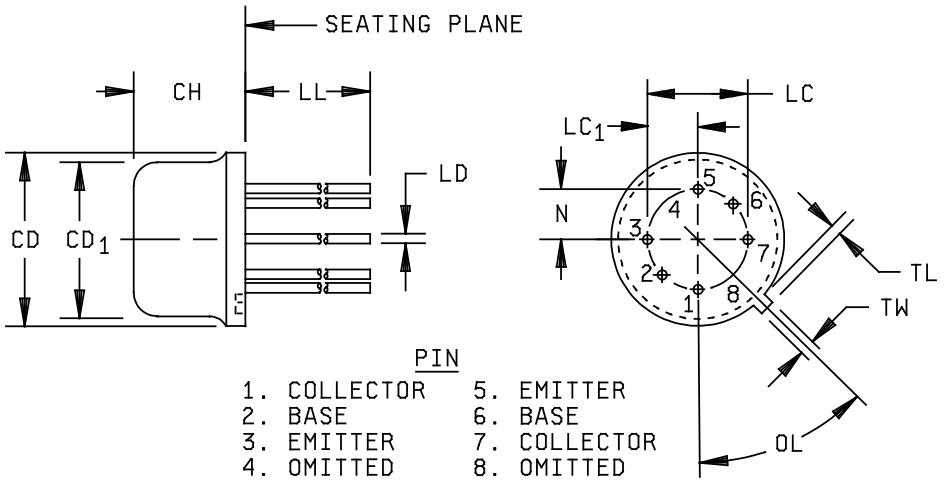
1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.6 Radiation features. The following radiation features are applicable for RHA devices supplied to this specification sheet.

* 1.6.1 Maximum total ionizing dose (TID). The maximum TID that RHA devices were tested to in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750 are as follows:

For device type 2N5795, 2N5795A: ..... 300 krads(Si) 1/
For device type 2N5796, U, UC, 2N5796A, AU, AUC: ..... 300 krads(Si) 1/

* 1/ The manufacturers supplying these device types have performed characterization testing in accordance with condition A (dose rate = 50 to 300 rad(Si)/s) of method 1019 of MIL-STD-750. The radiation end point limits are guaranteed only to a maximum TID level of 300 krads(Si).

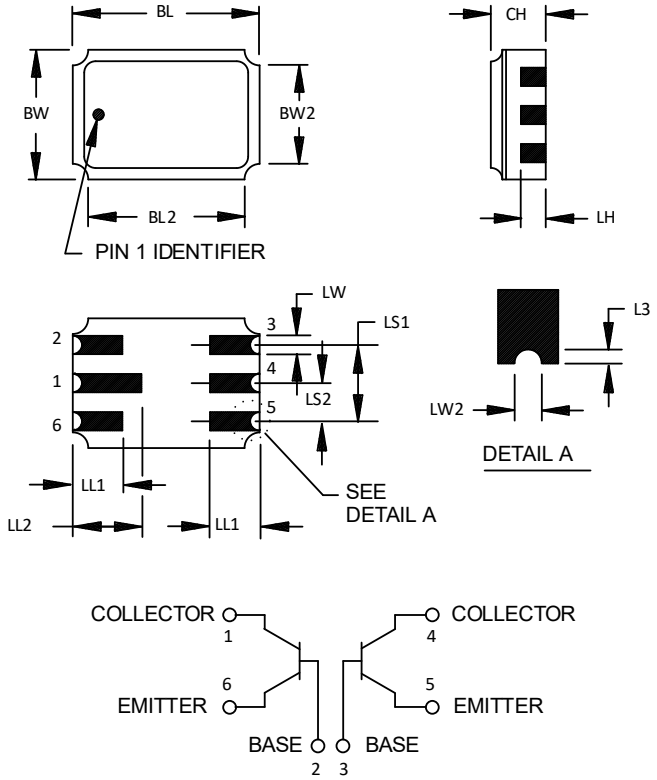


Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.335	.370	8.51	9.40	
CD_1	.305	.335	7.75	8.51	
CH	.150	.185	3.81	4.70	
LD	.016	.021	0.41	0.53	
LC	.200 BSC		5.08 BSC		3
LC_1	.100 BSC		2.54 BSC		3
LL	.500		12.70		
TW	.028	.034	0.71	0.86	
TL	.029	.045	0.74	1.14	4
OL	45° BSC		45° BSC		5
N	.100 BSC		2.54 BSC		

NOTES:

1. Dimension are in inches. Millimeters are given for general information only.
2. The product may be measured by direct methods or by gauge.
3. Leads having maximum diameter .019 inch (0.483 mm) measured in gaging plan .054 inch (1.37 mm) + .001 inch (0.025 mm) - .000 inch (0.000 mm) below the seating plane of the product shall be within .007 inch (.178 mm) of their true position relative to a maximum width tab.
4. Measured from maximum diameter of the product.
5. Tab centerline.

FIGURE 1. Physical dimensions for TO-78 package (2N5795, 2N5795A, 2N5796A and 2N5796).



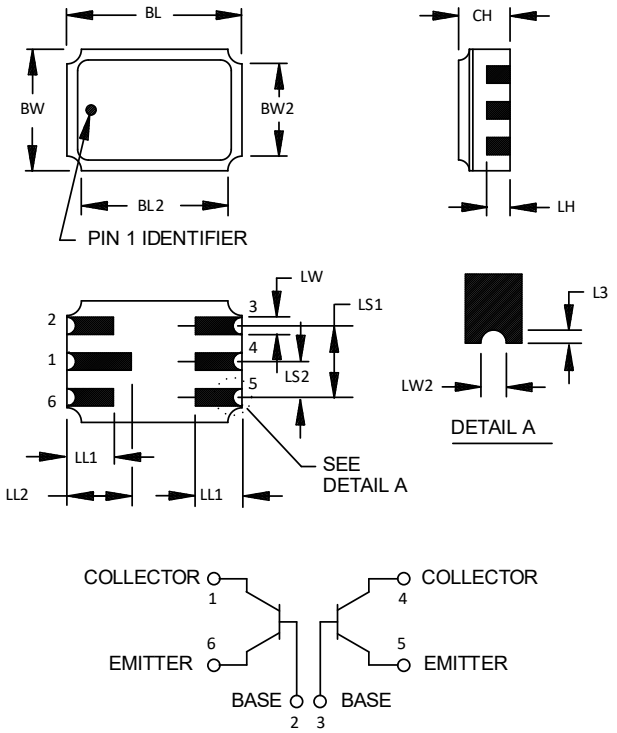
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL_2		.250		6.35
BW	.165	.175	4.19	4.45
BW_2		.175		4.45
CH	.058	.100	1.47	2.54
L_3	.003	.007	0.08	0.18
LH	.026	.039	0.66	0.99

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
LL_1	.060	.070	1.52	1.78
LL_2	.082	.098	2.08	2.49
LS_1	.095	.105	2.41	2.67
LS_2	.045	.055	1.14	1.40
LW	.022	.028	0.56	0.71
LW_2	.006	.022	0.15	0.56

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimension "CH" controls the overall package thickness.
3. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option from that shown on the drawing.
4. Dimensions "LW_2" minimum and "L_3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW_2" maximum and dimension "L_3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.

FIGURE 2. Physical dimensions for U package (2N5796U and 2N5796AU).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.240	.250	6.10	6.35
BL_2		.250		6.35
BW	.165	.175	4.19	4.45
BW_2		.175		4.45
CH	.058	.115	1.47	2.92
L_3	.003	.007	0.08	0.18
LH	.026	.039	0.66	0.99

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
LL_1	.060	.070	1.52	1.78
LL_2	.082	.098	2.08	2.49
LS_1	.095	.105	2.41	2.67
LS_2	.045	.055	1.14	1.40
LW	.022	.028	0.56	0.71
LW_2	.006	.022	0.15	0.56

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Dimension "CH" controls the overall package thickness and is ceramic.
3. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option from that shown on the drawing.
4. Dimensions "LW_2" minimum and "L_3" minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "LW_2" maximum and dimension "L_3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.

FIGURE 3. Physical dimensions for UC package (2N5796UC and 2N5796AUC ceramic lid).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods For Semiconductor Devices.

(Copies of these documents are available online at https://quicksearch.dla.mil.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-1950 and as follows.

$R_{\theta JA}$ ..... Thermal resistance junction to ambient.
$R_{\theta JC}$ ..... Thermal resistance junction to case.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and figures 1 (similar to TO-78), 2 (six pin LLC), and 3 (six pin ceramic lid LLC) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin-out. The pin-out of the device shall be as shown on figures 1, 2, and 3 as applicable.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-1950 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (quality levels JANS, JANTX, and JANTXV only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
9	I_{CBO2} and h_{FE4}	Not applicable
10	48 hours minimum	48 hours minimum
11	I_{CBO2} and h_{FE4}; Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent of initial value	I_{CBO2} and h_{FE4}
12	See 4.3.1	See 4.3.1
13	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent of initial value.	Subgroup 2 of table I herein; ΔI_{CBO2} = 100 percent of initial value or 5 nA dc, whichever is greater. Δh_{FE4} = ±15 percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a and does not need to be repeated for quality levels JANTX and JANTXV in screening requirements.

* 4.3.1 Burn-in conditions. Burn-in conditions shall be as follows: V_{CB} = -10 - -30 V dc; power shall be applied to achieve T_J = +135°C minimum using P_T = 300 mW each section (600 mW total device). T_A = ambient rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW} , t_{MD} (V_C and V_H where appropriate). See table III, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-1950, a sample of screened devices shall be submitted to and pass the requirements of subgroup 1 and 2, of table I herein, inspection only (table E-VIB, group B, subgroup 1 is not required to be performed since solderability and resistance to solvents testing is performed in table I herein).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-1950, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with 4.4.2.1 for quality level JANS and 4.4.2.2 for quality levels JAN, JANTX, and JANTXV.

4.4.2.1 Quality level JANS. Group B inspection for quality level JANS shall be conducted in accordance with the conditions specified for subgroup testing in table E–VIA of MIL-PRF-19500 and herein.

	Subgroup	Method	Condition
*	B4	1037	V_{CB} = -10 V dc, adjust device current, or power, to achieve a minimum ΔT_J of 100°C.
*	B5	1027	V_{CB} = -10 V dc; $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIA, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours minimum, sample size = 45, c = 0; adjust T_A or P_D to achieve a T_J = +225°C minimum.

4.4.2.2 Quality levels JAN, JANTX, and JANTXV. Group B inspection for quality levels JAN, JANTX, and JANTXV shall be conducted in accordance with the conditions specified in table E–VIC (small die flow) of MIL-PRF-19500 and herein.

	Step	Method	Condition
*	1	1026	Steady-state life: 1,000 hours minimum, V_{CB} = -10 V dc, power shall be applied to achieve T_J = +150°C minimum using a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3. n = 45 devices, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
	2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
	3	1032	High-temperature life (non-operating), t = 340 hours, T_A = +175°C. n = 22, c = 0.

4.4.2.2.1 Sample selection. Samples selected for small die flow group B inspection shall be in accordance with all of the following requirements:

a. Samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot (see MIL-PRF-19500).

b. Samples shall be selected from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test may be tested prior to the application of final lead finish.

c. Separate samples may be used for each step.

4.4.2.2.2 Failures. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during small die flow group B inspection shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in 4.4.3.1 (JANS) or 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing.

4.4.3.1 Quality level JANS.

	Subgroup	Method	Condition
	C2	2036	Test condition E; (not applicable for U, UC, and AUC device).
	C5	3131	$R_{\theta JA}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
*	C6	1026	1,000 hours at V_{CB} = -10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Quality levels JAN, JANTX, and JANTXV.

Subgroup	Method	Condition
C2	2036	Test condition E, (not applicable for U, UC, and AUC devices).
C5	3131	$R_{\theta JA}$ only, as applicable (see 1.3) and in accordance with thermal impedance curves.
C6		Not applicable.

4.4.3.3 Sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. The conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical examination 3/	2071	n = 45 devices, c = 0				
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ 6/	1071	n = 22 devices, c = 0				
Fine leak						
Gross leak						
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hours or T_A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance 7/	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to base cutoff current	3036	Bias condition D, V_{CB} = -60 V dc	I_{CBO1}		-10	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = -10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-60		V dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO1}		-10	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = -50 V dc	I_{CBO2}		-10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 3 V dc	I_{EBO2}		-100	nA dc
Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -0.1 mA dc	h_{FE1}			
2N5795 8/				40		
2N5796 8/				75		
Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -1.0 mA dc	h_{FE2}			
2N5795 8/				40		
2N5796 8/				100		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio 2N5795 8/ 2N5796 8/	3076	V_{CE} = -10 V dc; I_C = -10 mA dc; pulsed (see 4.5.1)	h_{FE3}	 40 100		
Forward-current transfer ratio 2N5795 8/ 2N5796 8/	3076	V_{CE} = -10 V dc; I_C = -150 mA dc; pulsed (see 4.5.1)	h_{FE4}	 40 100	 150 300	
Forward-current transfer ratio 2N5795 8/ 2N5796 8/	3076	V_{CE} = -10 V dc; I_C = -300 mA dc; pulsed (see 4.5.1)	h_{FE5}	 20 50		
Forward-current transfer ratio 2N5795 8/ 2N5796 8/	3076	V_{CE} = -1.0 V dc; I_C = -150 mA dc; pulsed (see 4.5.1)	h_{FE6}	 20 50		
Collector-emitter saturation voltage	3071	I_C = -150 mA dc; I_B = -15 mA dc pulsed (see 4.5.1)	$V_{CE(sat)1}$		-0.4	V dc
Collector-emitter saturation voltage	3071	I_C = -500 mA dc; I_B = -50 mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		-1.6	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = -150 mA dc; I_B = -15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.3	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = -500 mA dc; I_B = -50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.6	V dc
Forward-current transfer ratio (gain ratio) 9/	3076	V_{CE} = -10 V dc; I_C = -1 mA dc; pulsed (see 4.5.1)	$\frac{h_{FE2-1}}{h_{FE2-2}}$	0.9	1.1	
Forward-current transfer ratio (gain ratio) 9/	3076	V_{CE} = -10 V dc; I_C = -10 mA dc; pulsed (see 4.5.1)	$\frac{h_{FE3-1}}{h_{FE3-2}}$	0.9	1.1	
Absolute value of base emitter-voltage differential 9/	3066	Test condition B; V_{CE} = -10 V dc; I_C = -1 mA dc	$\lvert V_{BE1} - V_{BE2} \rvert$		-10	mV dc
Subgroup 3						
High temperature operation		T_A = +150°C				
Collector to base cutoff current	3036	Bias condition D; V_{CB} = -50 V dc	I_{CBO3}		-10	µA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 3 - continued.						
Low temperature operation		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -150 mA dc	h_{FE7}			
2N5795 8/				16		
2N5796 8/				40		
Subgroup 4						
Magnitude of small-signal short- circuit forward current transfer ratio	3306	V_{CE} = -20 V dc; I_C = -20 mA dc; f = 100 MHz	$\lvert h_{fe} \rvert$	2	10	
Open circuit output capacitance	3236	V_{CB} = -10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		8	pF
Input capacitance (output open- circuited)	3240	V_{EB} = -2.0 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz	C_{ibo}		30	pF
Pulse response	3251	Test condition A, (see figure 7)				
Saturated turn-on time		V_{CC} = -30 V dc; I_C = -150 mA dc; I_{B1} = 15 mA dc, $V_{BE(OFF)}$ = 0.5 V dc	t_{on}		50	ns
Saturated turn-off time		V_{CC} = -30 V dc; I_C = -150 mA dc; I_{B1} = I_{B2} =15 mA dc	t_{off}		140	ns
Subgroups 5						
Collector one to collector two leakage current		$V_{(1C–2C)}$ = ±50 V dc.	$1_{(1C–2C)}$		±1	nA dc

1/ For sampling plan see MIL-PRF-19500.
2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be repeated upon submission.
3/ Separate samples may be used.
4/ Not required for JANS devices.
5/ Not required for laser marked devices.
6/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.
7/ For end-point electrical measurements, this test is required for the following subgroups:
Group B, subgroups 3, 4 and 5 (JANS).
Group B, step 1(JAN, JANTX, JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.
8/ Includes all suffix designators for the device type (non-matching, matching or package suffixes as applicable).
9/ For matching device types only (e.g. 2N5795A, 2N5796A, 2N5796AU and 2N5796AUC).

TABLE II. Group D inspection.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 1 3/						
Neutron irradiation Collector to base cutoff current	1017 3036	Neutron exposure V_{CES} = 0 V Bias condition D; V_{CB} = -60 V dc	I_{CBO1}		-20	µA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = -10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-60		V dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 5 V dc	I_{EBO1}		-20	µA dc
Collector to base cutoff current	3036	Bias condition D; V_{CB} = -50 V dc	I_{CBO2}		-20	nA dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 3 V dc	I_{EBO2}		-200	nA dc
Forward-current transfer ratio 2N5795 5/ 2N5796 5/	3076	V_{CE} = -10 V dc; I_C = -0.1 mA dc	[h_{FE1}] 4/	 [20] [37.5]		
Forward-current transfer ratio 2N5795 5/ 2N5796 5/	3076	V_{CE} = -10 V dc; I_C = -1.0 mA dc	[h_{FE2}] 4/	 [20] [50]		
Forward-current transfer ratio 2N5795 5/ 2N5796 5/	3076	V_{CE} = -10 V dc; I_C = -10 mA dc	[h_{FE3}] 4/	 [20] [50]		
Forward-current transfer ratio 2N5795 5/ 2N5796 5/	3076	V_{CE} = -10 V dc; I_C = -150 mA dc	[h_{FE4}] 4/	 [20] [50]	 150 300	
Forward-current transfer ratio 2N5795 5/ 2N5796 5/	3076	V_{CE} = -10 V dc; I_C = -300 mA dc	[h_{FE5}] 4/	 [10] [25]		
Forward-current transfer ratio 2N5795 5/ 2N5796 5/	3076	V_{CE} = -1.0 V dc; I_C = -150 mA dc	[h_{FE6}] 4/	 [10] [25]		
* Collector-emitter saturation voltage	3071	I_C = -150 mA dc; $-I_B$ = -15 mA dc	$V_{CE(sat)1}$		-0.46	V dc
Collector-emitter saturation voltage	3071	I_C = -500 mA dc; I_B = -50 mA dc	$V_{CE(sat)2}$		-1.84	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = -150 mA dc; I_B = -15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.50	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = -500 mA dc; I_B = -50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.99	V dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

	Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
		Method	Conditions		Min	Max	
	Subgroup 1 - Continued. 3/						
*	Forward-current transfer ratio (gain ratio) 6/	3076	V_{CE} = -10 V dc; I_C = -1 mA dc; pulsed (see 4.5.1)	$\frac{h_{FE3-1}}{h_{FE3-2}}$	0.8	1.2	
*	Forward-current transfer ratio (gain ratio) 6/	3076	V_{CE} = -10 V dc; I_C = -10 mA dc; pulsed (see 4.5.1)	$\frac{h_{FE3-1}}{h_{FE3-2}}$	0.8	1.2	
*	Absolute value of base emitter-voltage differential 6/	3066	Test condition B; V_{CE} = -10 V dc; I_C = -1 mA dc	$\lvert V_{BE1} - V_{BE2} \rvert$		20	mV dc
	Subgroup 2 3/						
	Total dose irradiation	1019	Gamma exposure V_{CES} = -40 V; Condition A				
	Collector to base cutoff current	3036	Bias condition D; V_{CB} = -60 V dc	I_{CBO1}		-20	µA dc
	Breakdown voltage, collector to emitter	3011	Bias condition D; I_C = -10 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
	Emitter to base cutoff current	3061	Bias condition D; V_{EB} = -5 V dc	I_{EBO1}		-20	µA dc
	Collector to base cutoff current	3036	Bias condition D; V_{CB} = -50 V dc	I_{CBO2}		-20	nA dc
	Emitter to base cutoff current	3061	Bias condition D; V_{EB} = -3 V dc	I_{EBO2}		-200	nA dc
	Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -0.1 mA dc	[h_{FE1}] 4/			
	2N5795 5/				[20]		
	2N5796 5/				[37.5]		
	Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -1.0 mA dc	[h_{FE2}] 4/			
	2N5795 5/				[20]		
	2N5796 5/				[50]		
	Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -10 mA dc	[h_{FE3}] 4/			
	2N5795 5/				[20]		
	2N5796 5/				[50]		
*	Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = 150 mA dc	[h_{FE4}] 4/			
	2N5795 5/				[20]	150	
	2N5796 5/				[50]	300	
	Forward-current transfer ratio	3076	V_{CE} = -10 V dc; I_C = -300 mA dc	[h_{FE5}] 4/			
	2N5795 5/				[10]		
	2N5796 5/				[25]		
	Forward-current transfer ratio	3076	V_{CE} = -1.0 V dc; I_C = -150 mA dc	[h_{FE6}] 4/			
	2N5795 5/				[10]		
	2N5796 5/				[25]		

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued. 3/						
Collector-emitter saturation voltage	3071	I_C = -150 mA dc; I_B = -15 mA dc	$V_{CE(sat)1}$		-.46	V dc
Collector-emitter saturation voltage	3071	I_C = -500 mA dc; I_B = -50 mA dc	$V_{CE(sat)2}$		-1.84	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = -150 mA dc; I_B = -15 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.50	V dc
Base-emitter saturation voltage	3066	Test condition A; I_C = -500 mA dc; I_B = -50 mA dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-2.99	V dc
Forward-current transfer ratio (gain ratio) 6/	3076	V_{CE} = 10 V dc; I_C = 1 mA dc; pulsed (see 4.5.1)	$\frac{h_{FE2-1}}{h_{FE2-2}}$	0.8	1.2	
Forward-current transfer ratio (gain ratio) 6/	3076	V_{CE} = 10 V dc; I_C = 10 mA dc; pulsed (see 4.5.1)	$\frac{h_{FE3-1}}{h_{FE3-2}}$	0.8	1.2	
Absolute value of base emitter-voltage differential 6/	3066	Test condition B; V_{CE} = 10 V dc; I_C = 1 mA dc	$\lvert V_{BE1} - V_{BE2} \rvert$		20	mV dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ See 6.2.e herein.
4/ See method 1019 of MIL-STD-750 to determine [h_{FE}] by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE}. The [h_{FE}] is not the same as h_{FE} and cannot be measured directly. The [h_{FE}] value can never exceed the pre-radiation minimum h_{FE} that it is based upon.
5/ Includes all suffix designators for the device type (non-matching, matching or package suffixes as applicable).
6/ For all matching device types only (2N5795A, 2N5796A, 2N5796AU and 2N5796AUC).

TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sampling plan
	Method	Conditions	
Subgroup 1			45 devices
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	c = 0
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	Intermittent operation life: V_{CB} = 10 V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 4			
Thermal impedance curves		See table E-IX of MIL-PRF-19500, subgroup 4.	
Subgroup 5			
Not applicable			
Subgroup 6			11 devices c = 0
Electrostatic discharge (ESD)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	

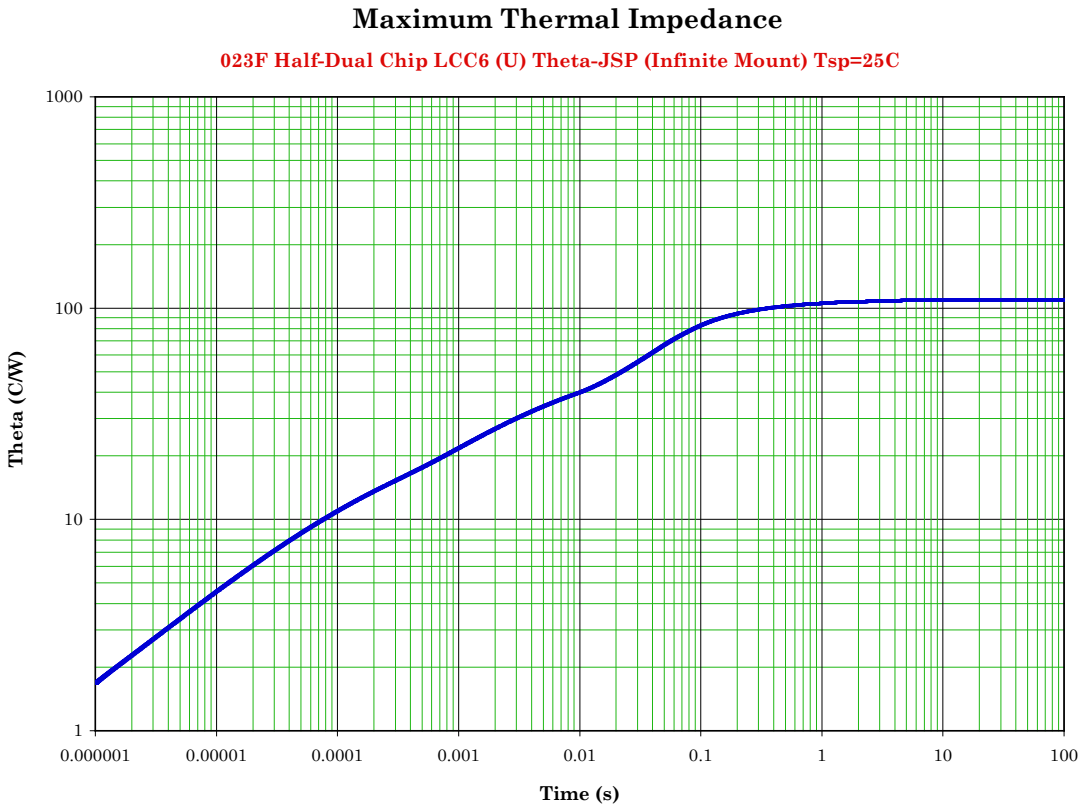


FIGURE 4. Thermal impedance graph ($R_{\theta JSP}$) for 2N5796U, 2N5796UC, 2N5796AU, and 2N5796AUC (U and UC).

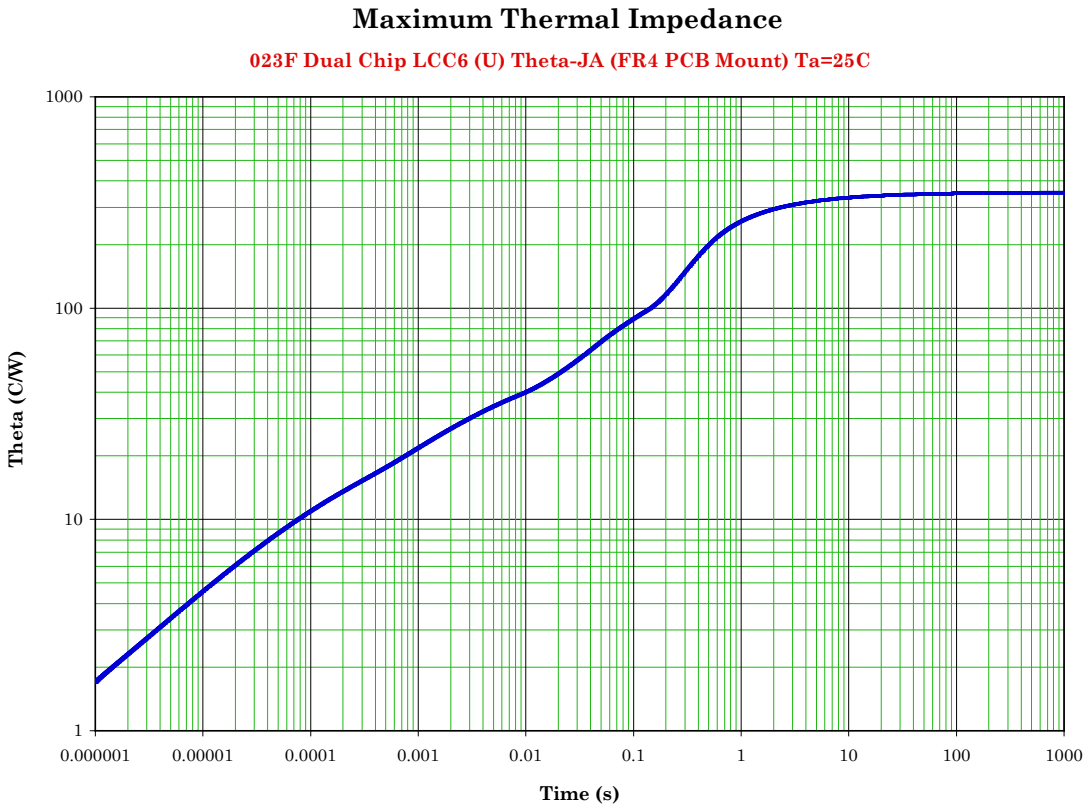


FIGURE 5. Thermal impedance graph ($R_{\theta JPCB}$) for 2N5796U, 2N5796UC, 2N5796AU, and 2N5796AUC (U and UC).

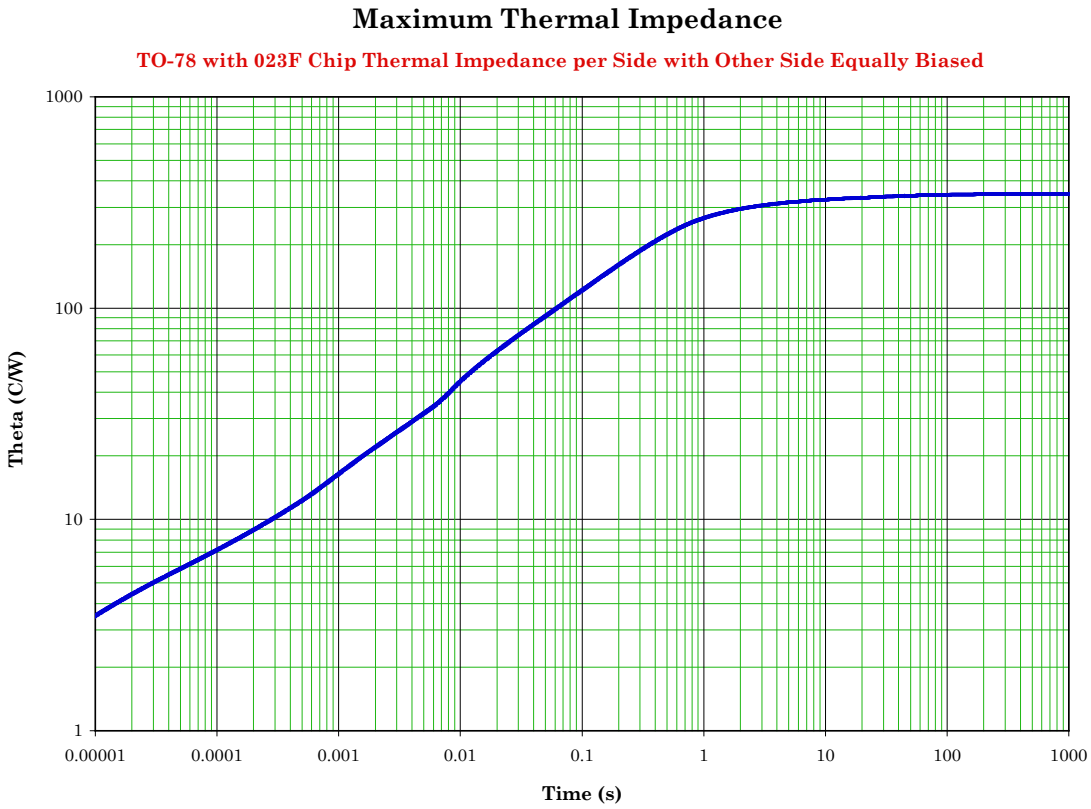
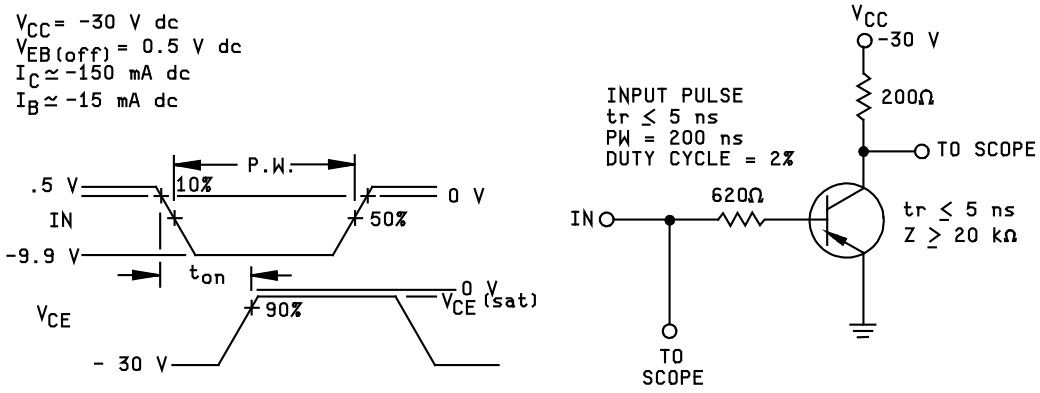
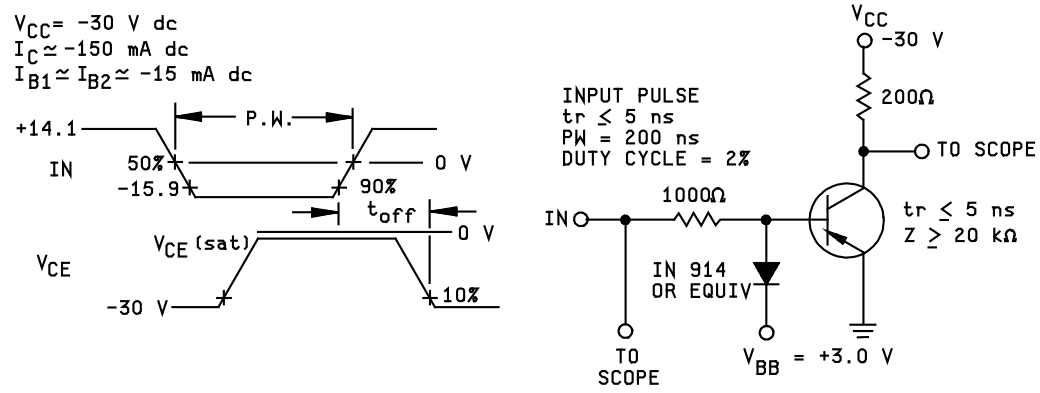


FIGURE 6. Thermal impedance graph ($R_{\theta JA}$) for 2N5795, 2N5796, 2N5795A and 2N5796A,



TURN-ON (t_{on}) TIME TEST CIRCUIT



TURN-ON (t_{off}) TIME TEST CIRCUIT

FIGURE 7. Turn-off time test circuits.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

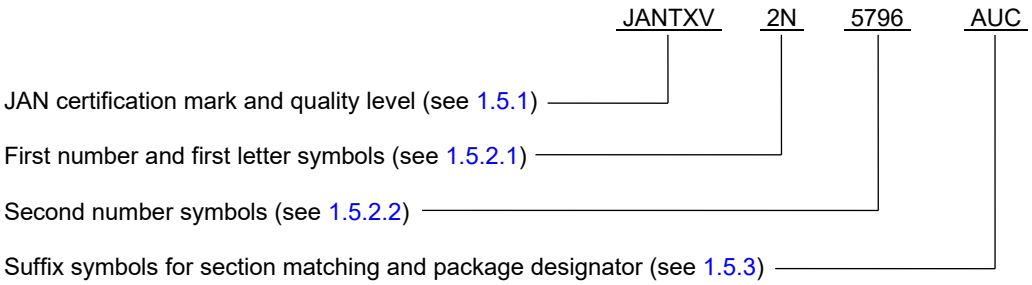
c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

e. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it should be specified in the contract.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

Quality level JAN	Quality level JANTX	Quality level JANTXV	Quality level JANS
JAN2N5795	JANTX2N5795	JANTXV2N5795	JANS2N5795
JAN2N5795A	JANTX2N5795A	JANTXV2N5795A	JANS2N5795A
JAN2N5796	JANTX2N5796	JANTXV2N5796	JANS2N5796
JAN2N5796U	JANTX2N5796U	JANTXV2N5796U	JANS2N5796U
JAN2N5796UC	JANTX2N5796UC	JANTXV2N5796UC	JANS2N5796UC
JAN2N5796A	JANTX2N5796A	JANTXV2N5796A	JANS2N5796A
JAN2N5796AU	JANTX2N5796AU	JANTXV2N5796AU	JANS2N5796AU
JAN2N5796AUC	JANTX2N5796AUC	JANTXV2N5796AUC	JANS2N5796AUC

6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - AR, MI, SM
Navy - AS, MC, OS
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2024-018)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.