The documentation and process conversion measures necessary to comply with this revision shall be completed by 27 July 2022.

INCH-POUND

MIL-PRF-19500/430D
w/AMENDMENT 1
27 April 2022
SUPERSEDING
MIL-PRF-19500/430D
15 April 2017

PERFORMANCE SPECIFICATION SHEET

TRANSISTORs, DUAL FIELD EFFECT, N-CHANNEL, SILICON TYPES 2N5545, 2N5546, AND 2N5547, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for two electrically isolated, matched N-channel, junction, silicon field-effect transistors in one package. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each device.

1.2 Package outlines. The device package outlines are as follows: TO-71 in accordance with figure 1 for all encapsulated device types.

* 1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

P_T T_A = +25°C (1)	P_T T_A = +25°C (1)	V_{DG}	V_{GS}	I_G	T_{STG}
One section	Both sections				
mW	mW	V dc	V dc	mA dc	°C
250	400	50	-50	30	-65 to +200

(1) For T_A > +25°C, derate linearly 1.67 mW/°C one section, 2.67 mW/°C both sections.

1.4 Primary electrical characteristics. T_C = +25°C, unless otherwise specified.

*

Limits	I_{DSS} V_{GS} = 0 V_{DS} = 15 V dc	$V_{GS(off)}$ V_{DS} = 15 V dc I_D = 0.5 nA dc	$\lvert y_{fs}\rvert$ V_{DS} = 15 V dc V_{GS} = 0 f = 1 kHz	$\lvert y_{fs}\rvert$ V_{DS} = 15 V dc V_{GS} = 0 f = 100 MHz	NF V_{DG} = 15 V dc I_D = 200 µA dc R_G = 1 MΩ f = 10 Hz		C_{iss} V_{DS} = 15 V dc V_{GS} = 0 f = 1 MHz	C_{rss} V_{DS} = 15 V dc V_{GS} = 0 f = 1 MHz
	mA dc	V dc	mmho	mmho	2N5545 dB	2N5546 dB	pF	pF
Min	0.5	-0.5	1.5	1.5				
Max	8.0	-4.5	6.0		3.5	5.0	6.0	2.0

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

AMSC N/A

FSC 5961

* DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1.4 Primary electrical characteristics - Continued.

	I_{DSS1} / I_{DSS2} V_{DG} = 15 V dc V_{GS} = 0			$\lvert y_{fs}\rvert_1$ / $\lvert y_{fs}\rvert_2$ V_{DG} = 15 V dc I_D = 200 µA dc f = 1 kHz			$\lvert V_{GS1} - V_{GS2}\rvert_2$ V_{DG} = 15 V dc I_D = 200 µA dc			$\lvert\Delta(V_{GS1} - V_{GS2})\Delta T_A\rvert$ (1) V_{DG} = 15 V dc I_D = 200 µA dc $T_{A(1)}$ = +25°C $T_{A(2)}$ = -55°C			$\lvert\Delta(V_{GS1} - V_{GS2})\Delta T_A\rvert$ (1) V_{DG} = 15 V dc I_D = 200 µA dc $T_{A(1)}$ = +25°C $T_{A(2)}$ = +125°C		
2N#	5545	5546	5547	5545	5546	5547	5545	5546	5547	5545	5546	5547	5545	5546	5547
							mV dc	mV dc	mV dc	mV dc	mV dc	mV dc	mV dc	mV dc	mV dc
Min	0.95	0.9	0.9	0.97	0.95	0.9									
Max	1.05	1.10	1.10	1.03	1.05	1.10	5	10	15	0.8	1.6	3.2	1	2	4

(1) Pulsed, (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

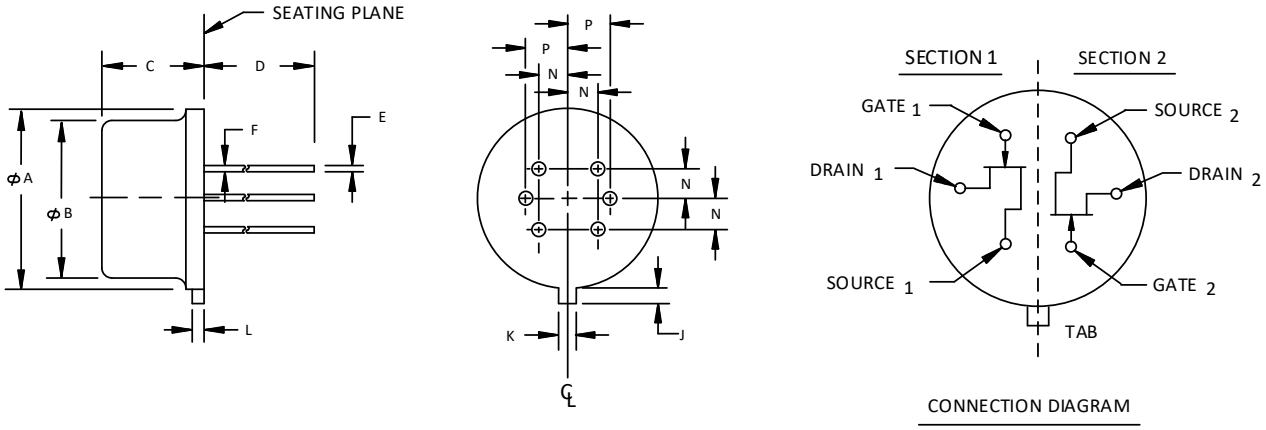
1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JAN”, “JANTX” and "JANTXV".

1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "5545", "5546", and "5547".

1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.



Ltr	Inches	Inches	mm	mm	Notes
	Min	Max	Min	Max	
ϕA	.209	.230	5.31	5.84	
ϕB	.178	.195	4.52	4.95	
C	.170	.210	4.32	5.33	
D	.500	.750	12.70	19.05	
E		.021		0.53	3
F	.016	.019	0.41	0.48	4
J	.028	.048	0.71	1.22	7
K	.036	.046	0.91	1.17	
L		.020		0.51	
* N	.0146 Nom.		.371 Nom.		5
P	.0354 Nom.		.900 Nom.		5

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Measured in the zone beyond .250 inch (6.35 mm) from the seating plane.
* 4. Measured in the zone from .50 inch (12.7 mm) to .250 inch (6.35 mm) from the seating plane.
* 5. When measured in a gauging plane .054 +.001, -.000 inch (1.37 +0.03, -0.00 mm) below the seating plane of the transistor, maximum diameter leads shall be within .007 inch (0.18 mm) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance.
6. All leads electrically insulated from case and each section electrically isolated from the other.
7. Measured from the maximum diameter of the actual device.
* 8. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions (similar to TO-71).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

$\frac{|I_{DSS1}|}{|I_{DSS2}|}$ ..... Zero-gate-voltage drain current ratio.

$|I_{G1} - I_{G2}|$ ..... Gate current differential.

$|V_{GS1} - V_{GS2}|$ ..... Gate-source voltage differential.

$|\Delta(V_{GS1} - V_{GS2})\Delta T_A|$ ..... Gate-source voltage differential change with temperature.

V_n ..... Equivalent short circuit input noise voltage for unity bandwidth.

$\frac{|y_{fs}|1}{|y_{fs}|2}$ ..... Small-signal common-source forward transfer admittance ratio.

$||y_{os}|1 - |y_{os}|2|$ ..... Small-signal common-source output admittance differential.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

* 3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices shall be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent, if practical.

g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100$ kΩ, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and table I.

3.8 Electrical test requirements. The electrical test requirements shall be specified in table I herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500), and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurements for JANTX and JANTXV levels
9	Not applicable.
10	Not applicable.
11	I_{DSS}, I_{GSS}, $\|y_{fs}\|$
12	See 4.3.1.
13	Subgroup 2 of table I herein; ΔI_{GSS} = 0.1 nA dc or 100 percent of initial value, whichever is greater. $\|\Delta y_{fs}\|$ = ±20 percent of initial value. ΔI_{DSS} = 10 percent of initial value.

4.3.1 Power burn-in. Power burn-in conditions are in accordance with MIL-STD-750, method 1039, condition A and as follows: T_A = +175°C; V_{GS} = -40 V dc; V_{DS} = 0.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. Alternate flow is allowed for quality conformance inspection in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table II herein.

Subgroup	Method	Condition
B3	1027	V_{GS} = -40 V dc; T_A = +175°C; V_{DS} = 0.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table II herein.

Subgroup	Method	Condition
C2	2036	Lead fatigue: Test condition E.
C6	1027	V_{GS} = -40 V dc; T_A = +175°C; V_{DS} = 0.

4.4.4 Gate current differential. The gate current of each individual section of a dual unit shall be measured at the specified conditions and the absolute value of the difference of the two currents shall be calculated. If possible, this difference shall be measured directly to improve accuracy.

4.4.5 Gate-source voltage differential. The gate-source voltage of each individual section of a dual unit shall be measured at the specified conditions and the absolute value of the difference of the two voltages shall be calculated. If possible, this difference shall be measured directly to improve accuracy.

4.4.6 Gate-source voltage differential change with temperature. The gate-source voltage differential shall be measured at the two specified temperatures in accordance with 4.4.5 herein except that the polarities of the differentials and identities of the individual sections shall be maintained. The absolute value of the algebraic differences between the values at the two temperatures shall be calculated. If possible, this difference should be measured directly to improve accuracy. A mathematical formula for the parameter is:

$$|(V_{GS1} - V_{GS2})T_1 - (V_{GS1} - V_{GS2})T_2|$$

4.4.7 Zero-gate-voltage drain current ratio. The value for the zero-gate-voltage drain current for each individual section of a dual unit shall be measured using method 3413 of MIL-STD-750. The zero-gate-voltage drain current ratio shall be calculated by dividing one of the values by the other. If possible, this ratio shall be measured directly to improve accuracy.

4.4.8 Small-signal common-source forward transfer admittance ratio. The magnitude for the small-signal common-source forward transfer admittance ratio for each individual section of a dual unit shall be measured using method 3455 of MIL-STD-750. The small-signal common-source forward transfer admittance ratio shall be calculated by dividing one of the values by the other. If possible, this ratio shall be measured directly to improve accuracy.

4.4.9 Small-signal common-source output admittance differential. The magnitude for the small-signal common-source output admittance differential for each individual section of a dual unit shall be measured using method 3453 of MIL-STD-750. The small-signal common-source output admittance differential shall be calculated by dividing one of the values by the other. If possible, this ratio shall be measured directly to improve accuracy.

4.4.10 Spot noise figure and equivalent input noise voltage. These tests should be conducted with a model 2173C Quan Tech Laboratories test set or equivalent. Conditions shall be as specified in table I.

4.4.11 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical 3/ examination	2071					
Subgroup 2						
Reverse gate current	3411	Bias condition C; V_{GS} = -50 V dc; V_{DS} = 0	I_{GSS1}		-1.0	µA dc
Reverse gate current	3411	Bias condition C; V_{GS} = -30 V dc; V_{DS} = 0	I_{GSS2}		-0.1	nA dc
Drain current	3413	Bias condition C; V_{DS} = 15 V dc; V_{GS} = 0	I_{DSS}	0.5	8.0	mA dc
Gate current		V_{DG} = 15 V dc; I_D = 200 µA dc	I_G		-50	pA dc
Gate-source cutoff voltage	3403	V_{DS} = 15 V dc; I_D = 0.5 nA dc	$V_{GS(off)}$	-0.5	-4.5	V dc
Gate-source voltage differential	3403	V_{DG} = 15 V dc; I_D = 50 µA dc; (see 4.4.5)	$\lvert V_{GS1} - V_{GS2}\rvert 1$			
2N5545					5	mV dc
2N5546					10	mV dc
2N5547					15	mV dc
Gate-source voltage differential	3403	V_{DG} = 15 V dc; I_D = 200 µA dc; (see 4.4.5)	$\lvert V_{GS1} - V_{GS2}\rvert 2$			
2N5545					5	mV dc
2N5546					10	mV dc
2N5547					15	mV dc
Gate-source voltage differential change with temperature	3403	V_{DG} = 15 V dc; I_D = 200 µA dc; $T_{A(1)}$ = +25°C; $T_{A(2)}$ = -55°C; (see 4.4.6)	$\lvert\Delta(V_{GS1} - V_{GS2})\Delta T_A\rvert$			
2N5545					.8	mV dc
2N5546					1.6	mV dc
2N5547					3.2	mV dc
Gate-source voltage differential change with temperature	3403	V_{DG} = 15 V dc; I_D = 200 µA dc; $T_{A(1)}$ = +25°C; $T_{A(2)}$ = +125°C; (see 4.4.6)	$\lvert\Delta(V_{GS1} - V_{GS2})\Delta T_A\rvert$			
2N5545					1	mV dc
2N5546					2	mV dc
2N5547					4	mV dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
Subgroup 2 -continued						
Zero-gate-voltage drain current ratio	3413	Bias condition C; V_{DS} = 15 V dc; V_{GS} = 0; (see 4.4.7)	I_{DSS1} / I_{DSS2}			
2N5545				0.95	1.05	
2N5546				0.90	1.10	
2N5547				0.90	1.10	
Small-signal common-source short-circuit forward transfer admittance ratio	3455	V_{DG} = 15 V dc; I_D = 200 µA dc; f = 1 kHz; (see 4.4.8)	$\lvert y_{fs}\rvert_1$ / $\lvert y_{fs}\rvert_2$			
2N5545				0.97	1.03	
2N5546				0.95	1.05	
2N5547				0.90	1.10	
Small -signal common-source short-circuit, output admittance differential	3453	V_{DS} = 15 V dc; V_{GS} = 0; f = 1 kHz	$\lvert\lvert y_{os}\rvert_1 - \lvert y_{os}\rvert_2\rvert$			
2N5545					1	µmho
2N5546					2	µmho
2N5547					3	µmho
Subgroup 3						
High temperature operation:		T_A = +150°C				
Reverse gate current	3411	Bias condition C; V_{GS} = -30 V dc; V_{DS} = 0	I_{GSS3}		-150	nA dc
Gate current differential		V_{DG} = 15 V dc; I_D = 200 µA dc; T_A = +125°C; (see 4.4.4)	$\lvert I_{G1} - I_{G2}\rvert$		5	nA dc
Small-signal common-source short-circuit forward transfer admittance	3455	V_{DS} = 15 V dc; V_{GS} = 0; 100 kHz ≤ f ≤ 1 MHz	$\lvert y_{fs}\rvert$	1.5	6.0	mmho
Small signal common-source short-circuit, output admittance	3453	V_{DS} = 15 V dc; V_{GS} = 0; 100 kHz ≤ f ≤ 1 MHz	$\lvert y_{os}\rvert$		25	µmho

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit	Limit	Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Small signal common-source short-circuit, input capacitance	3431	V_{GS} = 0 V dc; V_{DS} = 15; 100 kHz ≤ f ≤ 1 MHz	C_{iss}		6	pF
Small signal common-source short-circuit, reverse transfer capacitance	3433	V_{GS} = 0 V dc; V_{DS} = 15; 100 kHz ≤ f ≤ 1 MHz	C_{rss}		2	pF
Spot noise figure (2N5545, 2N5546 only)		V_{DS} = 15 V dc; I_D = 200 μA dc; f = 10 Hz; R_G = 1 MΩ; Noise bandwidth = 5 Hz (see 4.4.10)	NF			
2N5545					3.5	dB
2N5546					5.0	dB
Equivalent input noise voltage		V_{DS} = 15 V dc; I_D = 200 μA dc; Noise bandwidth = 5 Hz (see 4.4.10)	V_n			
2N5545					180	$nV\sqrt{Hz}$
2N5546					200	$nV\sqrt{Hz}$
Subgroups 5 and 6						
Not applicable						
Subgroup 7						
Low temperature operation:		T_A = -65°C				
Magnitude of small-signal common-source short-circuit forward transfer admittance	3455	V_{DS} = 15 V dc; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$		10.0	mmho

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed subgroup A1, double the sample size of the failed test or sequence of tests.
3/ Separate samples may be used.

TABLE II. Groups A, B, and C electrical end-point measurements. 1/ 2/

Step	Inspection	MIL-STD-750		Symbol	Limit	Limit	Unit
		Method	Conditions		Min	Max	
1.	Reverse gate current	3411	Bias condition C: V_{GS} = -30 V dc; V_{DS} = 0	I_{GSS4}		-0.5	nA dc
2.	Magnitude of small-signal common-source short-circuit forward transfer admittance	3455	V_{DS} = 15 V dc V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$	1.5	6.0	mmho
3.	Reverse gate current	3411	Bias condition C; V_{GS} = -30 V dc; V_{DS} = 0	I_{GSS5}		-1.0	nA dc
4.	Small-signal common-source short-circuit forward transfer admittance	3455	V_{DS} = 15 V dc; V_{GS} = 0; f = 1 kHz	$\Delta\|y_{fs}\|$	±20		percent change from initial group A reading
5.	Gate-source voltage differential	3403	V_{DG} = 15 V dc; I_D = 200 μA dc	$|V_{GS1} - V_{GS2}|$3			
	2N5545					6	mV dc
	2N5546					12	mV dc
	2N5547					18	mV dc
6.	Zero-gate-voltage drain current ratio	3413	Bias condition C; V_{DG} = 15 V dc; V_{GS} = 0	$\frac{I_{DSS1}}{I_{DSS2}}$			
	2N5545				0.95	1.05	
	2N5546				0.90	1.10	
	2N5547				0.90	1.10	

1/ The electrical measurements for table E-VIB (JAN, JANTX, JANTXV) of MIL-PRF-19500 are as follows:
a. Subgroup 2, see table II herein, steps 1 and 2.
b. Subgroups 3 and 6, see table II herein, steps 3, 4, 5, and 6.

2/ The electrical measurements for table E-V of MIL-PRF-19500 are as follows: Subgroups 2, 3, and 6, see table II herein, steps 3, 4, 5, and 6.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	-55°C to +150°C, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable	
Electrical measurements		See table I, subgroup 2 and table II, all steps	
Subgroup 2			45 devices c = 0
Blocking life	1048	1,000 hours minimum, T_A = +150°C, V_{DG} or V_{GS} = 80 percent of rated.	
Electrical measurements		See table I, subgroup 2 and table II, all steps	
Subgroups 4 and 5			
Not applicable			

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

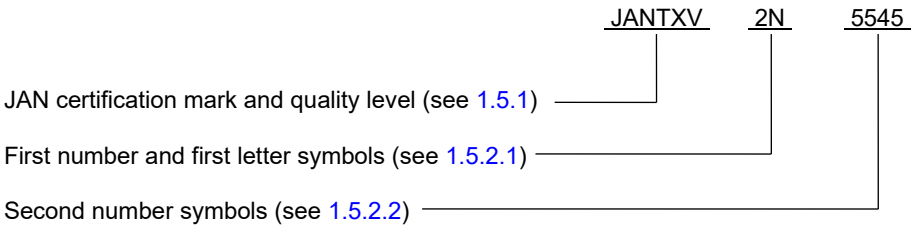
c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QPDSIS-19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil/.

6.4 PIN construction example.

6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs.

6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN2N5545	JANTX2N5545	JANTXV2N5545
JAN2N5546	JANTX2N5546	JANTXV2N5546
JAN2N5547	JANTX2N5547	JANTXV2N5547

6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-6939 or DSN 850-6939.

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
DLA - CC

Review activities:
Army - MI
* Air Force - 19
* NASA - NA

Preparing activity:
DLA - CC

(Project 5961-2022-030)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.