

# MSKSEMI 美森科

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



PLED

## **AO4614-MS**

**Product specification**

## Description

The AO4614-MS uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

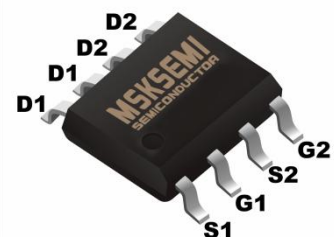
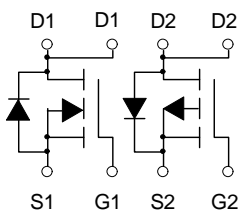

## General Features

- $V_{DS} = 40V$   $I_D = 7.2A$
- $R_{DS(ON)} < 26m\Omega$  @  $V_{GS} = 10V$
- $V_{DS} = -40V$   $I_D = 6.5A$
- $R_{DS(ON)} < 54m\Omega$  @  $V_{GS} = 10V$

## Applications

- Battery protection
- Load switch
- Uninterruptible power supply

## Reference News

PACKAGE OUTLINE	N-Channel and P-Channel	Marking
 <p>SOP-8</p>		

## Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
$V_{DS}$	Drain-Source Voltage	40	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	7.2	-6.5	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	5.6	-5.1	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	23	-22	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	16.2	39	mJ
$I_{AS}$	Avalanche Current	18	-28	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>4</sup>	1.67	1.67	W
$T_{STG}$	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	75		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	30		$^\circ C/W$

**N-Channel Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA	---	0.034	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =5A	---	20	26	m Ω
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =4A	---	28	33	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	---	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-4.56	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =5A	---	14	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz	---	2.6	---	
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =5A	---	5.5	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1.25	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2.5	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V , V <sub>GS</sub> =10V , R <sub>G</sub> =3.3 I <sub>D</sub> =1A	---	8.9	---	ns
T <sub>r</sub>	Rise Time		---	2.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	41	---	
T <sub>f</sub>	Fall Time		---	2.7	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz	---	593	---	pF
C <sub>oss</sub>	Output Capacitance		---	76	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	56	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	6.1	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	23	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C	---	---	1.2	V

**Note :**

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3. The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V,V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=18A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

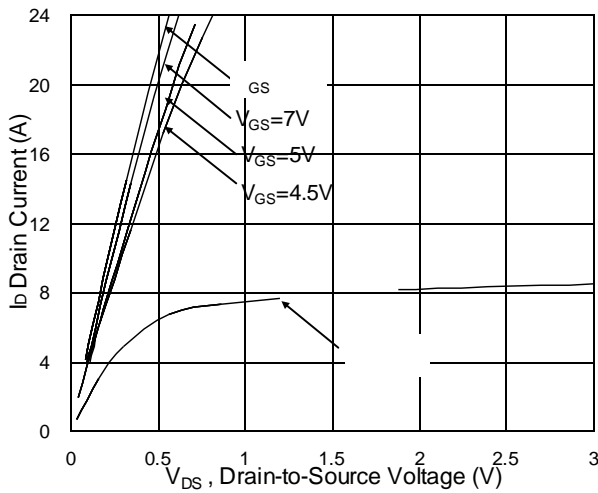
**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-40	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA	---	-0.02	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V , I <sub>D</sub> =-6A	---	45	54	m Ω
		V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-4A	---	80	85	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.0	---	-2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	3.72	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =-32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> = ± 20V , V <sub>DS</sub> =0V	---	---	± 100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-6A	---	13	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-20V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-6A	---	11.5	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	3.5	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	3.3	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V , V <sub>GS</sub> =-10V , R <sub>G</sub> =3.3 , I <sub>D</sub> =-1A	---	22	---	ns
T <sub>r</sub>	Rise Time		---	15.7	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	59	---	
T <sub>f</sub>	Fall Time		---	5.5	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz	---	1415	---	pF
C <sub>oss</sub>	Output Capacitance		---	134	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	102	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	-6	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	-22	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C	---	---	-1.2	V

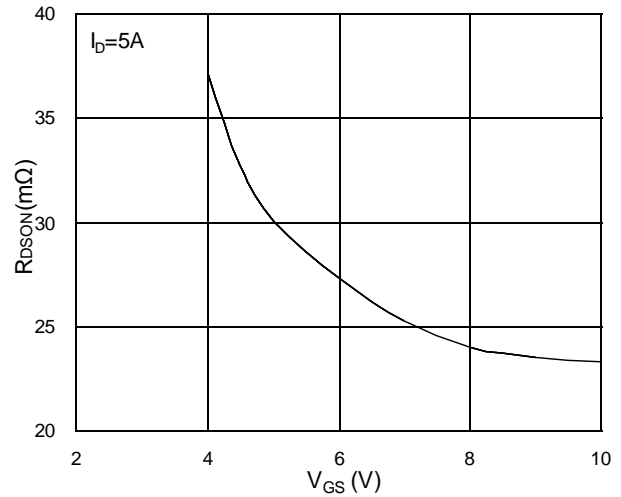
Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3. The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-25V,V<sub>GS</sub>=-10V,L=0.1mH,I<sub>AS</sub>=-28A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation

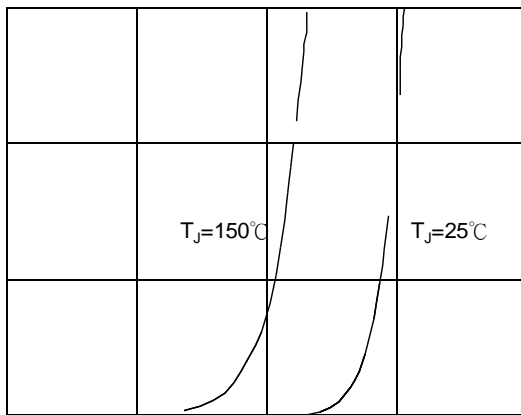
## N-Channel Typical Characteristics



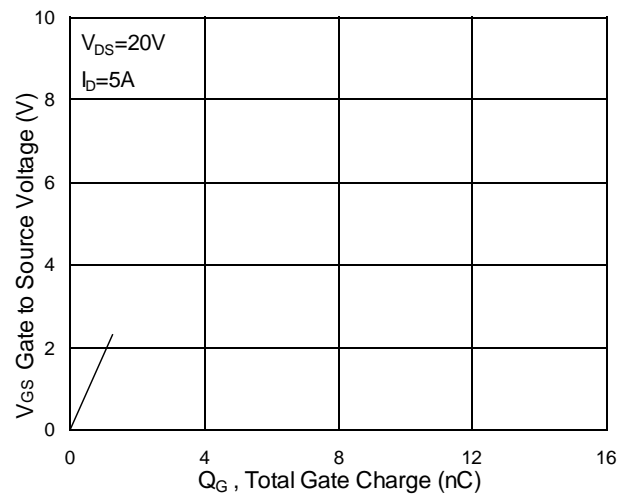
**Fig.1 Typical Output Characteristics**



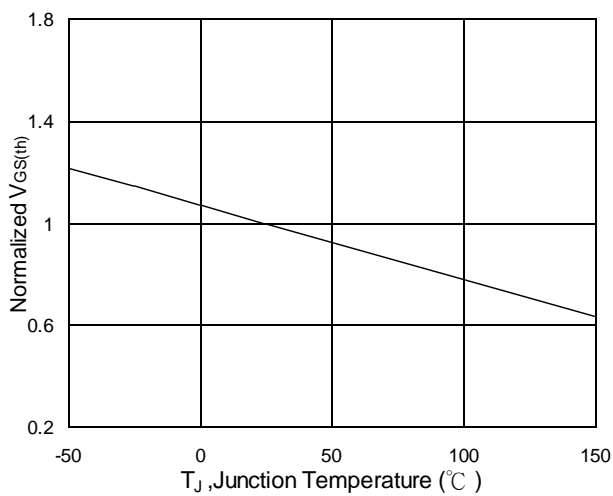
**Fig.2 On-Resistance vs. G-S Voltage**



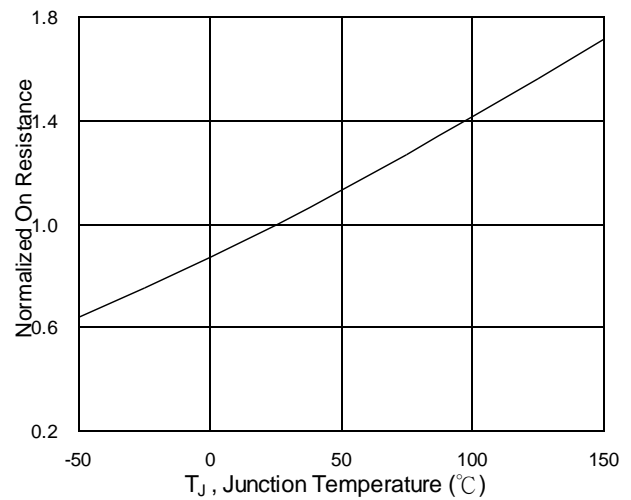
**Fig.3 Forward Characteristics of Reverse**



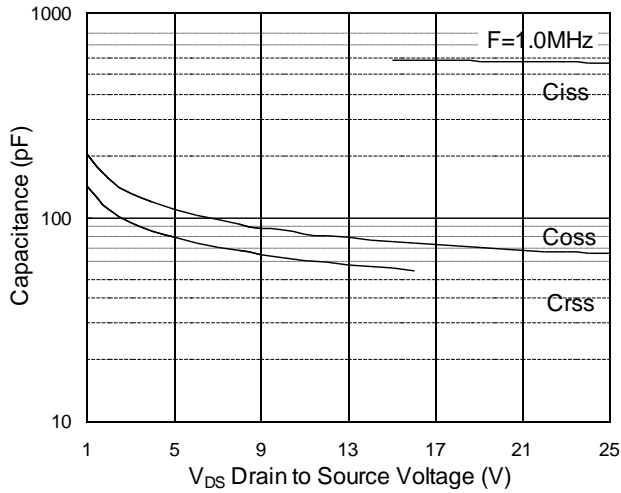
**Fig.4 Gate-Charge Characteristics**



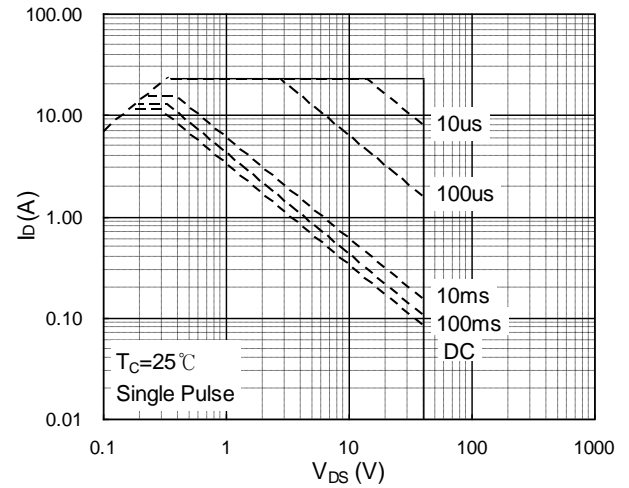
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



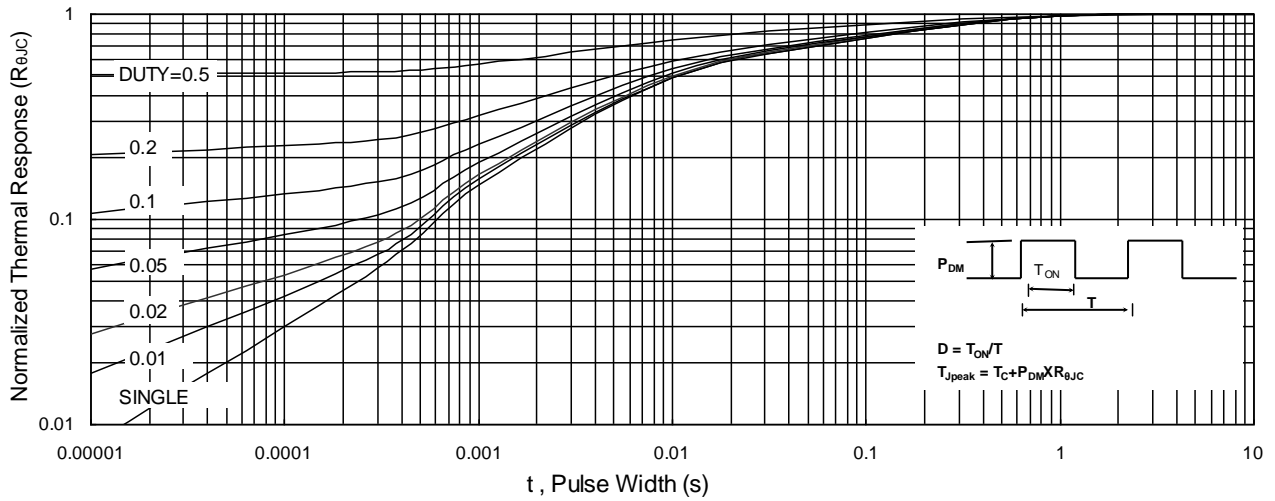
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



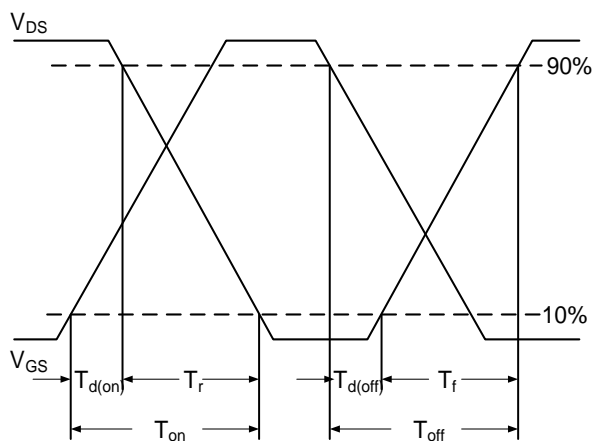
**Fig.7 Capacitance**



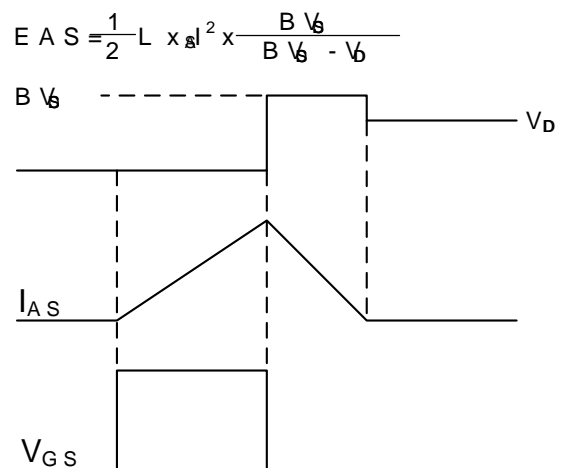
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

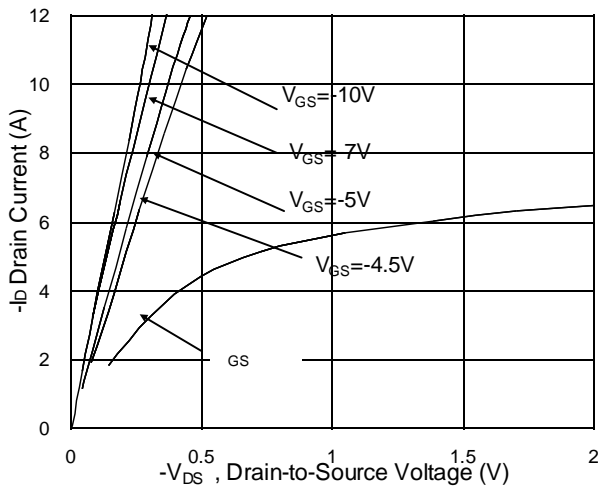


**Fig.10 Switching Time Waveform**

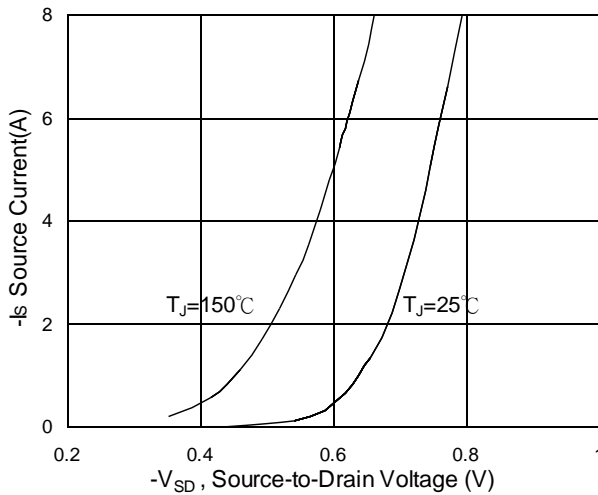


**Fig.11 Unclamped Inductive Switching Wave**

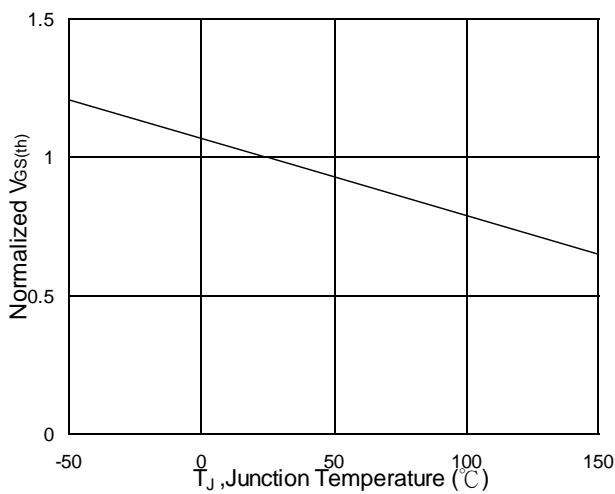
## P-Channel Typical Characteristics



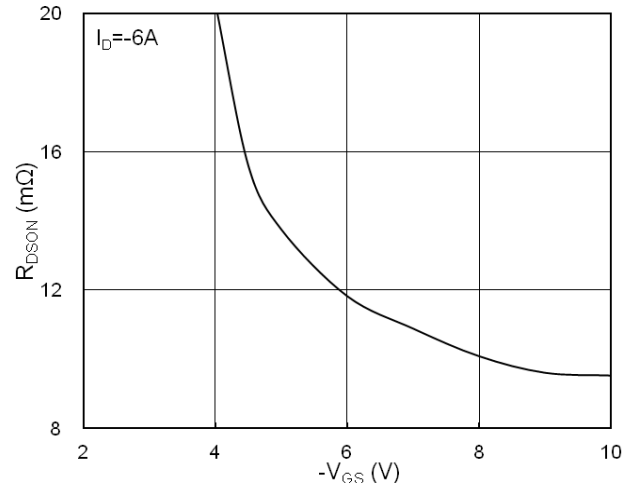
**Fig.1 Typical Output Characteristics**



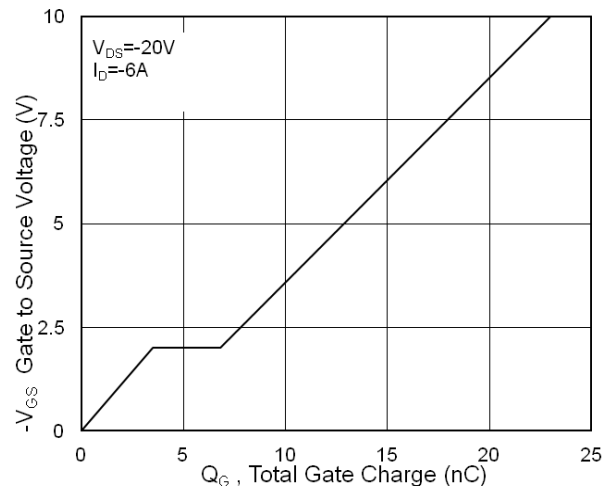
**Fig.3 Forward Characteristics of Reverse**



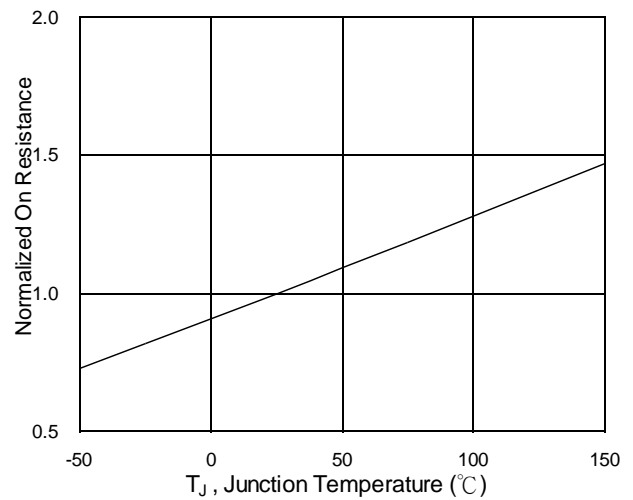
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



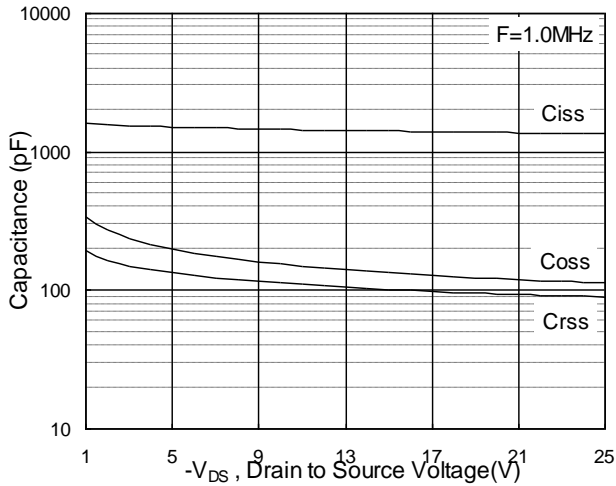
**Fig.2 On-Resistance v.s Gate-Source**



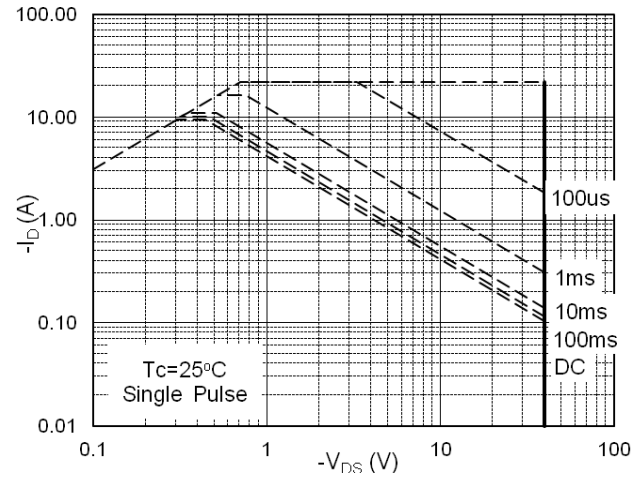
**Fig.4 Gate-Charge Characteristics**



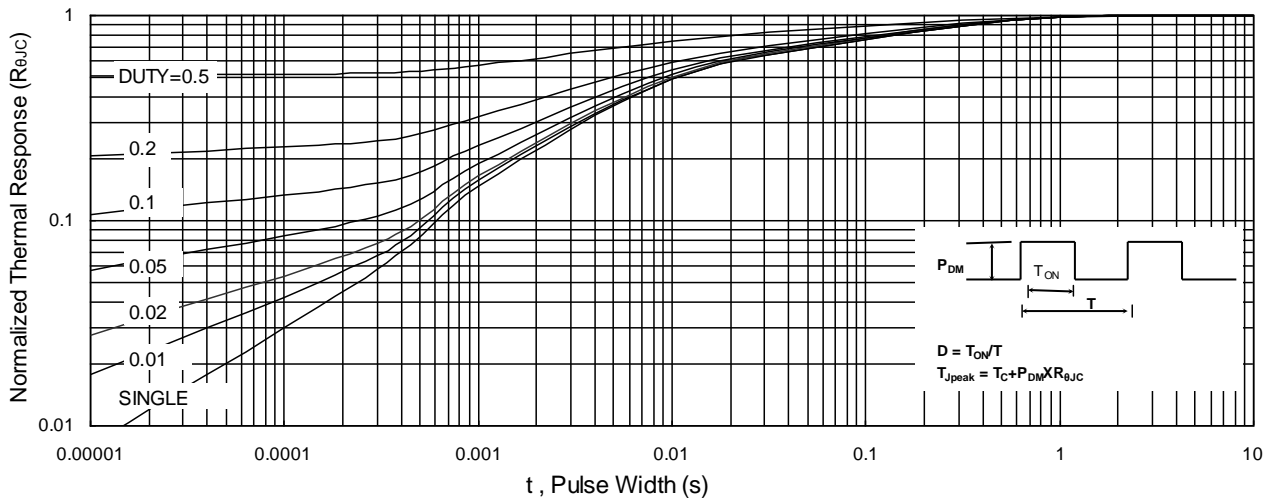
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



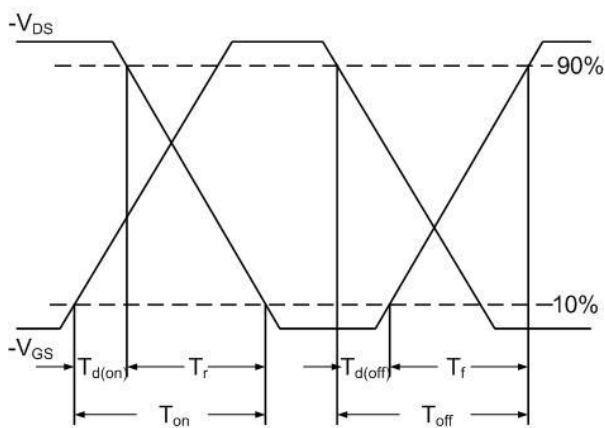
**Fig.7 Capacitance**



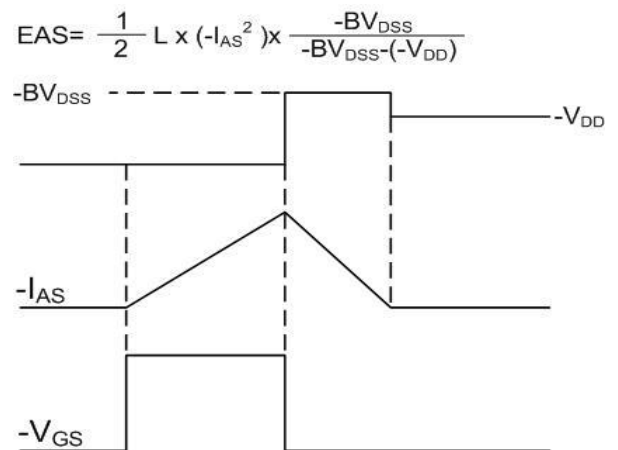
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



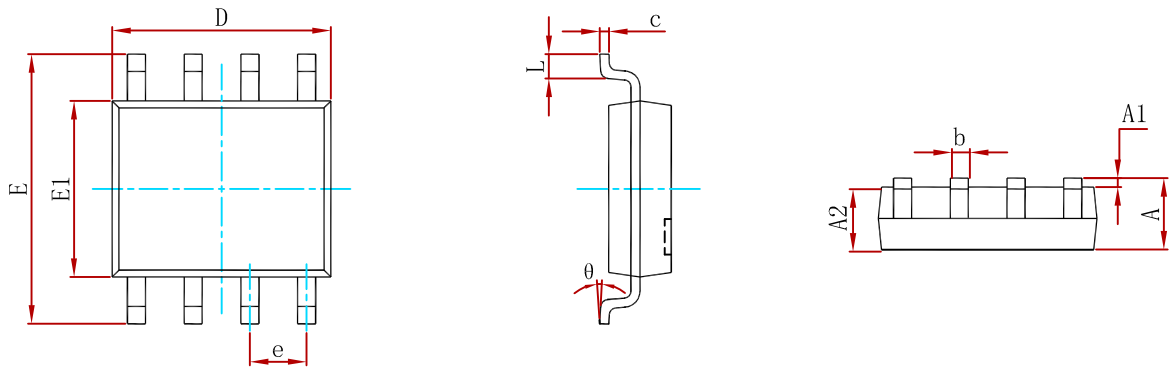
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

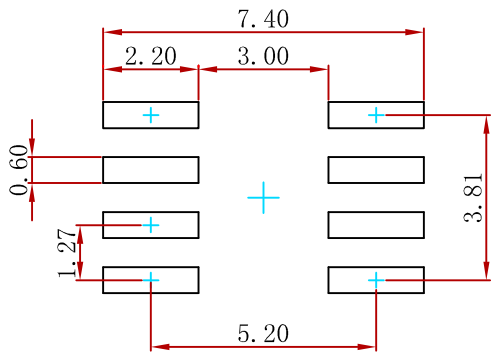


PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:  
1. Controlling dimension: in millimeters.  
2. General tolerance:  $\pm 0.05\text{mm}$ .  
3. The pad layout is for reference purposes only.

REEL SPECIFICATION

P/N	PKG	QTY
AO4614-MS	SOP-8	3000

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