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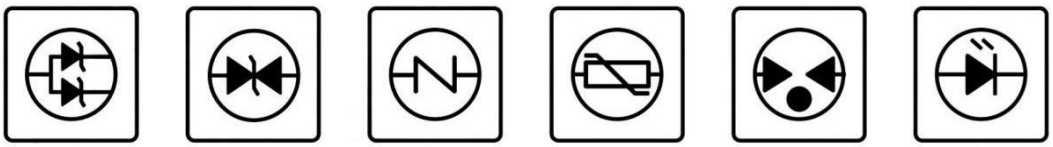
SEMICONDUCTOR



AO4828-MS

Product specification

Description

The AO4828-MS uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

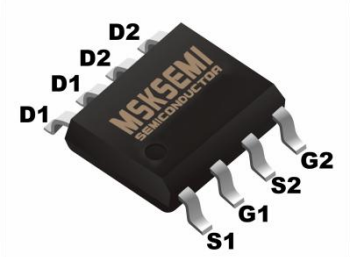
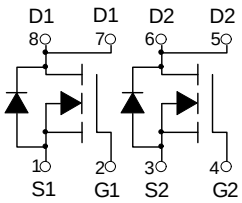
General Features

- V_{DS} =60V,I_D =6.5A
- $R_{DS(ON)}$ < 36mΩ @ V_{GS}=10V
- $R_{DS(ON)}$ < 48mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Low gate to drain charge to reduce switching losses

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Reference News

PACKAGE OUTLINE	Dual N-Channel MOSFET	Marking
 SOP-8		MSKSEMI 4828 MS**NN

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	6.5	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	5	A
Pulsed Drain Current	I_{DM}	30	A
Maximum Power Dissipation	P_D	2.1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient(Note 2)	$R_{\theta JA}$	60	℃/W

Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	69	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	1.4	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A		30	36	mΩ
		V_{GS}=4.5V, I_D=4A		34	48	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=6A		20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		1920		PF
Output Capacitance	C_{oss}			155		PF
Reverse Transfer Capacitance	C_{rss}			116		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=30V, R_L=4.7Ω	-	8	-	nS
Turn-on Rise Time	t_r	V_{GS}=10V,R_{GEN}=3Ω	-	5	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29	-	nS
Turn-Off Fall Time	t_f		-	6	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=6A, V_{GS}=10V	-	50	-	nC
Gate-Source Charge	Q_{gs}		-	8	-	nC
Gate-Drain Charge	Q_{gd}		-	16	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=6A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	7	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, I_F =7A di/dt = 100A/μs(Note3)	-	35	-	nS
Reverse Recovery Charge	Qrr		-	43	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

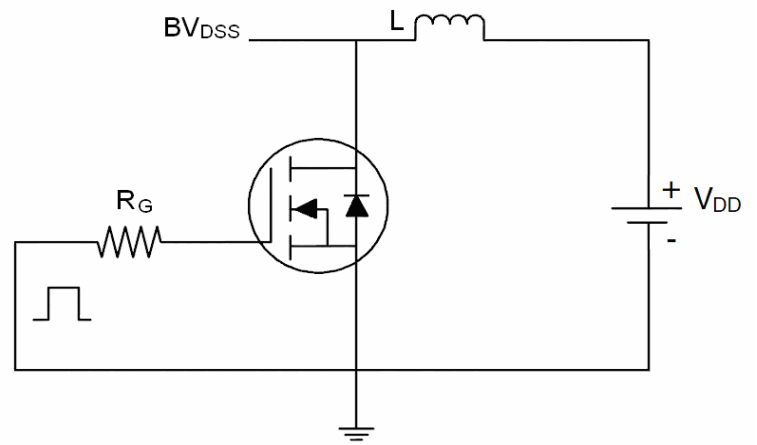
2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

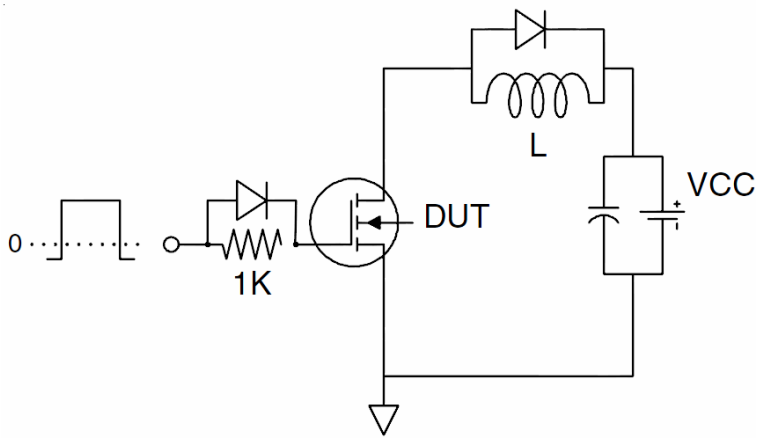
4. Guaranteed by design, not subject to production

Test Circuit

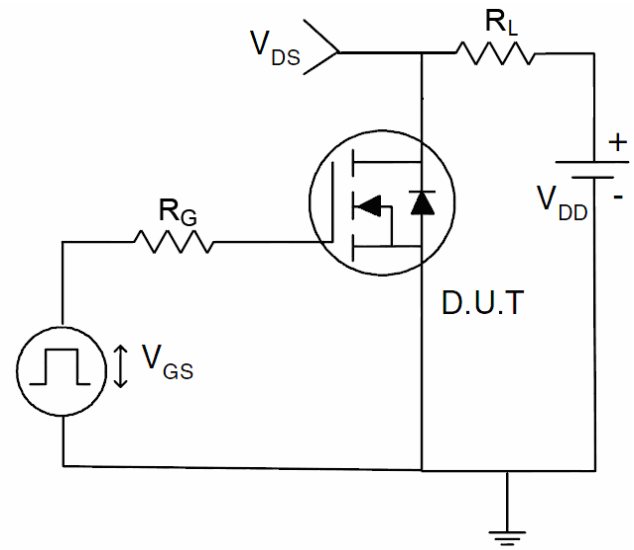
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

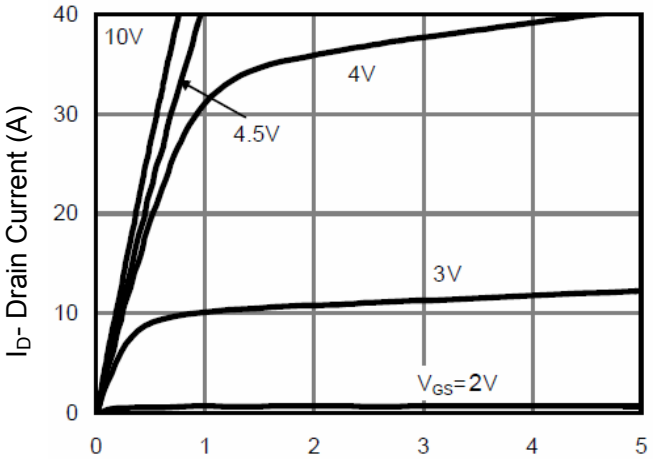


Figure 1 Output Characteristics

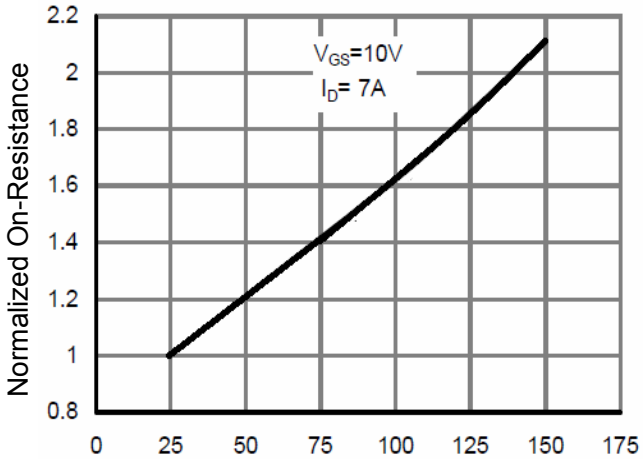


Figure 4 Rdson-JunctionTemperature

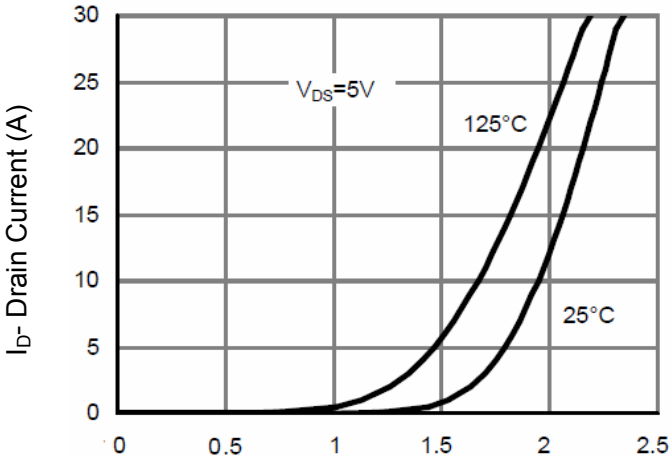


Figure 2 Transfer Characteristics

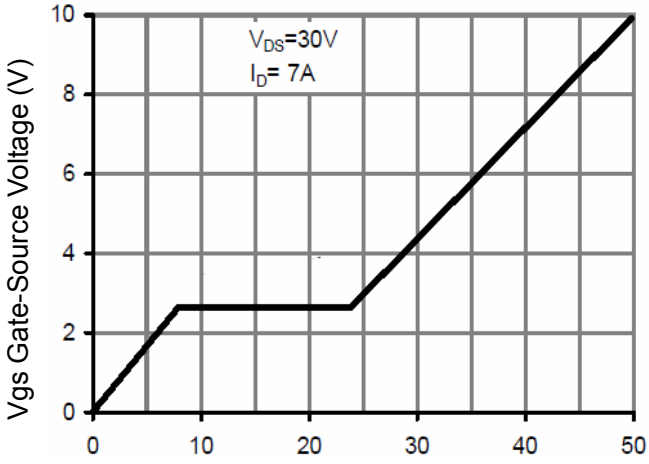


Figure 5 Gate Charge

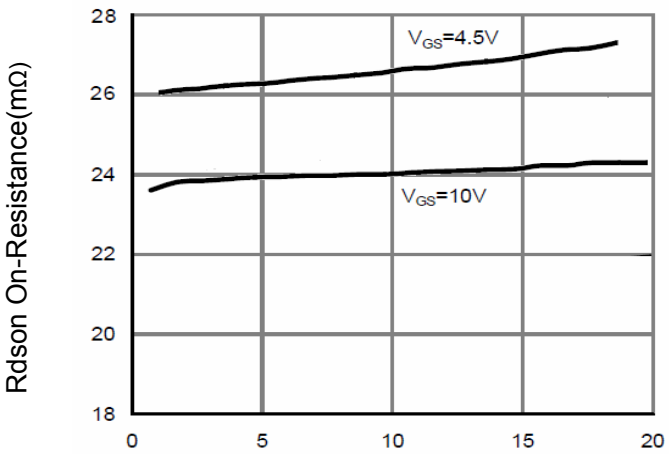


Figure 3 Rdson- Drain Current

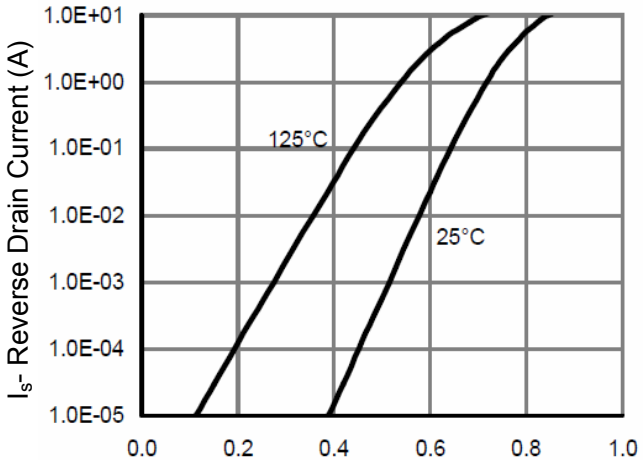


Figure 6 Source- Drain Diode Forward

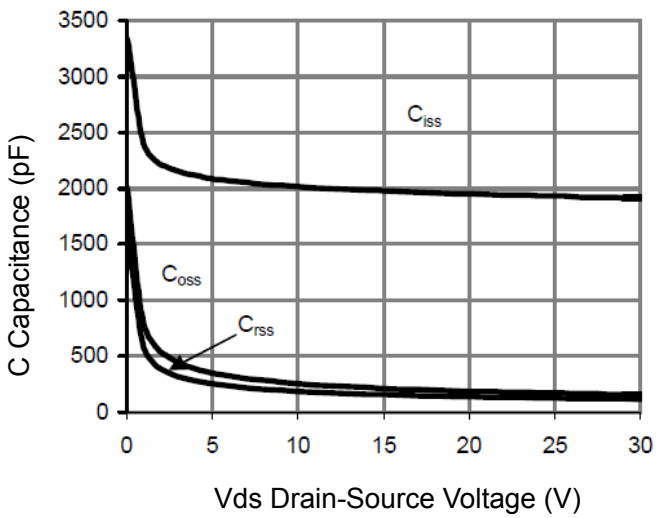


Figure 7 Capacitance vs Vds

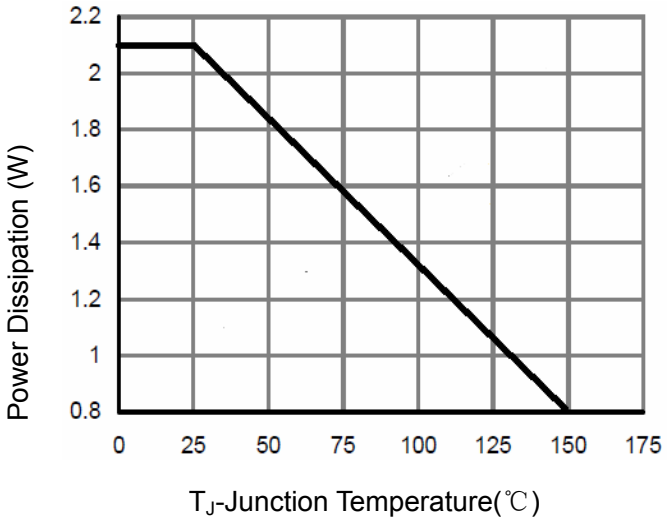


Figure 9 Power De-rating

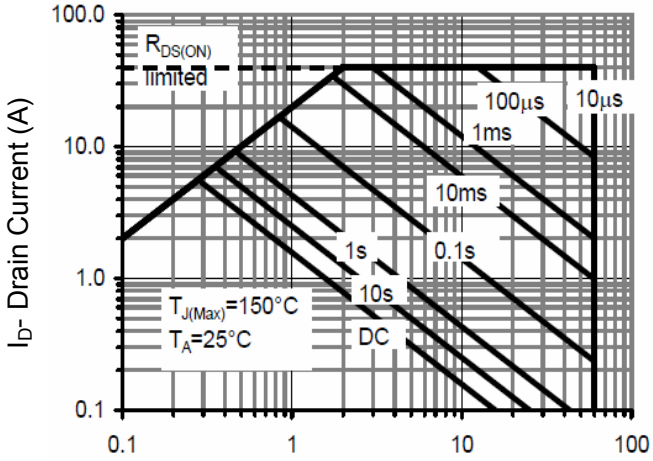


Figure 8 Safe Operation Area

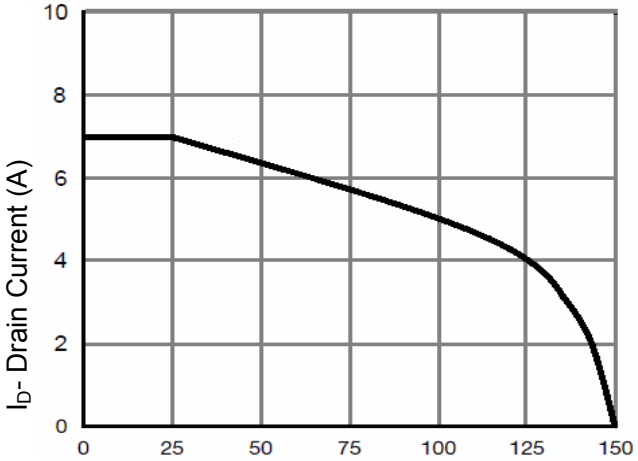


Figure 10 Current De-rating

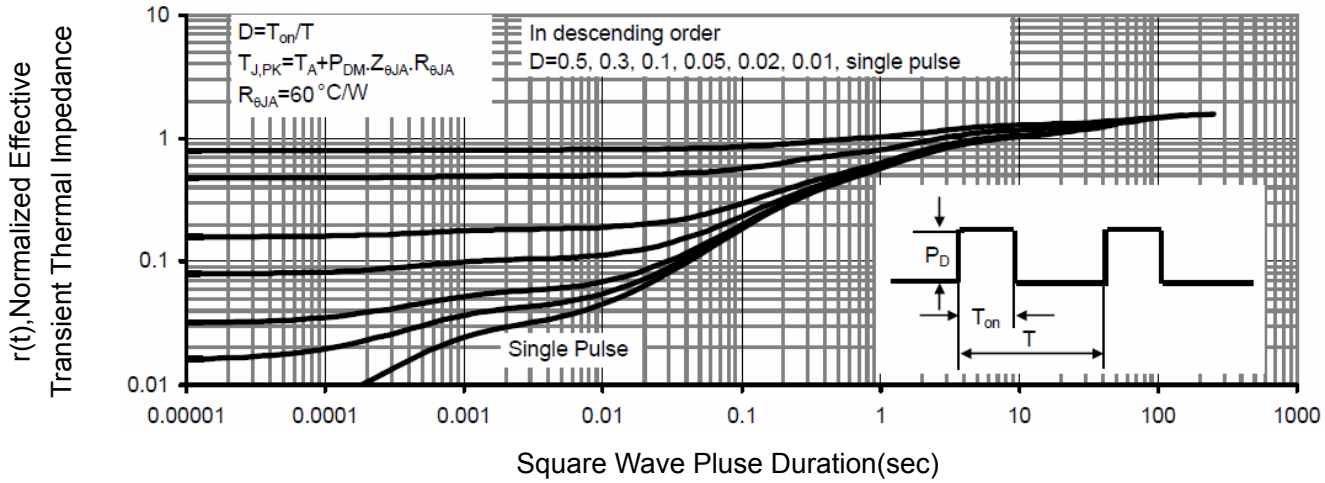
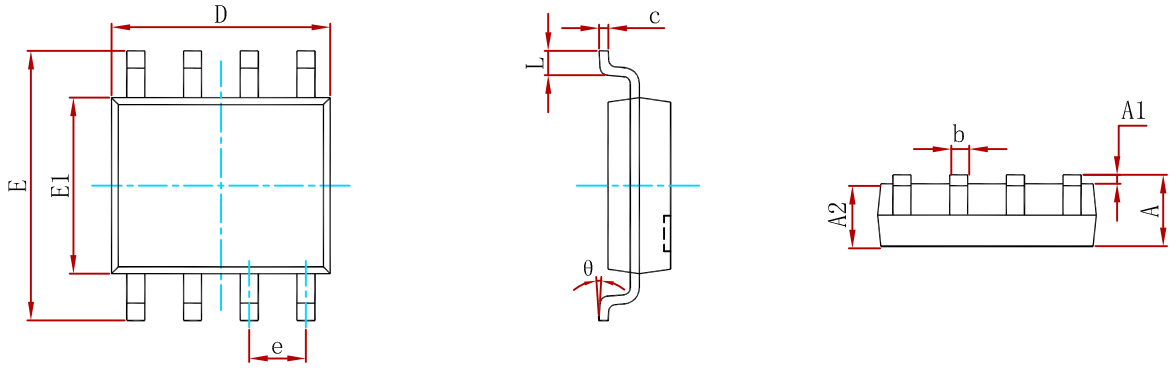


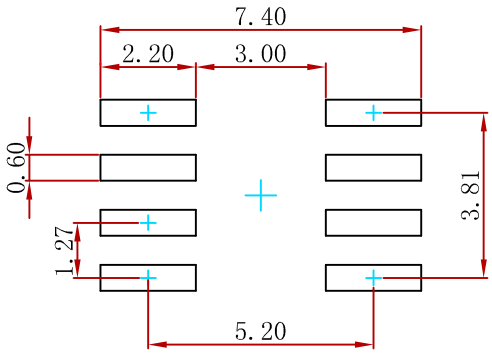
Figure 11 Normalized Maximum Transient Thermal Impedance

PACKAGEMECHANICALDATA



Symbol	DimensionsInMillimeters		DimensionsInInches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

REELSPECIFICATION

P/N	PKG	QTY
AO4828-MS	SOP-8	3000

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