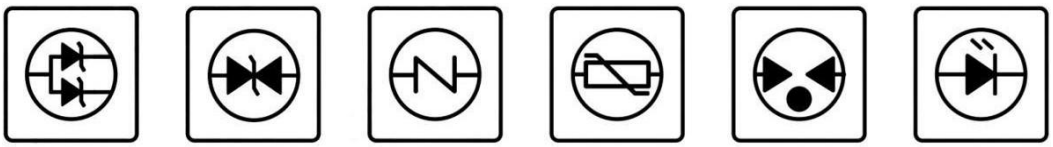
MSKSEMI 美森科
SEMICONDUCTOR



MS15N10

Product specification

General Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

BVDSS	RDSON	ID
100V	75mΩ	15A

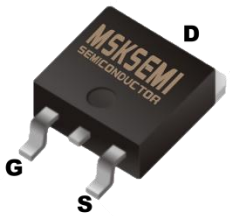
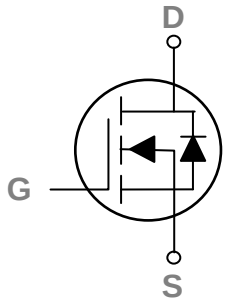
Features

- 100V,15A, RDS(ON) =75mΩ@VGS =10V
- Improved dv/dt capability
- Fast switching
- Green Device Available

Applications

- Networking
- Load Switch
- LED applications

Reference News

PACKAGE OUTLINE	N-Channel MOSFET	Marking
 TO-252		MSKSEMI 80N10 MS**

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current – Continuous (T_C=25℃)	15	A
	Drain Current – Continuous (T_C=100℃)	9.5	A
I_{DM}	Drain Current – Pulsed[1]	60	A
P_D	Power Dissipation (T_C=25℃)	50	W
	Power Dissipation – Derate above 25℃	0.4	W/℃
T_{STG}	Storage Temperature Range	-50 to 150	℃
T_J	Operating Junction Temperature Range	-50 to 150	℃

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction to Case	---	2.5	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	100	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.05	---	V/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=100V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=80V , V_{GS}=0V , T_J=125℃	---	---	10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA

On Characteristics

$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V , I_D=5A	---	75	95	mΩ
		V_{GS}=4.5V , I_D=3A	---	85	110	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.8	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5	---	mV/℃
gfs	Forward Transconductance	V_{DS}=10V , I_D=3A	---	8.7	---	S

Dynamic and switching Characteristics

Q_g	Total Gate Charge[2,3]	V_{DS}=48V , V_{GS}=10V , I_D=5A	---	9.3	---	nC
Q_{gs}	Gate-Source Charge[2,3]		---	2.1	---	
Q_{gd}	Gate-Drain Charge[2,3]		---	1.8	---	
$T_{d(on)}$	Turn-On Delay Time[2,3]	V_{DD}=30V , V_{GS}=10V , R_G=3.3Ω I_D=1A	---	2.9	---	ns
T_r	Rise Time[2,3]		---	9.5	---	
$T_{d(off)}$	Turn-Off Delay Time[2,3]		---	18.4	---	
T_f	Fall Time[2,3]		---	5.3	---	
C_{iss}	Input Capacitance	V_{DS}=50V , V_{GS}=0V , F=1MHz	---	1480	---	pF
C_{oss}	Output Capacitance		---	480	---	
C_{rss}	Reverse Transfer Capacitance		---	35	---	
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, F=1MHz	---	1.3	---	Ω

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	---	---	15	A
I_{SM}	Pulsed Source Current		---	---	30	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

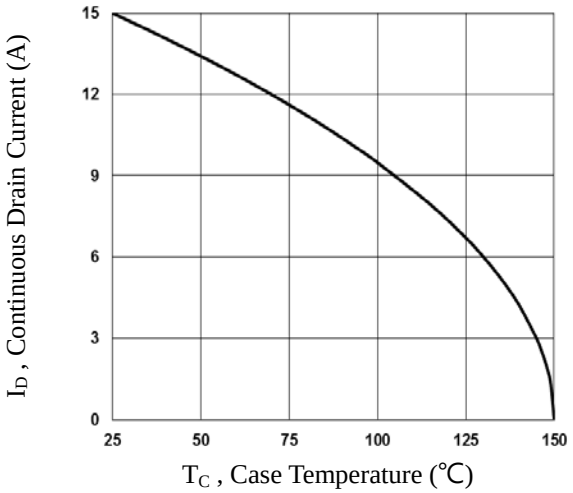


Fig.1 Continuous Drain Current vs. TC

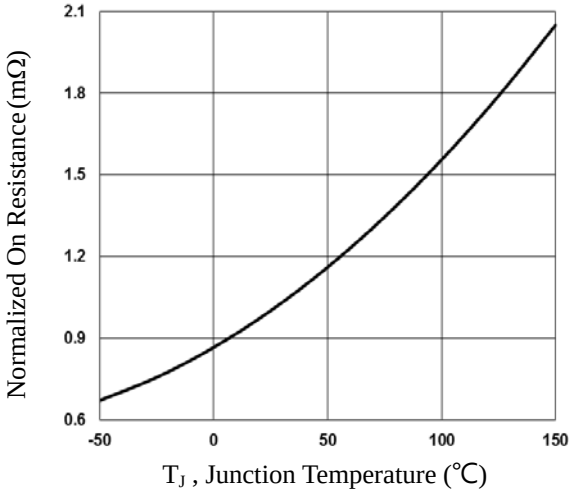


Fig.2 Normalized RDSON vs. TJ

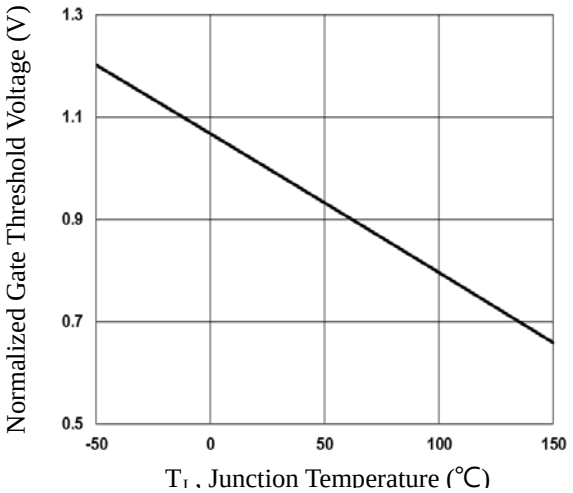


Fig.3 Normalized V_{th} vs. T_J

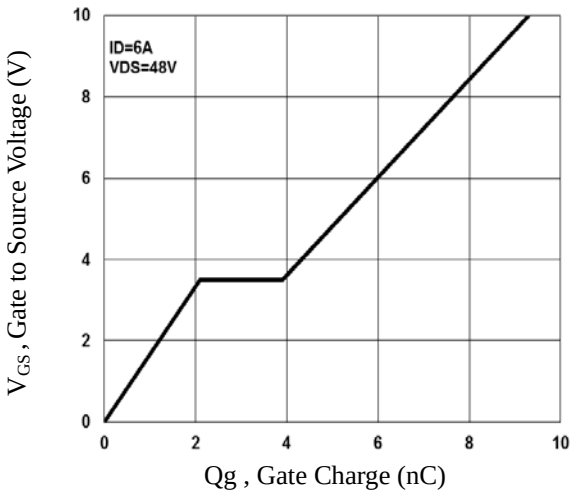


Fig.4 Gate Charge Characteristics

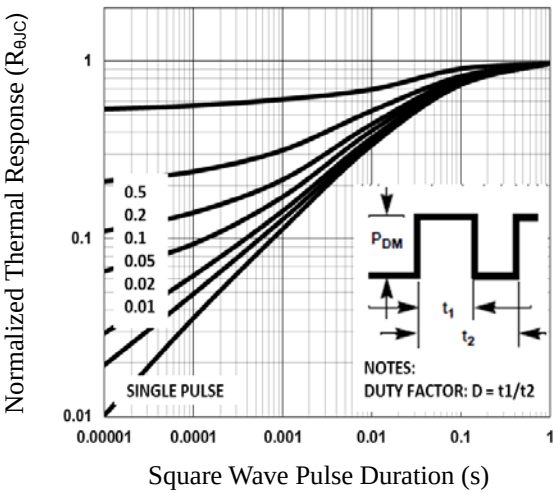


Fig.5 Normalized Transient Impedance

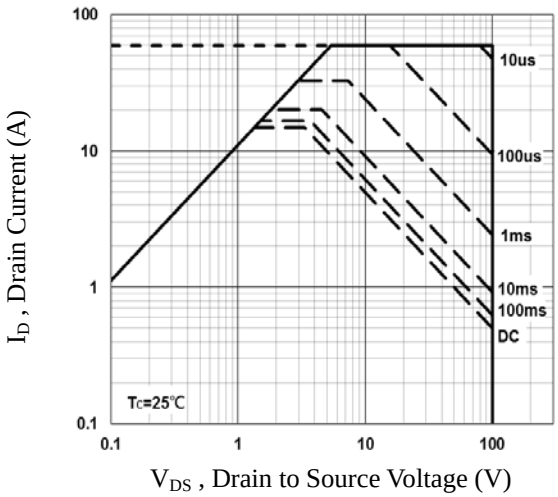


Fig.6 Maximum Safe Operation Area

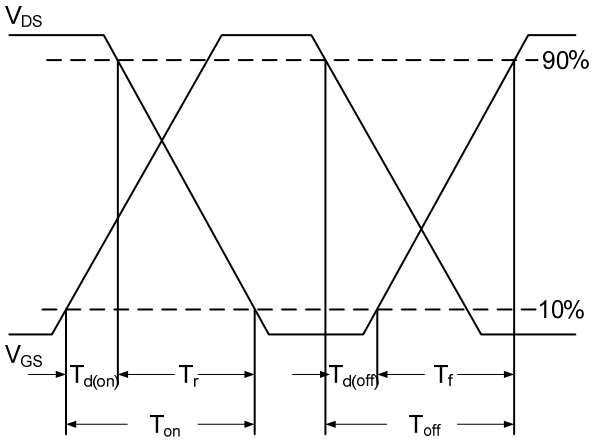


Fig.7 Switching Time Waveform

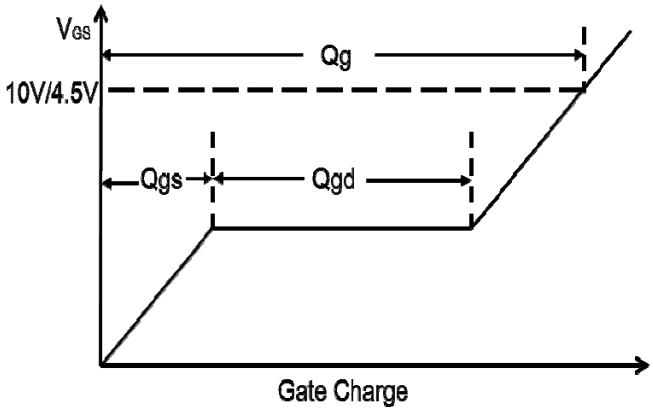
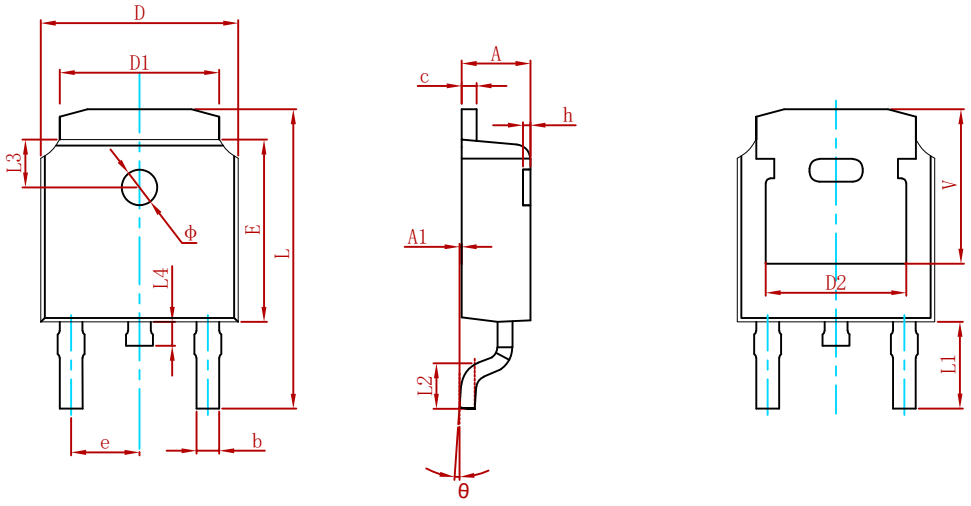


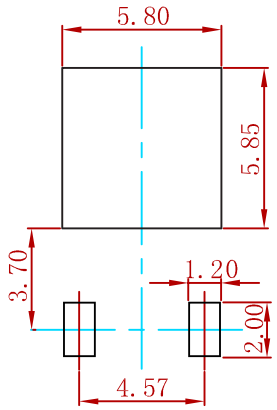
Fig.8 Gate Charge Waveform

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

REELSPECIFICATION

P/N	PKG	QTY
MS15N10	TO-252	2500

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