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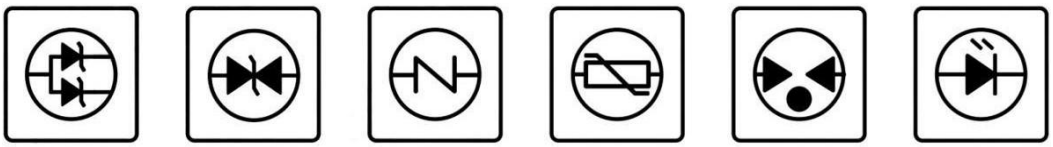
SEMICONDUCTOR



STU417S

Product specification

Description

The STU417S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

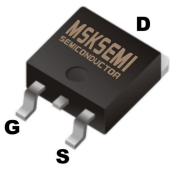
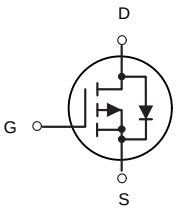
General Features

- V_{DS} = -40V I_D =-50A
- $R_{DS(ON)}$ < 13 mΩ @V_{GS}=10V

Application

- Battery protection
- Load switch
- Uninterruptible power supply

Reference News

PACKAGE OUTLINE	P-Channel MOSFET	Marking
 TO-252		MSKSEMI STU417S MS17P

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-40	V
VGS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	-50	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	-31	A
IDM	Pulsed Drain Current[2]	-200	A
P_D@T_C=25℃	Total Power Dissipation[4]	55	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
R_{θ}JA	Thermal Resistance Junction-ambient [1]	61	℃/W
R_{θ}JC	Thermal Resistance Junction-Case[1]	2.27	℃/W

Electrical Characteristics（T_J= 25°C, unless otherwise noted）

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	5	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance[4]		$R_{DS(on)}$	V_{GS} = -10V, I_D = -16A	-	10.5	13	mΩ
			V_{GS} = -4.5V, I_D = -12A	-	14.2	20	
Forward Transconductance[4]		g_{fs}	V_{DS} = -10V, I_D = -16A	-	44	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = -20V, V_{GS} =0V, f =1MHz	-	3050	-	pF
Output Capacitance		C_{oss}		-	282	-	
Reverse Transfer Capacitance		C_{rss}		-	230	-	
Gate Resistance		R_g	f =1MHz	-	9	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = -10V,V_{DS} = -20V, I_D= -16A	-	28	-	nC
Gate-Source Charge		Q_{gs}		-	8	-	
Gate-Drain Charge		Q_{gd}		-	8.5	-	
Turn-on Delay Time		$t_{d(on)}$	V_{GS} =-10V, V_{DD} = -15V, R_G = 3Ω, I_D= -16A	-	38	-	ns
Rise Time		t_r		-	31	-	
Turn-off Delay Time		$t_{d(off)}$		-	90	-	
Fall Time		t_f		-	9.2	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = -1A, V_{GS} = 0V	-	-	-1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	-50	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V,L=0.1mH,I_{AS}= -40A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Characteristics

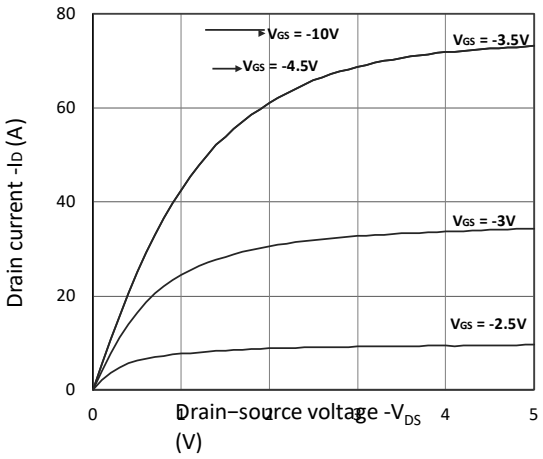


Figure 1. Output Characteristics

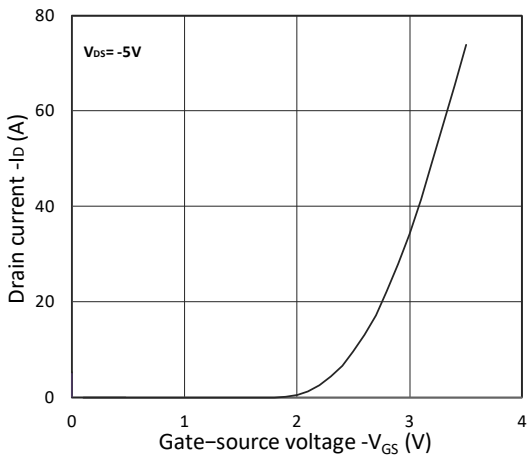


Figure 2. Transfer Characteristics

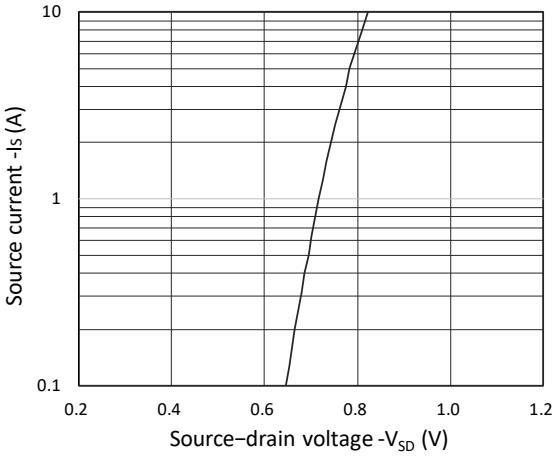


Figure 3. Forward Characteristics of Reverse

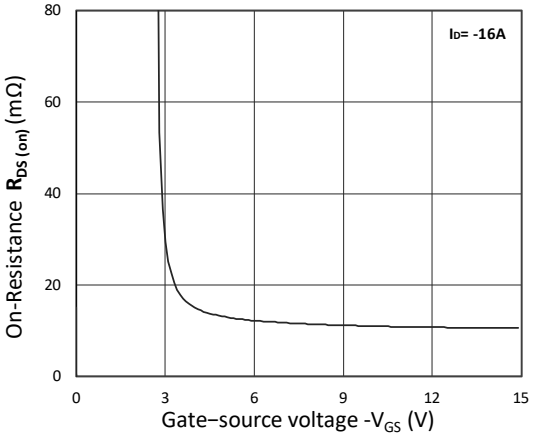


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

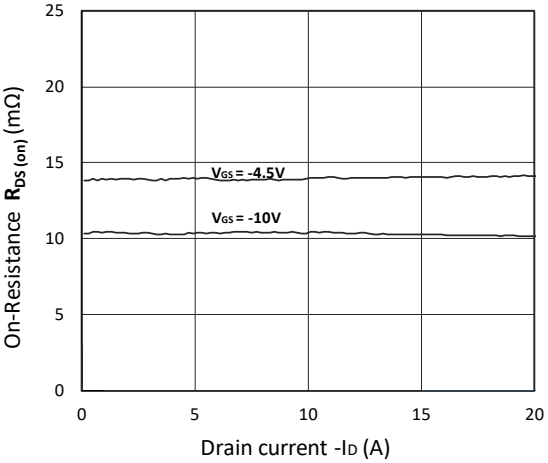


Figure 5. $R_{DS(ON)}$ vs. I_D

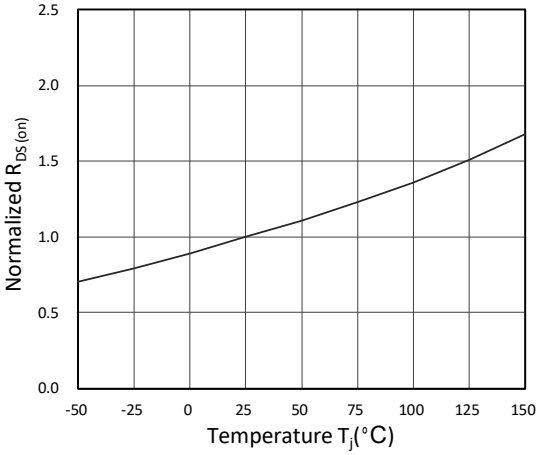


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

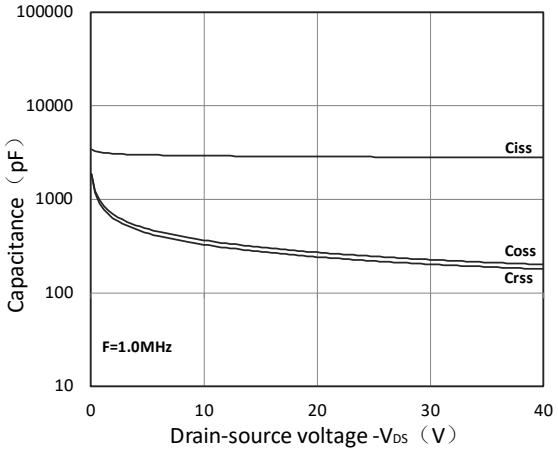


Figure 7. Capacitance Characteristics

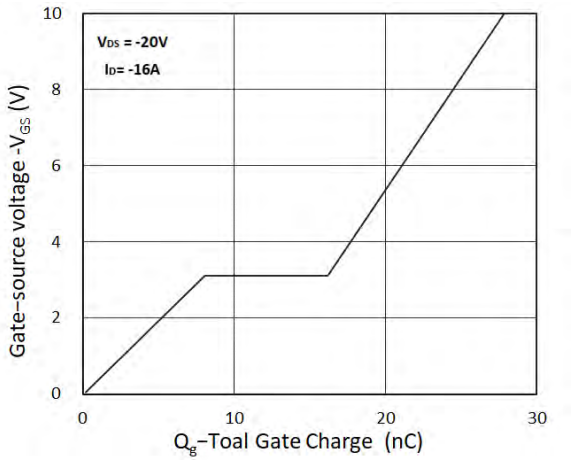


Figure 8. Gate Charge Characteristics

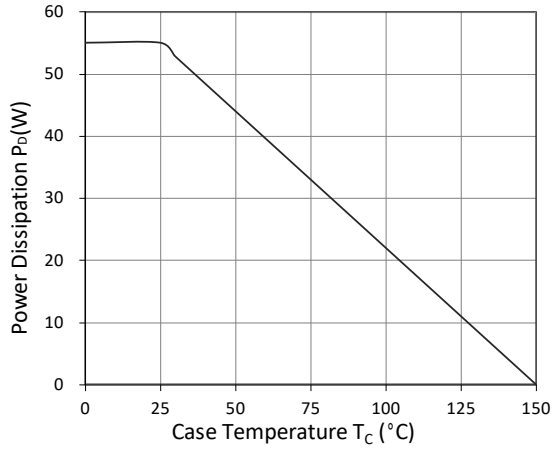


Figure 9. Power Dissipation

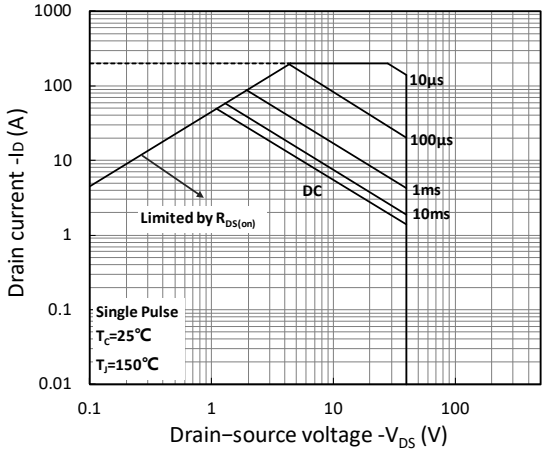


Figure10. Safe Operating Area

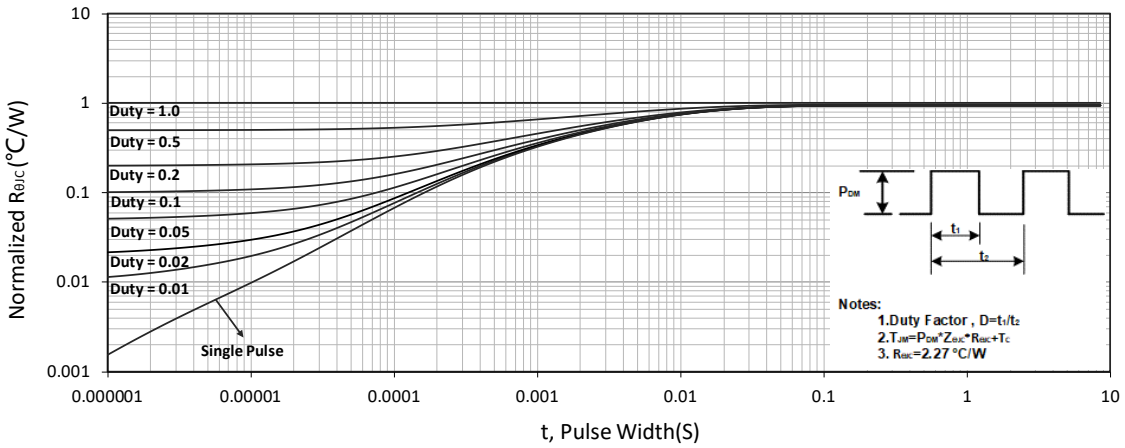


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

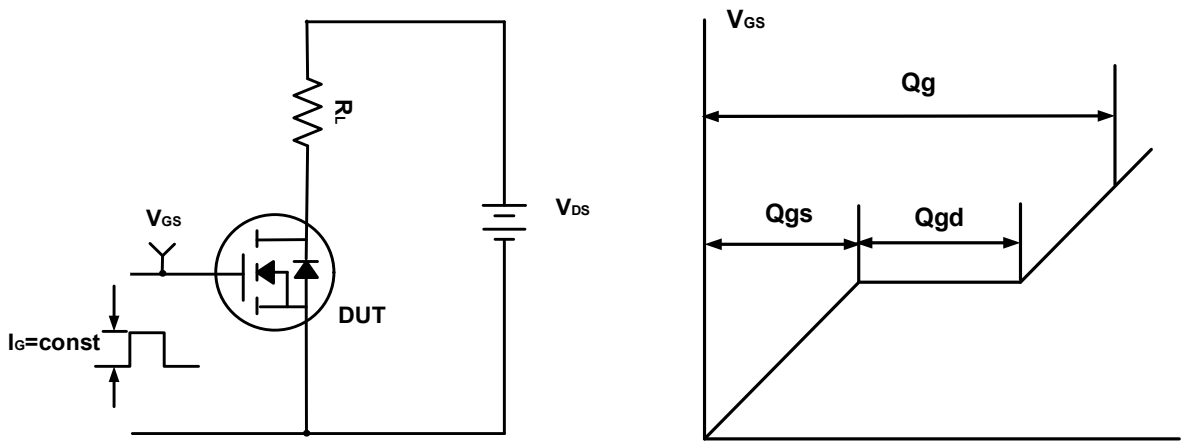


Figure A. Gate Charge Test Circuit & Waveforms

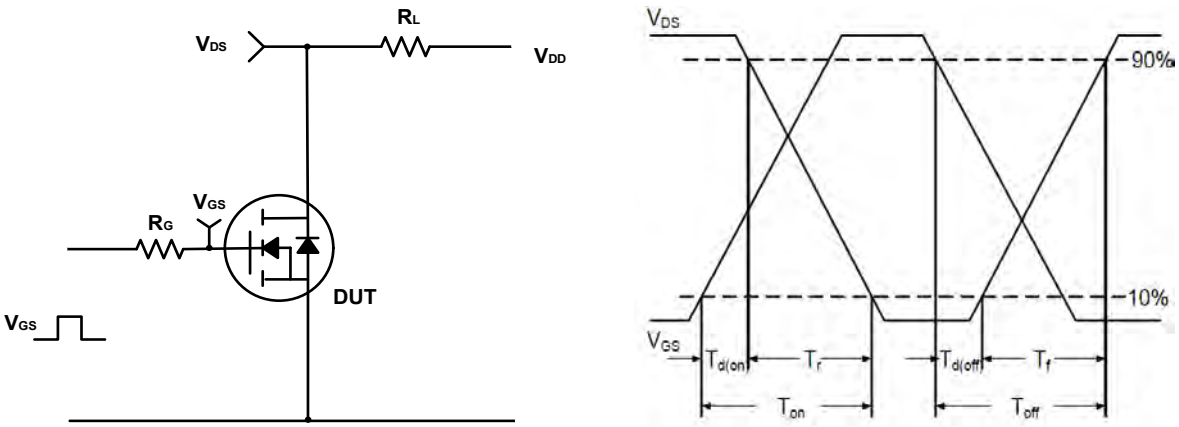


Figure B. Switching Test Circuit & Waveforms

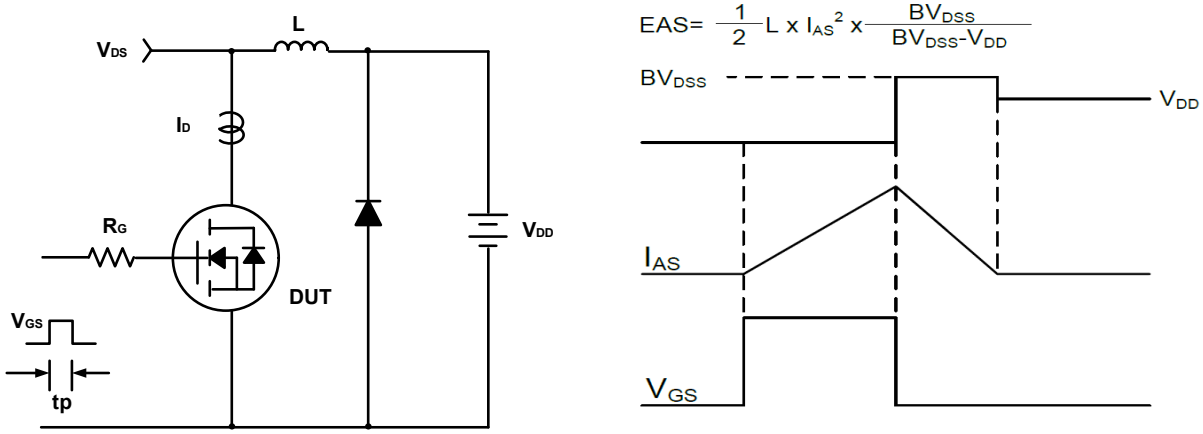
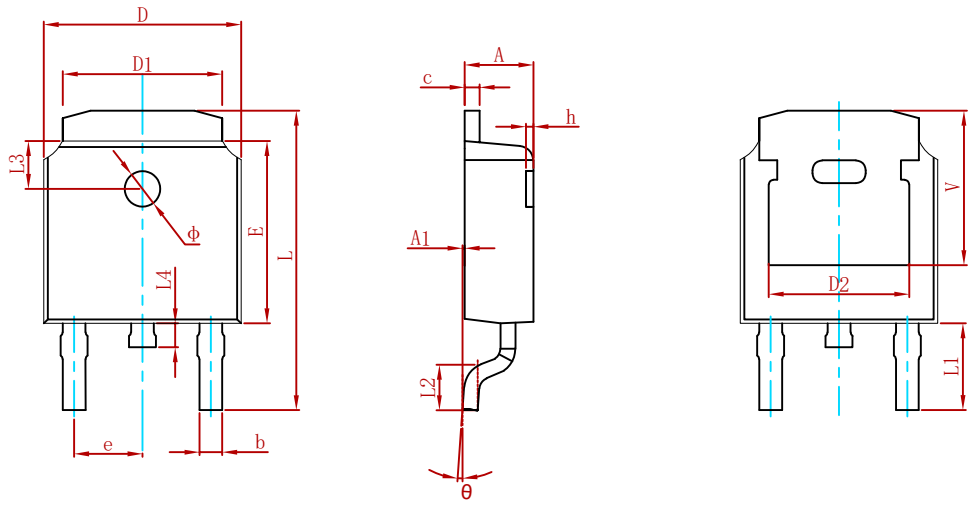


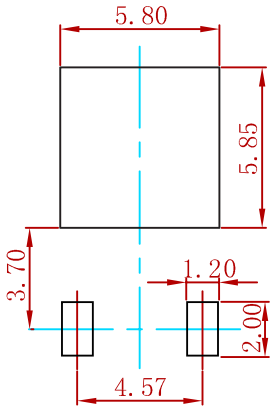
Figure C. Unclamped Inductive Switching Circuit & Waveforms

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

REELSPECIFICATION

P/N	PKG	QTY
STU417S	TO-252	2500

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