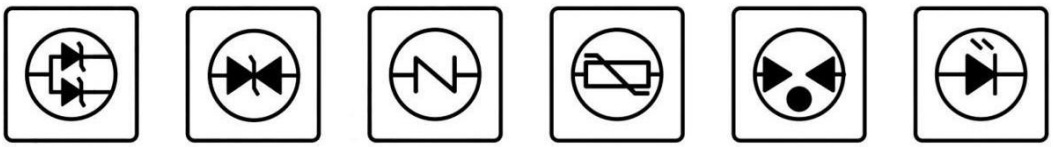
MSKSEMI 美森科
SEMICONDUCTOR



4953

Product specification

Description

These Dual P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications

BVDSS	RDSON	ID
-30V	40mΩ	-5.5A

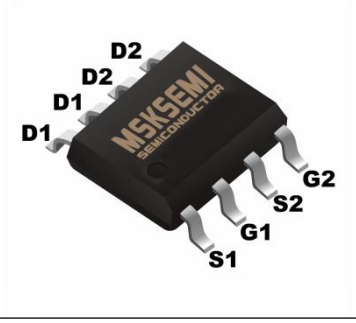
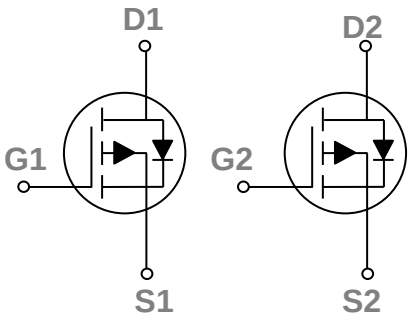
Features

- -30V,-5.5A, RDS(ON) =40mΩ@VGS = -10V
- Fast switching
- Green Device Available
- Suit for -4.5V Gate Drive Applications

Applications

- Notebook
- Load Switch
- Battery Protection
- Hand-held Instruments

Reference News

PACKAGE OUTLINE	P-Channel and P-Channel	Marking
 SOP-8		MSKSEMI 4953 BPP

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current - Continuous (T_C=25℃)	-5.5	A
	Drain Current - Continuous (T_C=100℃)	-3.48	A
I_{DM}	Drain Current - Pulsed[1]	-22	A
P_D	Power Dissipation (T_C=25℃)	2.1	W
	Power Dissipation - Derate above 25℃	0.017	W/℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	60	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.03	---	V/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=125℃	---	---	-10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}= ±20V , V_{DS}=0V	---	---	±100	nA

On Characteristics

$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V , I_D=-3A	---	40	55	mΩ
		V_{GS}=-4.5V , I_D=-2A	---	60	80	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.6	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4	---	mV/℃
gfs	Forward Transconductance	V_{DS}=-10V , I_D=-3A	---	3.5	---	S

Dynamic and switching Characteristics

Q_g	Total Gate Charge[2,3]	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-3A	---	5.1	---	nC
Q_{gs}	Gate-Source Charge[2,3]		---	2	---	
Q_{gd}	Gate-Drain Charge[2,3]		---	2.2	---	
$T_{d(on)}$	Turn-On Delay Time[2,3]	V_{DD}=-15V , V_{GS}=-10V , R_G=6Ω I_D=-1A	---	3.4	---	ns
T_r	Rise Time[2,3]		---	10.8	---	
$T_{d(off)}$	Turn-Off Delay Time[2,3]		---	26.9	---	
T_f	Fall Time[2,3]		---	6.9	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , F=1MHz	---	560	---	pF
C_{oss}	Output Capacitance		---	55	---	
C_{rss}	Reverse Transfer Capacitance		---	40	---	

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	---	---	-5.5	A
I_{SM}	Pulsed Source Current		---	---	-11	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :
1.Repetitive Rating : Pulsed width limited by maximum junction temperature.
2.V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=11A.,R_G=25Ω,Starting T_J=25℃.
3.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
4.Essentially independent of operating temperature.

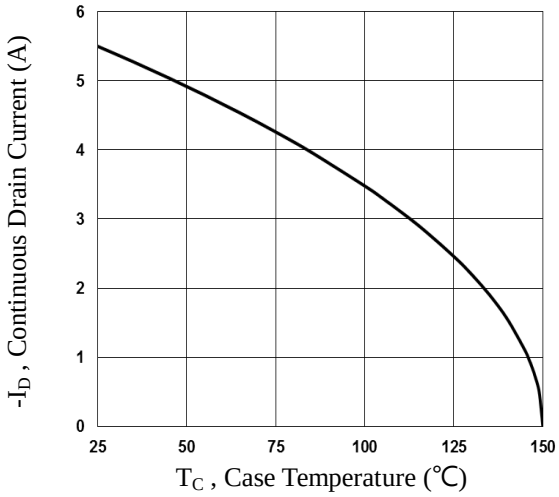


Fig.1 Continuous Drain Current vs. T_C

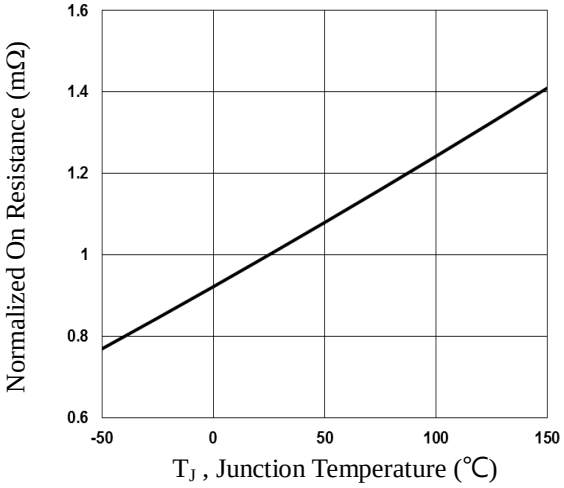


Fig.2 Normalized RDSON vs. T_J

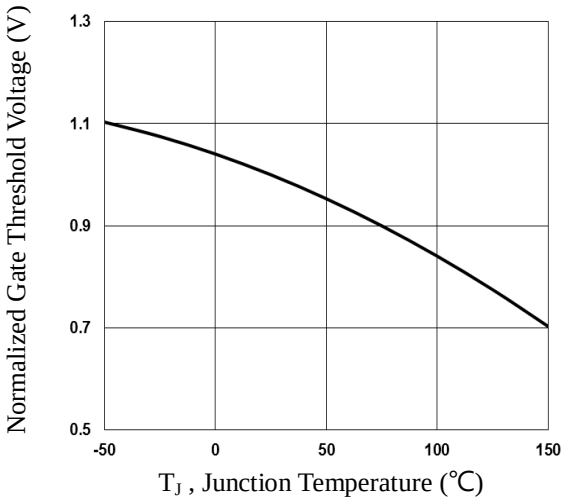


Fig.3 Normalized V_{th} vs. T_J

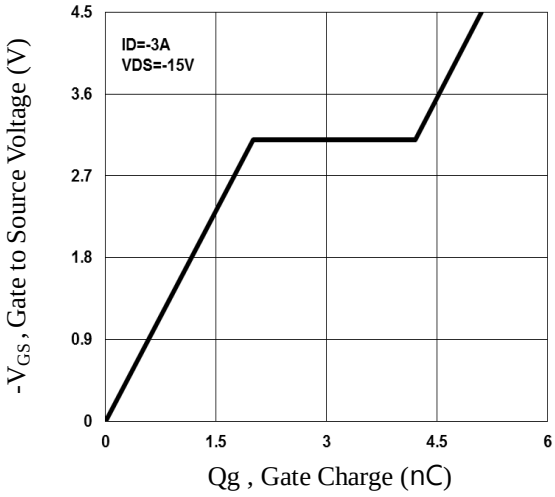


Fig.4 Gate Charge Waveform

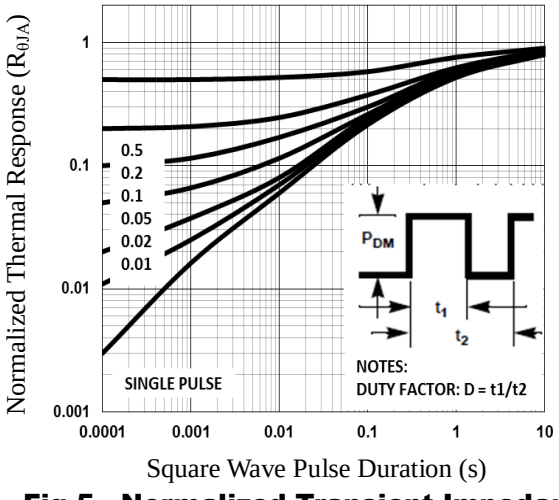


Fig.5 Normalized Transient Impedance

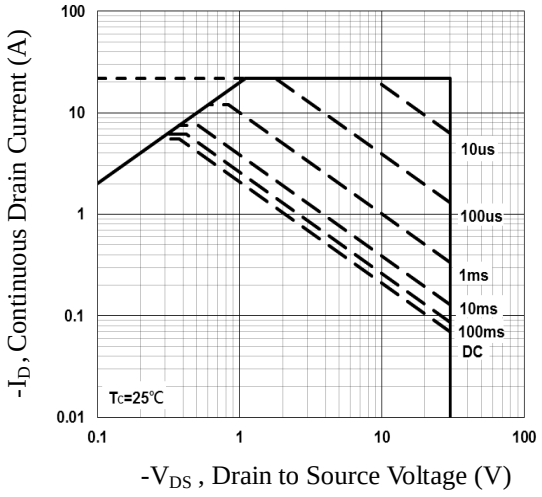


Fig.6 Maximum Safe Operation Area

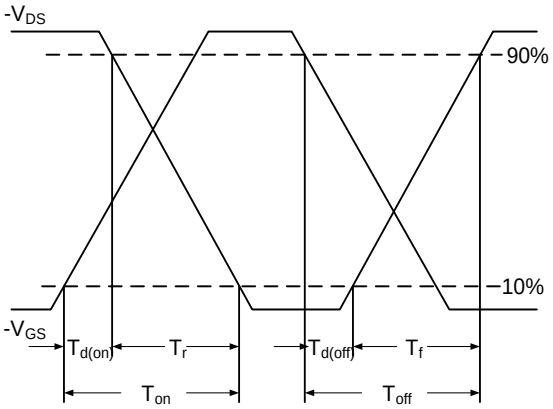


Fig.7 Switching Time Waveform

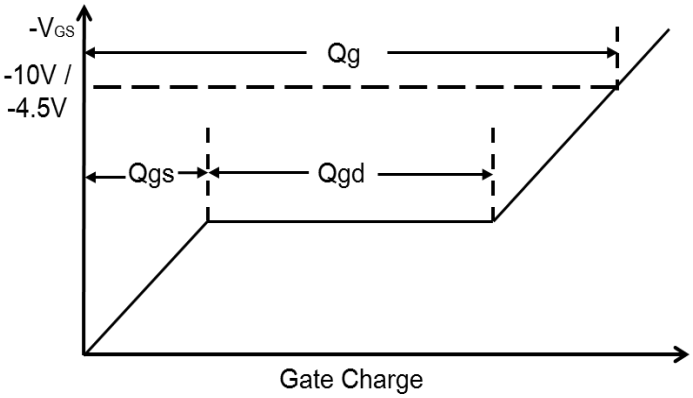
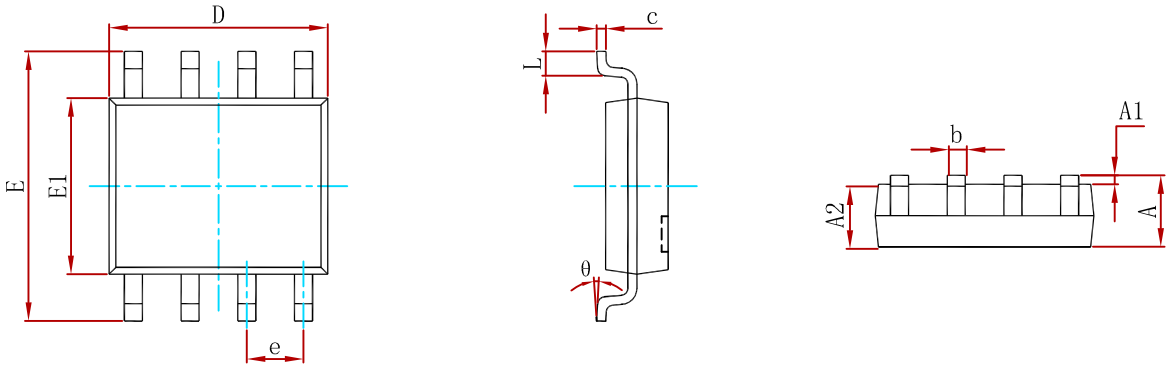


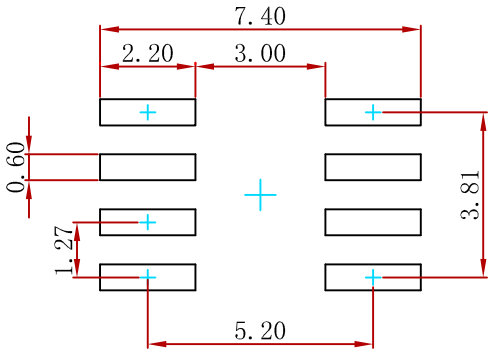
Fig.8 Gate Charge Waveform

PACKAGEMECHANICALDATA



Symbol	DimensionsInMillimeters		DimensionsInInches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

REELSPECIFICATION

P/N	PKG	QTY
4953	SOP-8	3000

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