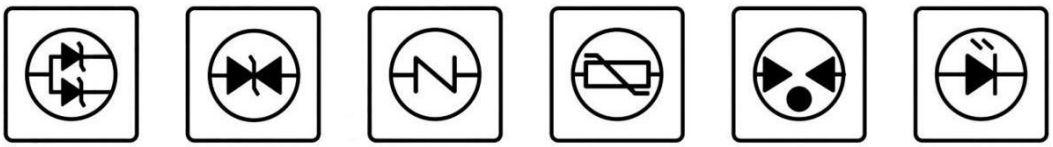
MSKSEMI 美森科
SEMICONDUCTOR



SI2305CDS

Product specification

Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

BVDSS	RDSON	ID
-12V	25mΩ	-5.5A

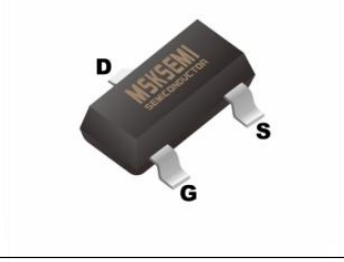
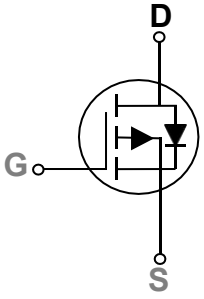
Features

- -20V,-5.5A, RDS(ON) =25mΩ@VGS = -4.5V
- Improved dv/dt capability
- Fast switching
- Green Device Available

Applications

- Notebook
- Load Switch
- Battery Protection
- Hand-held Instruments

Reference News

PACKAGE OUTLINE	P-Channel MOSFET	Marking
 SOT-23		N5***

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-12	V
V_{GS}	Gate-Source Voltage	±12	V
I_D	Drain Current – Continuous (T_C=25℃)	-5.5	A
	Drain Current – Continuous (T_C= 100℃)	-3.5	A
I_{DM}	Drain Current – Pulsed[1]	-21.2	A
P_D	Power Dissipation (T_C=25℃)	1.56	W
	Power Dissipation – Derate above 25℃	0.012	W/℃
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction to ambient	---	80	℃/W

Copyright© Msksemi Incorporated

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Off Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-12	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.02	---	V/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-20V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-16V , V_{GS}=0V , T_J= 125℃	---	---	-10	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA

On Characteristics

$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V , I_D=-4A	---	25	35	mΩ
		V_{GS}=-2.5V , I_D=-3A	---	35	50	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.3	-0.6	-1	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2	---	mV/℃
gfs	Forward Transconductance	V_{DS}=-12V , I_S=-3A	---	8.4	---	S

Dynamic and switching Characteristics

Q_g	Total Gate Charge[2] , [3]	V_{DS}=-10V , V_{GS}=-4.5V , I_D=-4A	---	16.1	---	nC
Q_{gs}	Gate-Source Charge[2] , [3]		---	1.8	---	
Q_{gd}	Gate-Drain Charge[2] , [3]		---	3.8	---	
$T_{d(on)}$	Turn-On Delay Time[2] , [3]	V_{DD}=-10V , V_{GS}=-4.5V , R_G=25Ω I_D=-1A	---	8.2	---	nS
T_r	Rise Time[2] , [3]		---	30	---	
$T_{d(off)}$	Turn-Off Delay Time[2] , [3]		---	71.1	---	
T_f	Fall Time[2] , [3]		---	19.8	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , F= 1MHz	---	1440	---	pF
C_{oss}	Output Capacitance		---	155	---	
C_{rss}	Reverse Transfer Capacitance		---	115	---	

Drain-Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	V_G=V_D=0V , Force Current	---	---	-5.5	A
I_{SM}	Pulsed Source Current		---	---	-21.2	A
V_{SD}	Diode Forward Voltage	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1.2	V

Note :

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

Copyright© Msksemi Incorporated

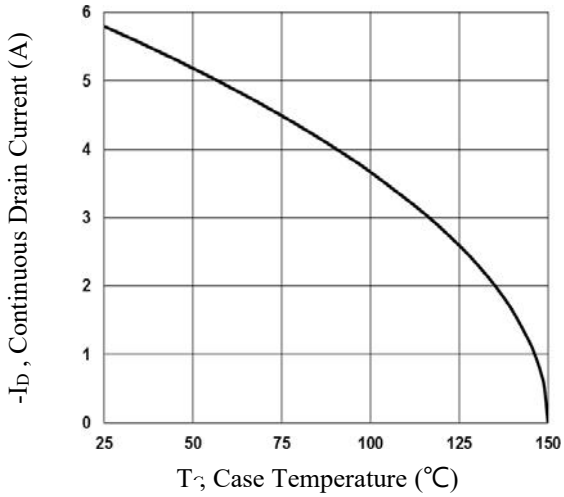


Fig.1 Continuous Drain Current vs. T_C

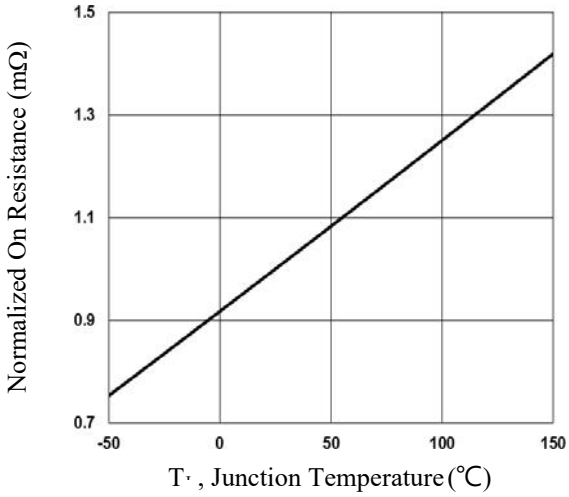


Fig.2 Normalized RDSON vs. T_J

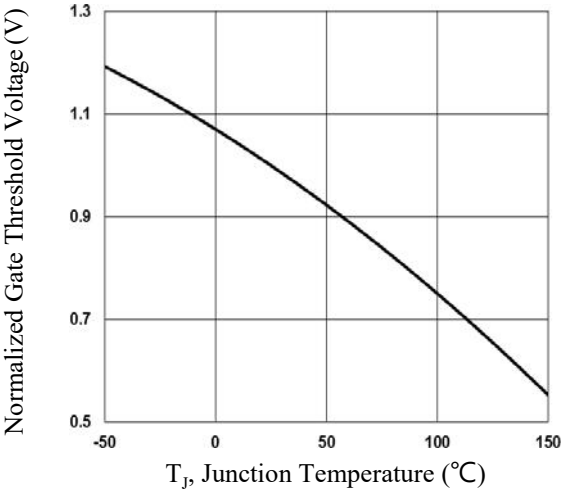


Fig.3 Normalized V_{th} vs. T_J

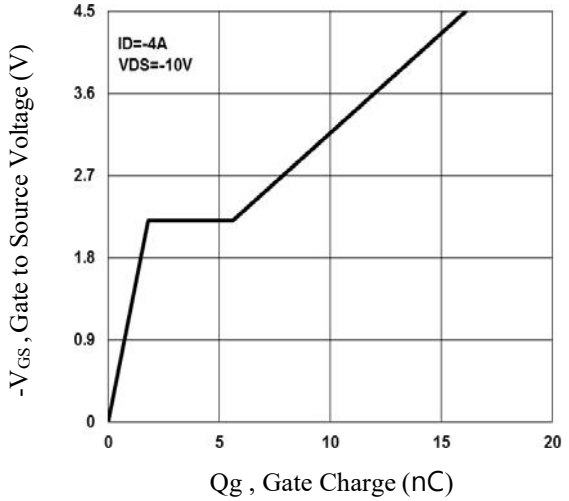


Fig.4 Gate Charge Waveform

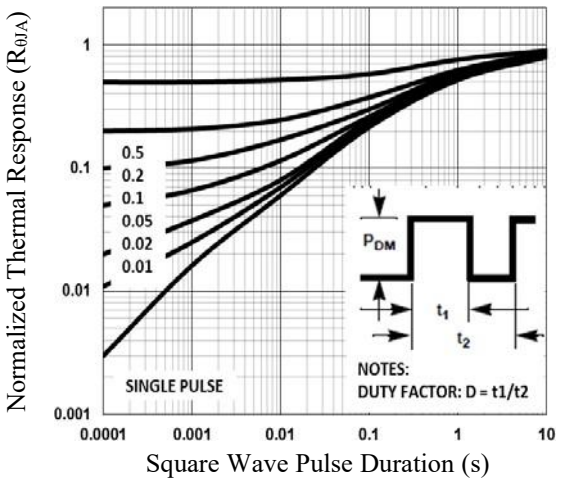


Fig.5 Normalized Transient Impedance

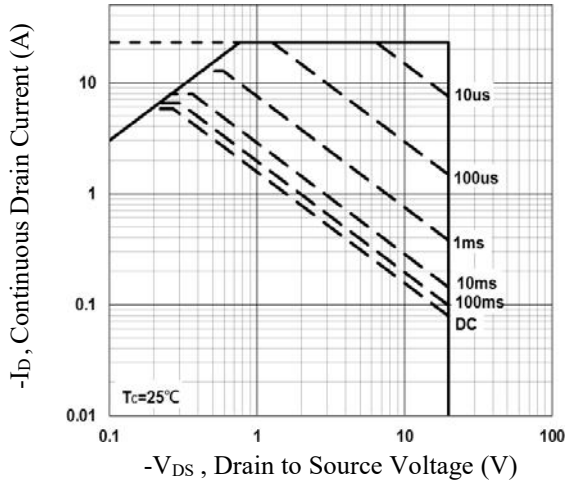
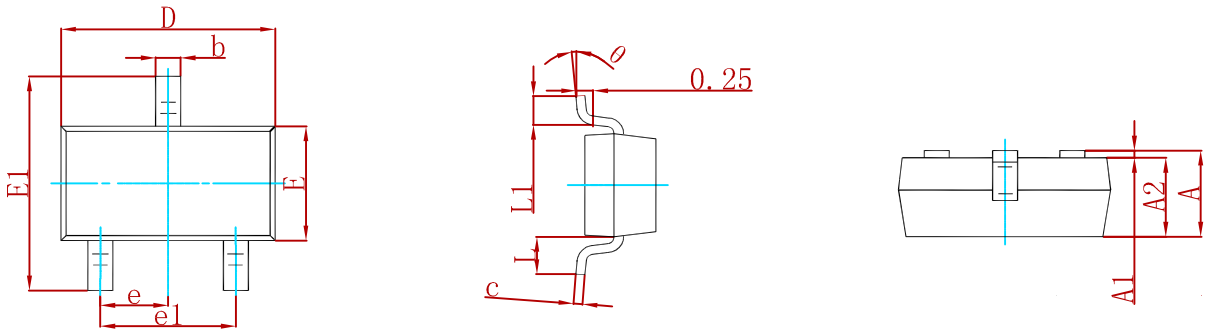


Fig.6 Maximum Safe Operation Area

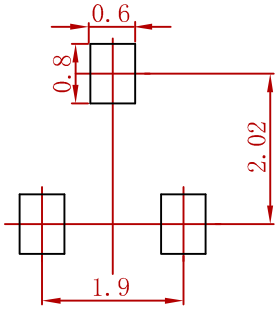
Copyright© Msksemi Incorporated

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

REELSPECIFICATION

P/N	PKG	QTY
SI2305CDS	SOT-23	3000

Copyright© Msksemi Incorporated

Attention

■ Any and all MSKSEMI Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MSKSEMI Semiconductor representative nearest you before using any MSKSEMI Semiconductor products described or contained herein in such applications.

■ MSKSEMI Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specificationsof any andall MSKSEMI Semiconductor products described orcontained herein.

■ Specifications of any and all MSKSEMI Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer'sproducts orequipment.

■ MSKSEMI Semiconductor. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with someprobability. It is possiblethat these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits anderror prevention circuitsfor safedesign, redundant design, and structural design.

■ In the event that any or all MSKSEMI Semiconductor products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from theauthorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MSKSEMI Semiconductor.

■ Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MSKSEMI Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringementsof intellectual property rights or other rightsof third parties.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. Whendesigning equipment, referto the "Delivery Specification" for the MSKSEMI Semiconductor productthat you intend to use.

Copyright© Msksemi Incorporated