

## Power MOSFET

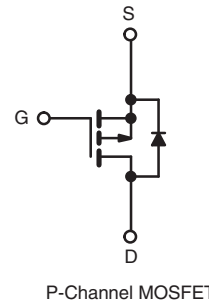
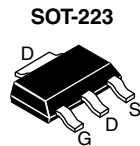
PRODUCT SUMMARY		
$V_{DS}$ (V)	-250	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10\text{ V}$	1.2
$Q_g$ (Max.) (nC)	8.7	
$Q_{gs}$ (nC)	2.2	
$Q_{gd}$ (nC)	4.1	
Configuration	Single	

### FEATURES

- Surface mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	-250	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at - 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	-2.1	A
		T <sub>C</sub> = 100 °C		-1.69	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	-8.8	
Linear Derating Factor				0.025	W/°C
Linear Derating Factor (PCB Mount) <sup>e</sup>				0.017	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	100	mJ
Avalanche Current <sup>a</sup>			I <sub>AR</sub>	-1.1	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	0.31	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	3.1	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	T <sub>A</sub> = 25 °C			2.0	
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	-5.5	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s			300	

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 7.7\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = -4.4\text{ A}$  (see fig. 12).
- $I_{SD} \leq -4.4\text{ A}$ ,  $dI/dt \leq -75\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	60	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	40	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS** ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-250	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = -1\text{ mA}$		-	-0.091	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -0.66\text{ A}^b$	-	1.2	-	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -0.66\text{ A}$		0.82	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = -25\text{ V},$ $f = 1.0\text{ MHz, see fig. 5}$		-	200	-	pF
Output Capacitance	$C_{oss}$			-	94	-	
Reverse Transfer Capacitance	$C_{rss}$			-	18	-	
Total Gate Charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -4.0\text{ A}, V_{DS} = -80\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	8.7	nC
Gate-Source Charge	$Q_{gs}$			-	-	2.2	
Gate-Drain Charge	$Q_{gd}$			-	-	4.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, I_D = -4.0\text{ A},$ $R_G = 24\text{ }\Omega, R_D = 11\text{ }\Omega, \text{ see fig. 10}^b$		-	10	-	ns
Rise Time	$t_r$			-	27	-	
Turn-Off Delay Time	$t_{d(off)}$			-	15	-	
Fall Time	$t_f$			-	17	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	$L_S$			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	-1.1	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	-8.8	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-5.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -4.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	80	160	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.15	0.30	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

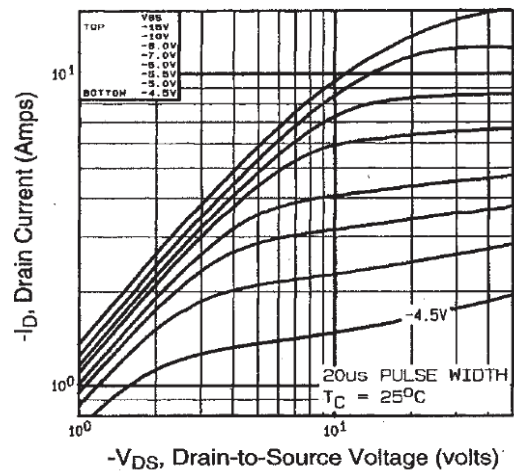


Fig. 1 - Typical Output Characteristics

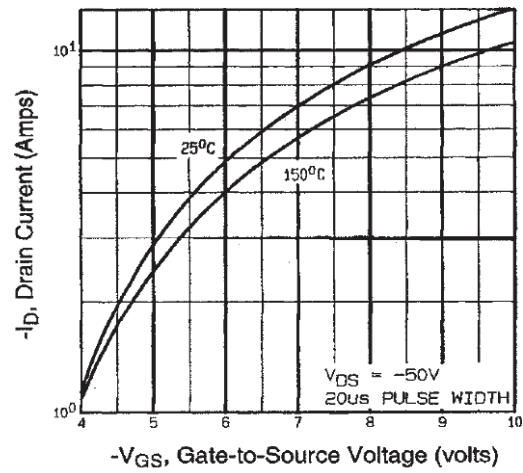


Fig. 3 - Typical Transfer Characteristics

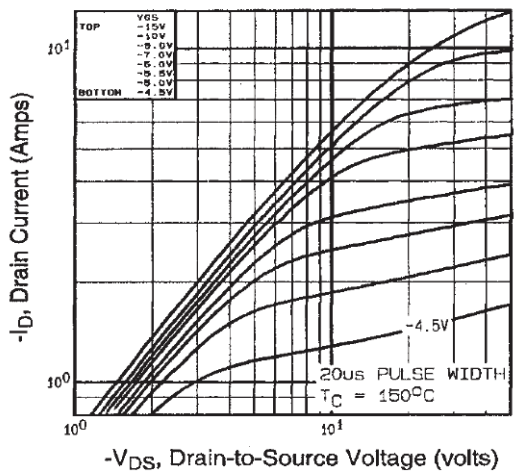


Fig. 2 - Typical Output Characteristics

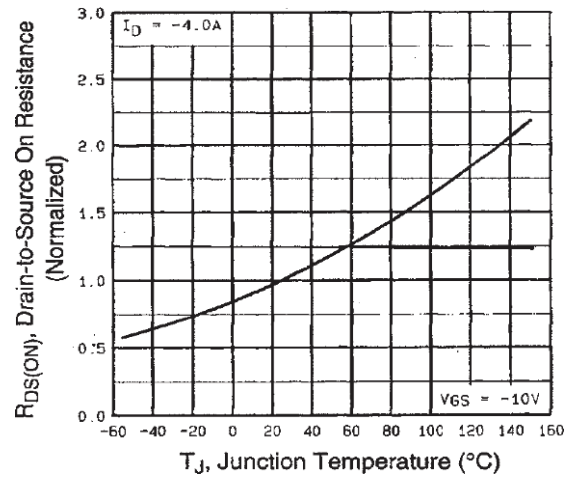


Fig. 4 - Normalized On-Resistance vs. Temperature

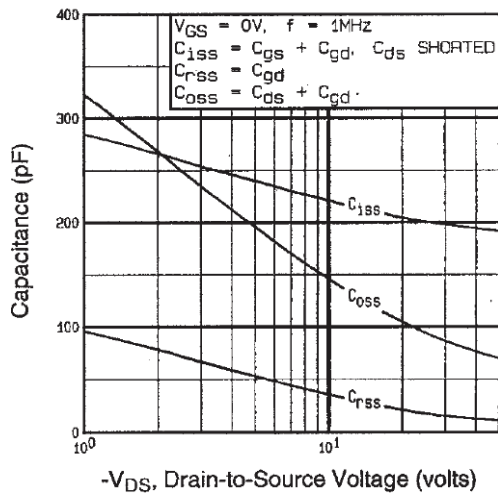


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

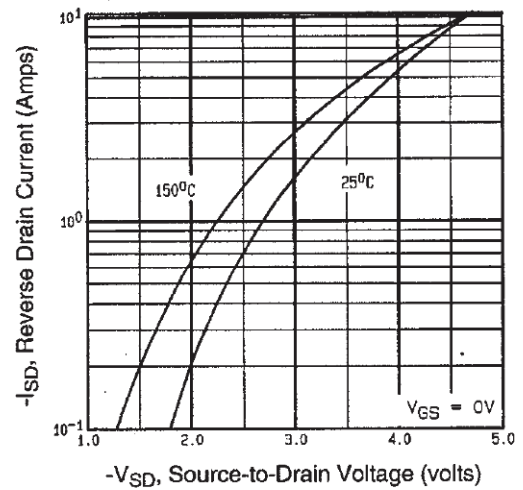


Fig. 7 - Typical Source-Drain Diode Forward Voltage

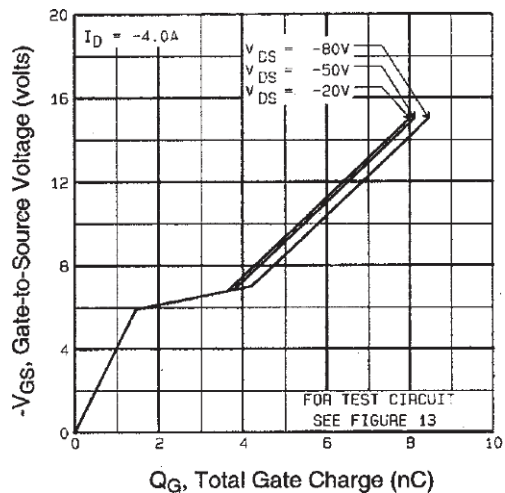


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

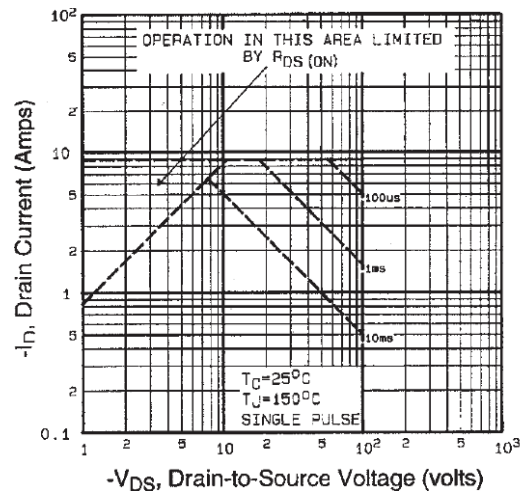


Fig. 8 - Maximum Safe Operating Area

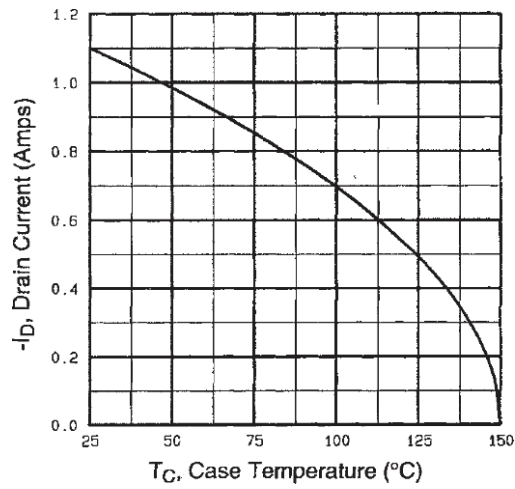


Fig. 9 - Maximum Drain Current vs. Case Temperature

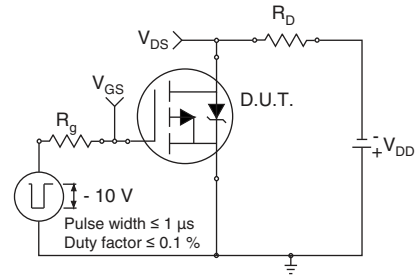


Fig. 10a - Switching Time Test Circuit

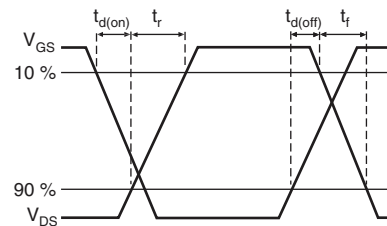


Fig. 10b - Switching Time Waveforms

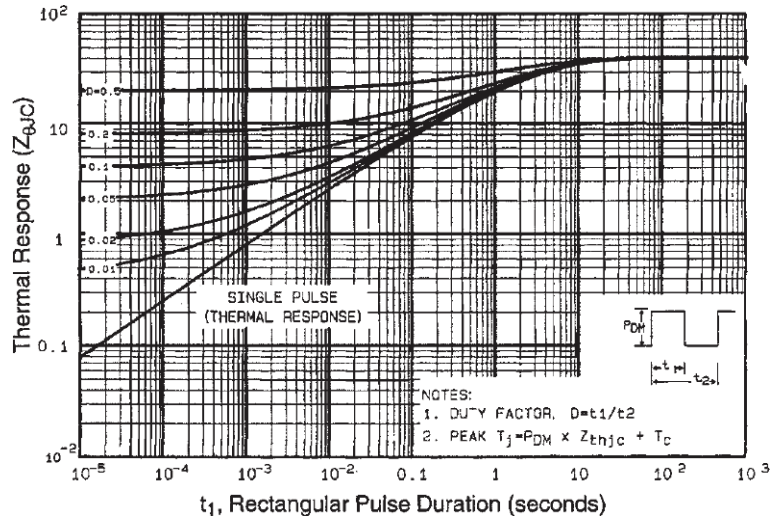


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

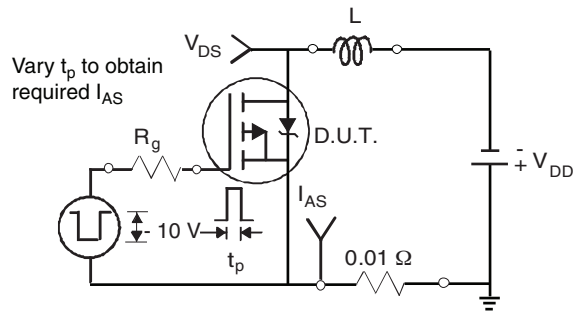


Fig. 12a - Unclamped Inductive Test Circuit

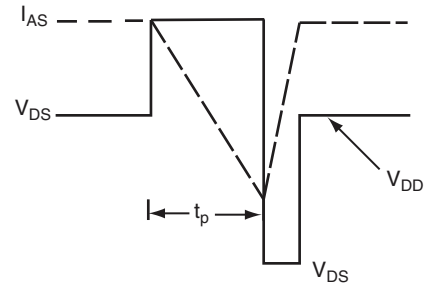


Fig. 12b - Unclamped Inductive Waveforms

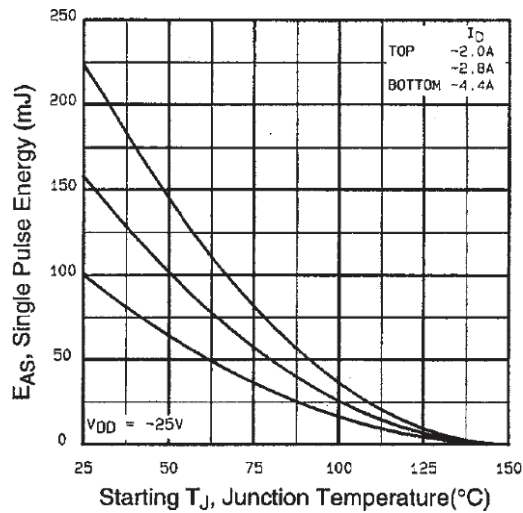


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

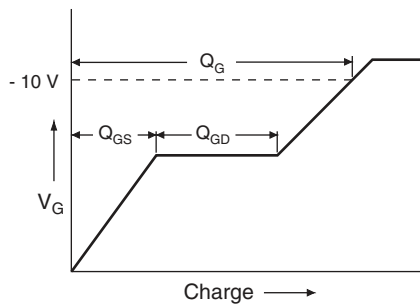


Fig. 13a - Basic Gate Charge Waveform

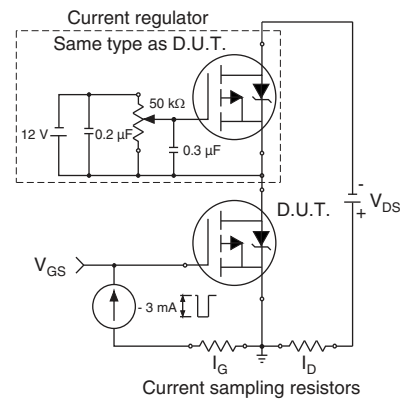
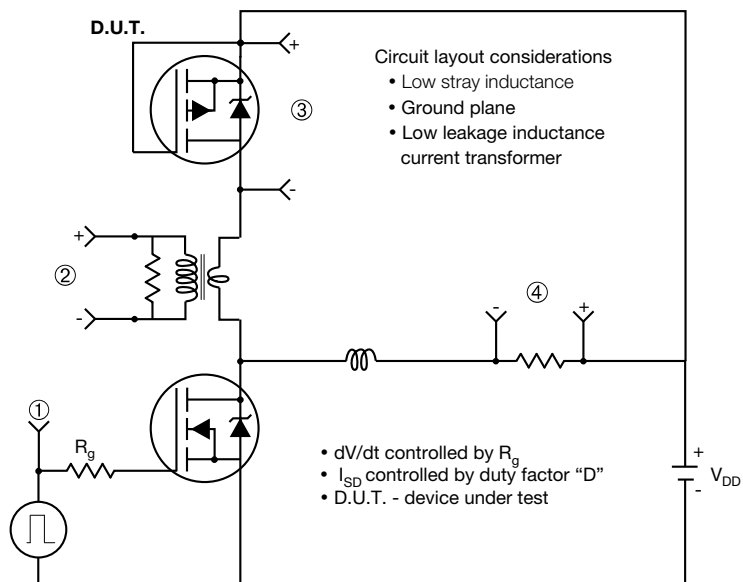
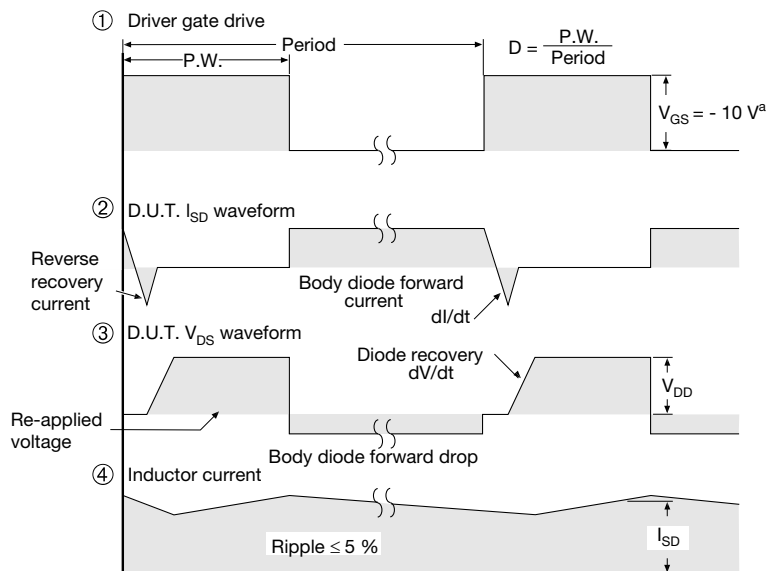


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

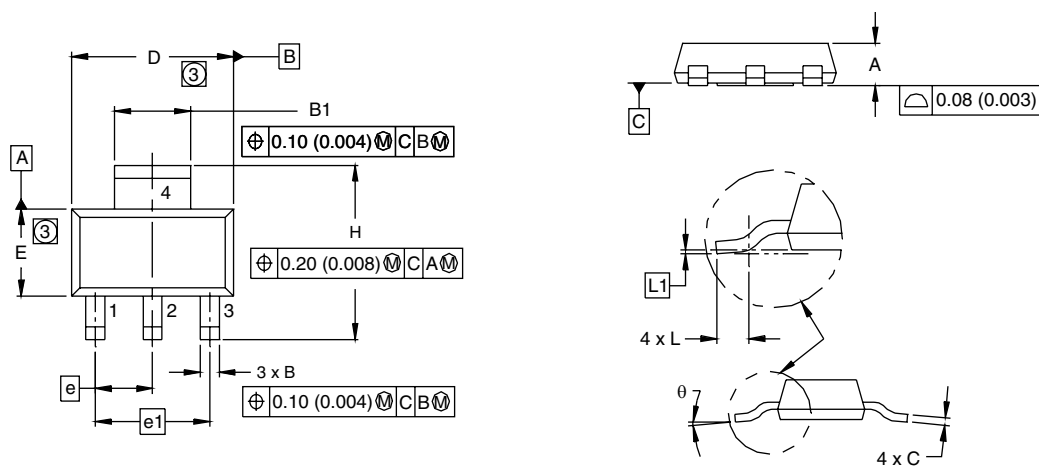


**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 14 - For P-Channel**

**SOT-223 (HIGH VOLTAGE)**

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10°	-	10°
ECN: S-82109-Rev. A, 15-Sep-08 DWG: 5969				

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.



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