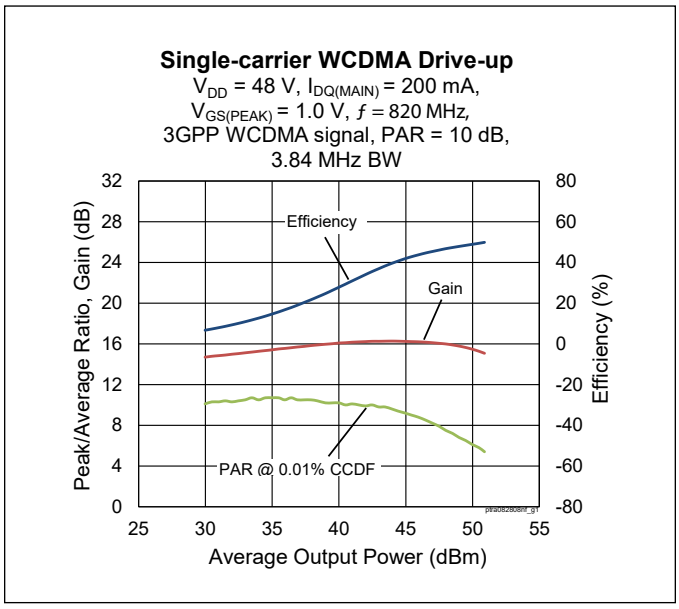
PTRA082808NF

Thermally-Enhanced High Power RF LDMOS FET
280 W, 48 V, 790 – 820 MHz

Package Types: PG-HBSOF-6-2

Description

The PTRA082808NF is a 280-watt LDMOS FET intended for use in multi-standard cellular power amplifier applications in the 790 to 820 MHz frequency band. Features include input and output matching, high gain and thermally-enhanced package with earless flanges. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



Features

- Broadband internal input and output matching
- Asymmetrical design
  - Main: P_{1dB} = 115 W Typ
  - Peak: P_{1dB} = 165 W Typ
- Typical Pulsed CW performance, 820 MHz, 48 V, Doherty configuration
  - Output power at P_{3dB} = 250 W
  - Efficiency = 55.6 %
  - Gain = 16.2 dB
- Capable of handling 10:1 VSWR @ 48 V, 56.2 W (CW) output power
- Human Body Model Class 1C (per ANSI/ESDA/JEDEC JS-001)
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty test fixture)
V_{DD} = 48 V, I_{DQ} = 200 mA, $V_{GS(PEAK)}$ = 1.0 V, P_{OUT} = 56.2 W avg, f = 820 MHz, 3GPP, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Gain	G_{ps}	15.2	15.5	—	dB
Drain Efficiency	η_D	42.7	44.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–36.4	–33.5	dBc
Output PAR @ 0.01% CCDF	OPAR	6.6	7.3	—	dB

Note:
All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

DC Characteristics (each side)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain-Source Breakdown Voltage	$V_{BR(DSS)}$	105	—	—	V	V_{GS} = 0 V, I_{DS} = 10 mA
Drain Leakage Current	I_{DSS}	—	—	1	µA	V_{DS} = 50 V, V_{GS} = 0 V
		—	—	10		V_{DS} = 105 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	1		V_{GS} = 10 V, V_{DS} = 0 V
On-State Resistance (main)	$R_{DS(on)}$	0.07	0.3	0.66	Ω	V_{GS} = 10 V, V_{DS} = 0.1 V
On-State Resistance (peak)		0.01	0.12	0.325		
Operating Gate Voltage (main)	V_{GS}	3.0	3.6	4.1	V	V_{DS} = 3.6 V, I_{DQ} = 0.2 A
Operating Gate Voltage (peak)		—	1	—		V_{DS} = 1.0 V, I_{DQ} = 0 A

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	105	V
Gate-source Voltage	V_{GS}	–6 to +12	
Operating Voltage	V_{DD}	0 to +55	
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

Characteristics	Symbol	Value	Unit	Conditions
Thermal Resistance (main)	$R_{\theta JC}$	0.766	°C/W	T_{CASE} = 70°C, 56.2 W CW
Thermal Resistance (peak)		0.208		T_{CASE} = 70°C, 200 W CW

Moisture Sensitivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTRA082808NF V1 R5	PTRA082808NF-V1-R5	PG-HBSOF-6-2	Tape & Reel, 500 pcs

Typical Performance (data taken in a production test fixture)

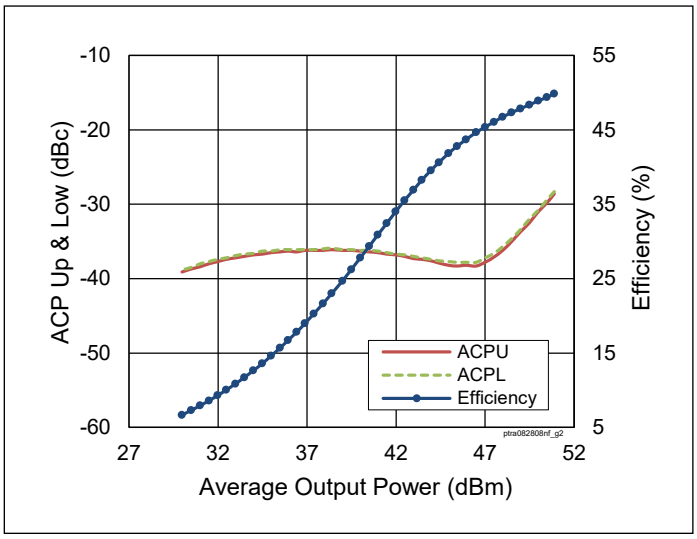


Figure 1. Single-carrier WCDMA Drive-up

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 1.0 V, f = 820 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz

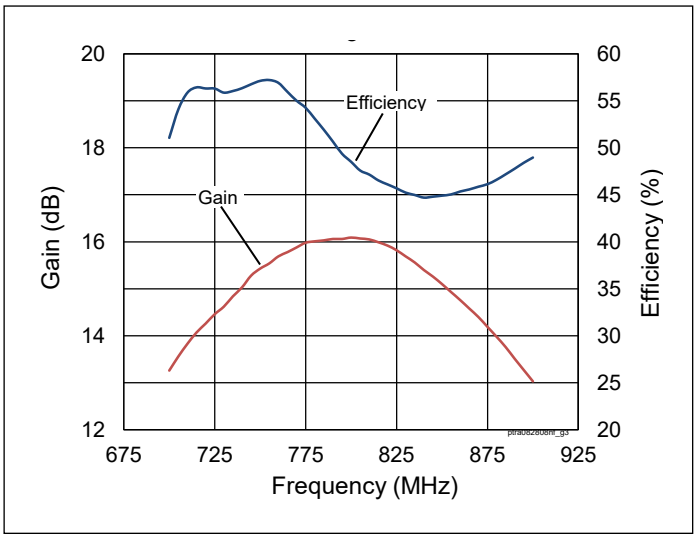


Figure 2. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 1.0 V, P_{OUT} = 47.5 dBm,
3GPP WCDMA signal, PAR = 10 dB

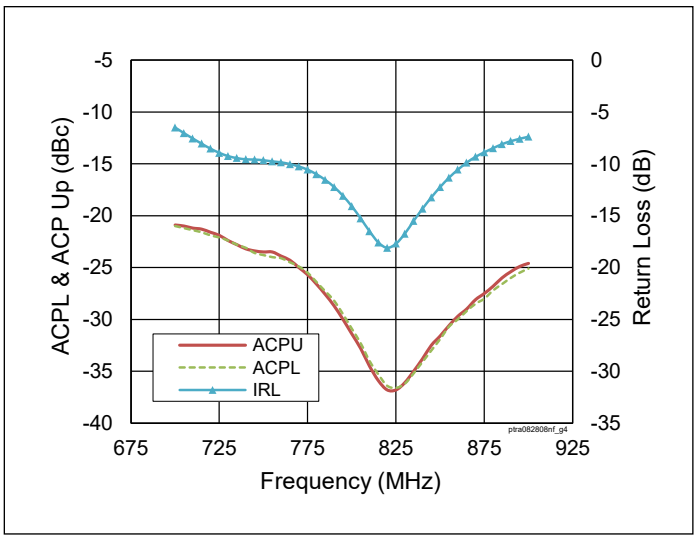


Figure 3. Single-carrier WCDMA Broadband Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 1.0 V, P_{OUT} = 47.5 dBm,
3GPP WCDMA signal, PAR = 10 dB

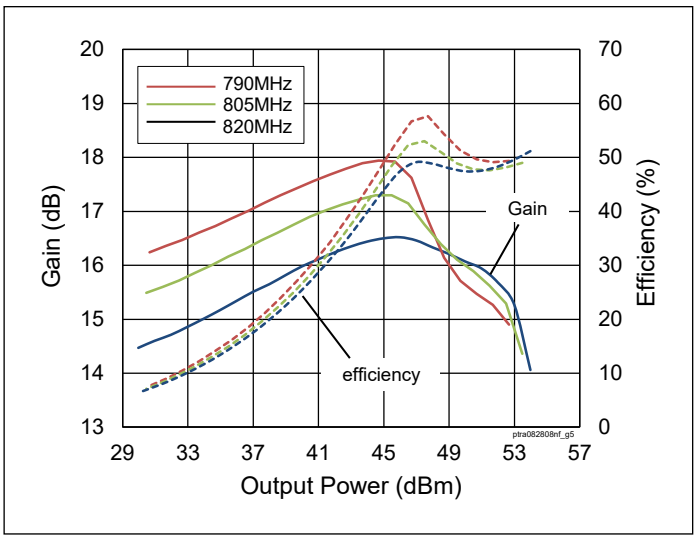


Figure 4. CW Performance

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 1.0 V

Typical Performance (cont.)

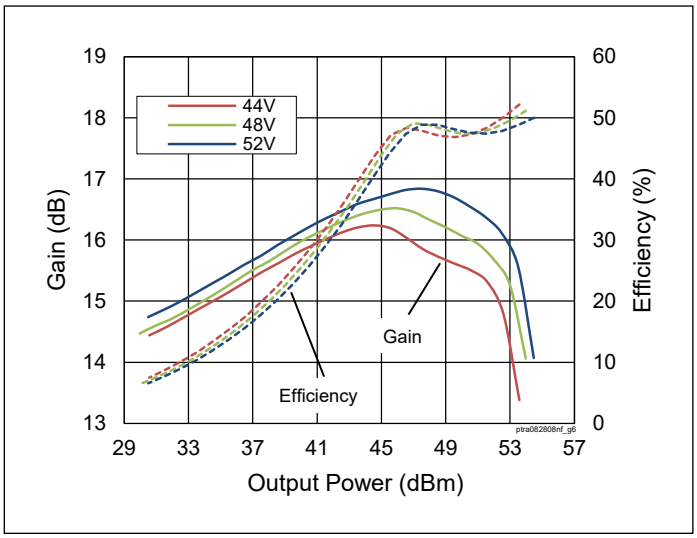


Figure 5. CW Performance at various V_{DD}

$I_{DQ(MAIN)}$ = 200 mA, $V_{GS(PEAK)}$ = 1.0 V,
f = 820 MHz

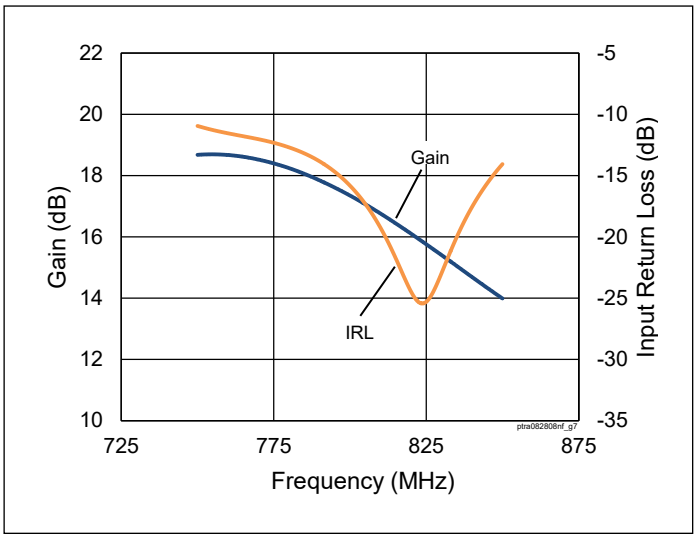


Figure 6. CW Performance Small Signal Gain & Input Return Loss

V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 200 mA,
$V_{GS(PEAK)}$ = 1.0 V

Load Pull Performance

Main Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 250 mA

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
790	1.8 – j4.4	2.4 – j1.6	20.24	51.73	149	58.9	5.4+ j2.6	22.49	48.72	74	69.8
805	1.8 – j5.2	2.6 – j1.8	20.28	51.47	140	58.6	5.4+ j2.5	22.41	48.74	75	70.2
820	1.8 – j5.2	2.9 – j1.8	20.65	51.41	138	60.9	5.3+ j1.9	22.51	48.97	79	70.4

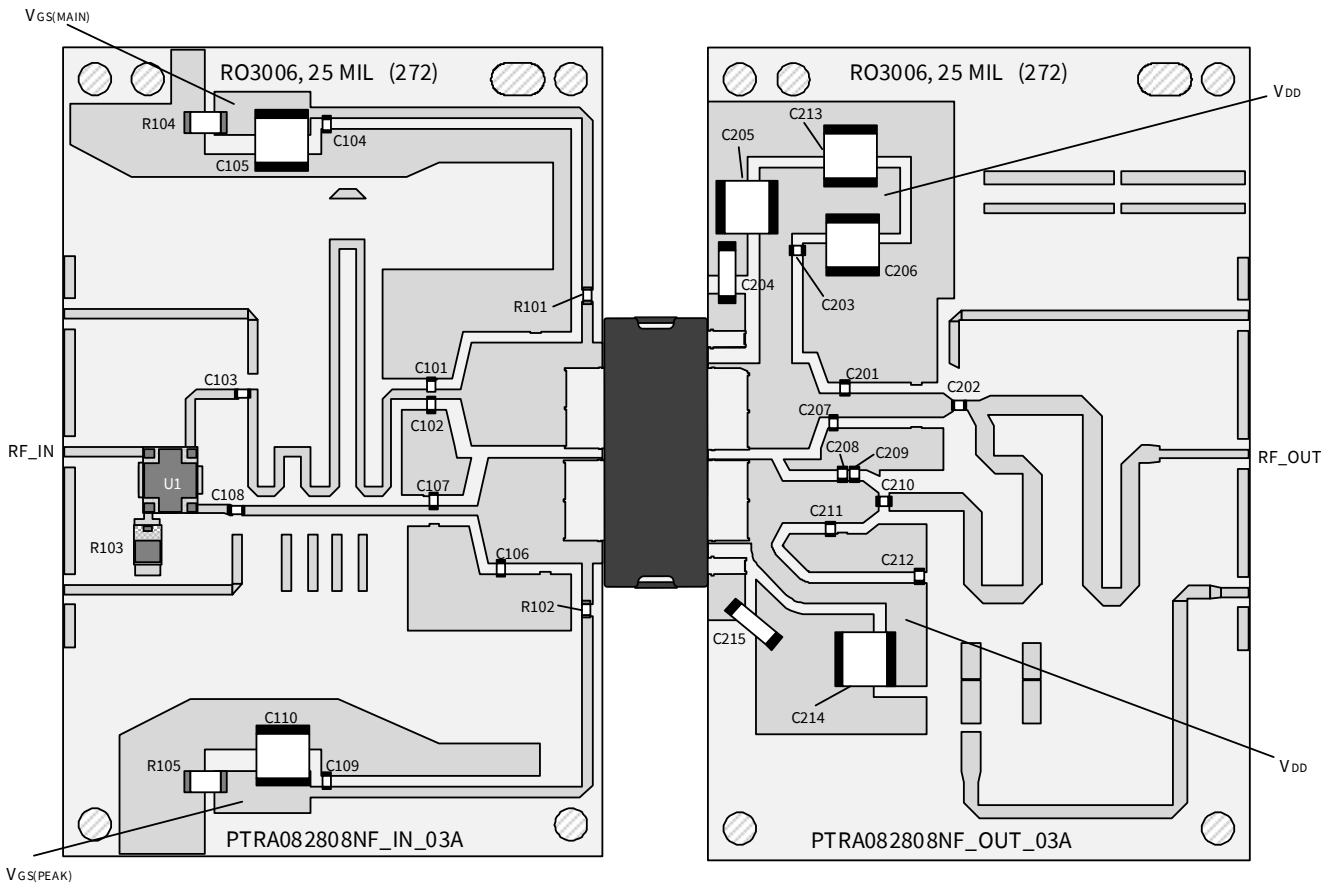
		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
790	1.8 – j4.4	2.6 – j1.9	18.3	52.53	179	62.7	5.5 + j0.2	20.27	50.63	116	71.2
805	1.8 – j5.2	2.8 – j2.6	18.3	52.29	169	60.2	5.6 + j0.0	20.18	50.61	115	71.2
820	1.8 – j5.2	2.9 – j3.1	18.4	52.24	168	60.0	5.6 + j1	20.45	50.13	103	71.3

Peak Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 350 mA

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{1dB} [dBm]	P_{1dB} [W]	ηD [%]
790	1.5 – j4.1	1.8 – j1.3	16.26	53.30	214	60.4	3.9 + j1.2	17.03	50.89	123	72.8
805	1.5 – j4.1	1.9 – j1.3	16.02	53.07	203	60.1	3.6 + j1.3	16.84	50.77	119	73.2
820	1.4 – j4.6	2.0 – j1.4	16.4	53.00	200	61.0	3.1 + j2.2	16.87	50.78	120	73.0

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Zl [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
790	1.5 – j4.1	2.0 – j1.4	14.37	54.07	255	65.3	3.6 – j0.1	15.05	52.54	180	73.9
805	1.5 – j4.1	2.0 – j2.3	14.84	53.86	243	60.5	3.7 + j1.2	14.84	51.42	139	73.8
820	1.4 – j4.6	2.1 – j1.5	14.43	53.77	238	64.0	3.6 + j0.7	15.13	51.83	152	73.6

Evaluation Board, 790 – 820 MHz



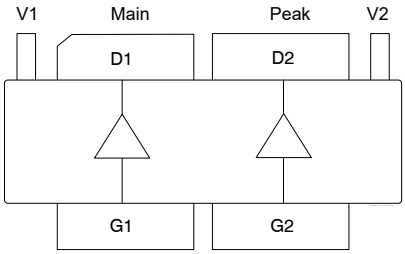
Reference circuit assembly diagram (not to scale)

Evaluation Board Part Number	LTA/PTRA082808NF-V1
PCB Information	Rogers 3006, 0.635 mm [0.025”] thick, 2 oz. copper, ε_r = 3.66, f = 790 – 820 MHz

Components Information

Component	Description	Manufacturer	P/N
Input			
C101, C102	Capacitor, 5.6 pF	ATC	ATC800A5R6CT250T
C103, C104, C108, C109	Capacitor, 56 pF	ATC	ATC800A560JT250T
C105, C110	Capacitor, 10 µF	TDK Corporation	C5750X5R1H106K230KA
C106	Capacitor, 10 pF	ATC	ATC800A100JT250T
C107	Capacitor, 1.5 pF	ATC	ATC800A1R5CT250T
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R103	Resistor, 50 ohms	Anaren	C8A50Z4A
R104, R105	Resistor, 1000 ohms	Panasonic Electronic Components	ERJ-8GEYJ102V
U1	Hybrid Coupler	Anaren	X3C07P1-05S
Output			
C201	Capacitor, 3.0 pF	ATC	ATC800A3R0CT250T
C202	Capacitor, 15 pF	ATC	ATC800A150JT250T
C203, C210, C212	Capacitor, 82 pF	ATC	ATC800A820JT250T
C204, C205, C206, C213, C214, C215	Capacitor, 10 µF , 100V	TDK Corporation	C5750X7S2A106M230KB
C207	Capacitor, 6.8 pF	ATC	ATC800A6R8CT250T
C208	Capacitor, 3.9 pF	ATC	ATC800A3R9CT250T
C209	Capacitor, 2.2 pF	ATC	ATC800A2R2CT250T
C211	Capacitor, 10 pF	ATC	ATC800A100JT250T

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1 (Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1, V2	Drain video decoupling, no DC bias

Package Outline Specifications – Package PG-HBSOF-6-2 (top view)

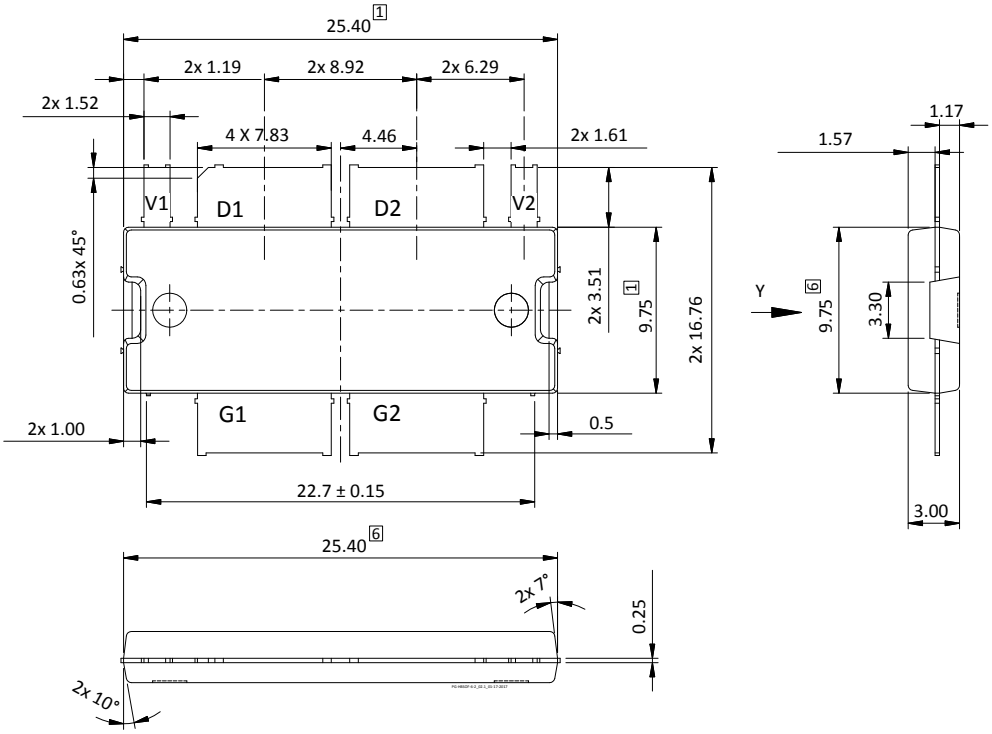
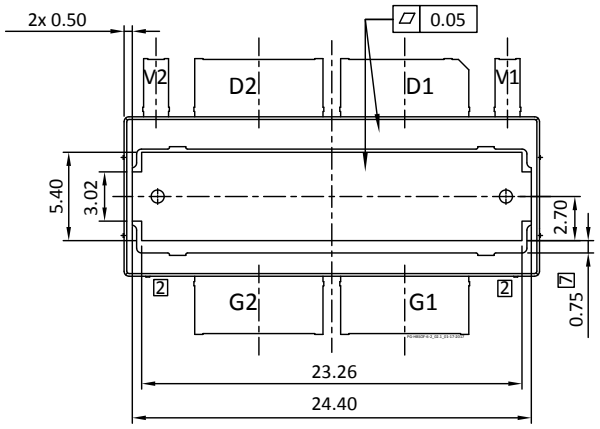


Diagram Notes—unless otherwise specified:

1. Mold/dam bar/metal protrusion of 0.30 mm max per side not included.
2. Metal protrusions are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Does not include mold/dam bar and metal protrusion.
7. Exposed metal surface is tin-plated, may not be covered by mold compound.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces are tin-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D1, D2 = drain; G1, G2 = gate; V1, V2 = drain video decoupling, no DC bias

Package Outline Specifications (cont.) **– Package PG-HBSOF-6-2** (bottom view)



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