ISL8011xEVAL1Z Evaluation Board User Guide

Description

The ISL8011xEVAL1Z provides a simple platform to evaluate performance of the ISL8011x family of split supply LDOs. Jumpers are provided to easily set popular output voltages.

The ISL80111, ISL80112 and ISL80113 are single-output LDOs specified for 1A, 2A, 3A of output current and are optimized for less than 2.5V and less output voltage conversions. The ISL8011x supports V_{IN} voltages down to 1V, provided a standard legacy 2.9V or 5.5V is applied on the V_{BIAS} pin. The output voltage is adjustable from 0.8V to 3.3V.

Specifications

This board has been configured and optimized for the following operating conditions:

- V_{IN} range of 1V to 3.6V
- V_{OUT} adjustable from 0.8V to 3.3V
- Convenient power connection
- Popular output voltages can easily set by jumpers

Key Features

- Ultra low dropout: 75mV at 3A, (typ)
- Excellent V_{IN} PSRR: 70dB at 1kHz (typ)
- ±1.6% guaranteed V_{OUT} accuracy for -40°C < T_J < +125°C
- Very fast load transient response

References

ISL80111, ISL80112, ISL80113 Datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL80111EVAL1Z	1A, Split Supply LDO Evaluation Board
ISL80112EVAL1Z	2A, Split Supply LDO Evaluation Board
ISL80113EVAL1Z	3A, Split Supply LDO Evaluation Board

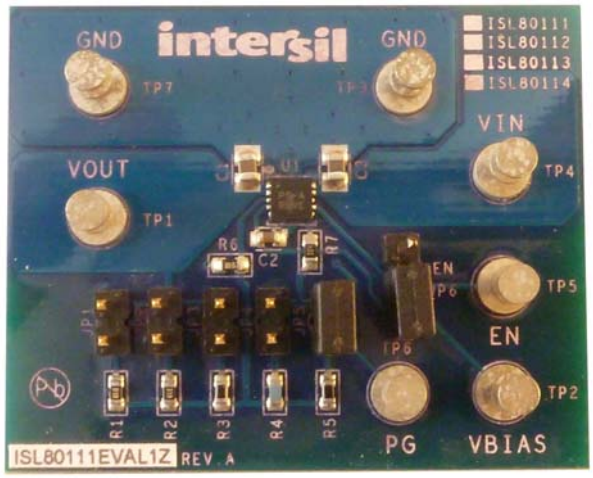


FIGURE 1. ISL80111EVAL1Z TOP SIDE

FIGURE 2. ISL80111EVAL1Z BOTTOM SIDE

What's Inside

The evaluation kit contains the following:

- The ISL80113EVAL1Z with the appropriate parts installed
- ISL80111, ISL80112, ISL80113 Datasheet

Test Steps

1. Select the desired output voltage by shorting one of the jumpers from JP2 through JP5.
2. Connect both the BIAS and VIN supplies and the load. Enable the IC using jumper JP6 (bottom position) or via a signal on the center post, observe the output.
3. The shipped configuration is enabled and V_{OUT} = 3.3V.
4. Scope shots taken from ISL8011xEVAL1Z boards.

Functional Description

The ISL8011xEVAL1Z provides a simple platform to evaluate performance of the ISL8011x family of split supply LDOs. Jumpers are provided to easily set popular output voltages.

The ISL80111, ISL80112 and ISL80113 are single-output LDOs specified for 1A, 2A, 3A of output current and are optimized for less than 2.5V and less output voltage conversions. The ISL8011X supports V_{IN} voltages down to 1V, provided a standard legacy 2.9V or 5.5V is applied on the V_{BIAS} pin. The output voltage is adjustable from 0.8V to 3.3V.

An enable input, having a threshold <1V, allows the part to be placed into a low quiescent current shutdown mode. A submicron CMOS process is utilized for this product family to deliver best-in-class analog performance and overall value for applications in need of input voltage conversions to typically below 2.5V. It also has the superior load transient regulation unique to a NMOS power stage.

These LDOs consume significantly lower quiescent current as a function of load compared to bipolar LDOs. This lower consumption translates into higher efficiency and the ability to consider packages with smaller footprints. The quiescent current has been modestly compromised in design to enable leading class fast load transient response and load regulation.

PCB Layout Guidelines

The following is an example of how to use vias to remove heat from the IC.

Filling the thermal pad area with vias is recommended. A typical via array is to fill the thermal pad footprint with vias spaced such that they are center on center 3x the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow.

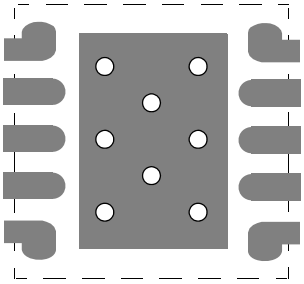
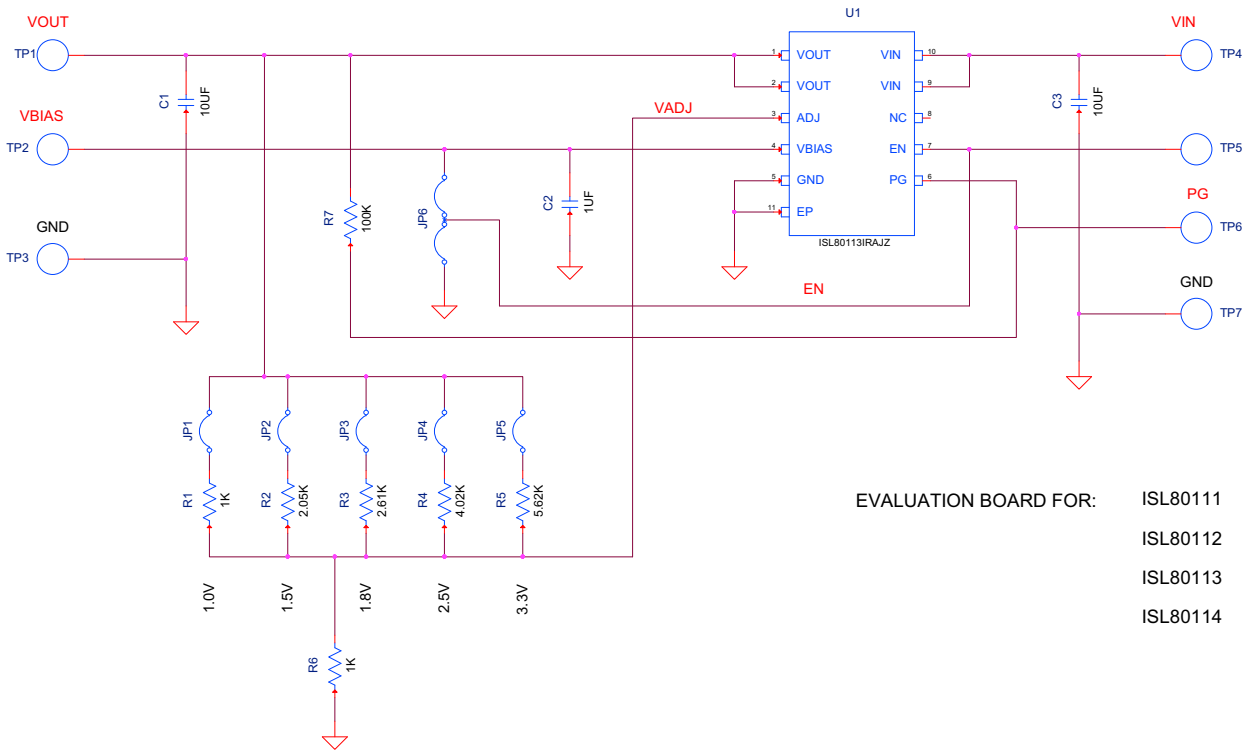


FIGURE 3. PCB VIA PATTERN

Connect all vias to the round plane. For efficient heat transfer, it is important that the vias have low thermal resistance. Do not use "thermal relief" patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane.

Schematic



Bill of Materials

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURER	PART NUMBER
U1		ISL80111, ISL80112 or ISL80113 as noted on the evaluation board	Intersil	ISL80111IRAJZ, ISL80112IRAJZ, ISL80113IRAJZ
C1, C3	10µF	CAP, SMD, 0805, 50V, 10%	Generic	
C2	1µF	CAP, SMD, 0603	Generic	
R1	1kΩ	RES, SMD, 0603, 1%	Generic	
R2	2.05kΩ	RES, SMD, 0603, 1%	Generic	
R3	2.61kΩ	RES, SMD, 0603, 1%	Generic	
R4	4.02kΩ	RES, SMD, 0603, 1%	Generic	
R5	5.62kΩ	RES, SMD, 0603, 1%	Generic	
R6	1kΩ	RES, SMD, 0603, 1%	Generic	
R7	100kΩ	RES, SMD, 0603, 1%	Generic	
JP1, JP2, JP3, JP4, JP5, JP6		Jumper	Generic	
TP1, TP2, TP3 TP4, TP5, TP6		Terminal Connector	Generic	

Board Layout

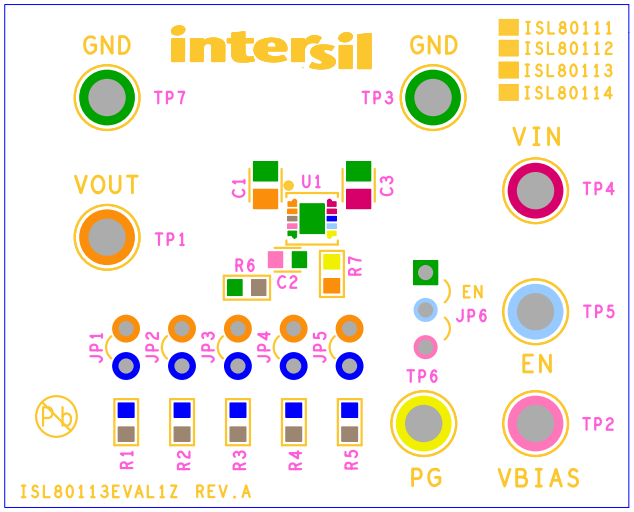


FIGURE 4. SILKSCREEN TOP

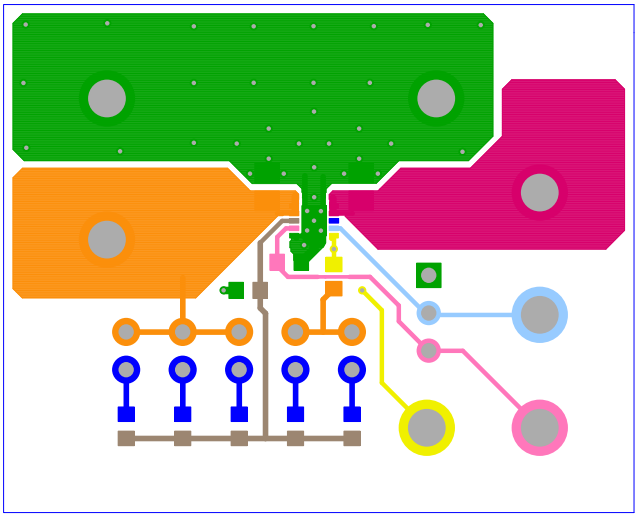


FIGURE 5. TOP LAYER COMPONENT SIDE

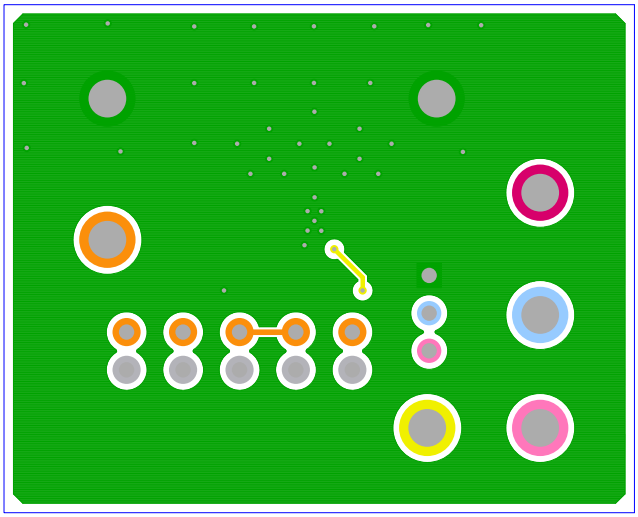


FIGURE 6. BOTTOM LAYER SOLDER SIDE

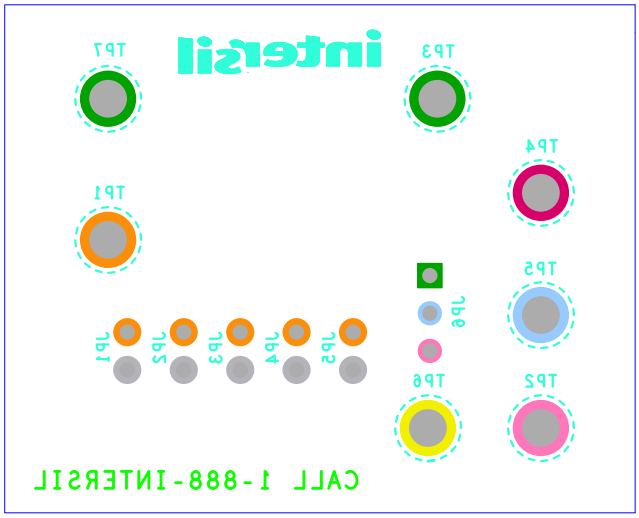


FIGURE 7. SILKSCREEN BOTTOM

Typical Performance Curves

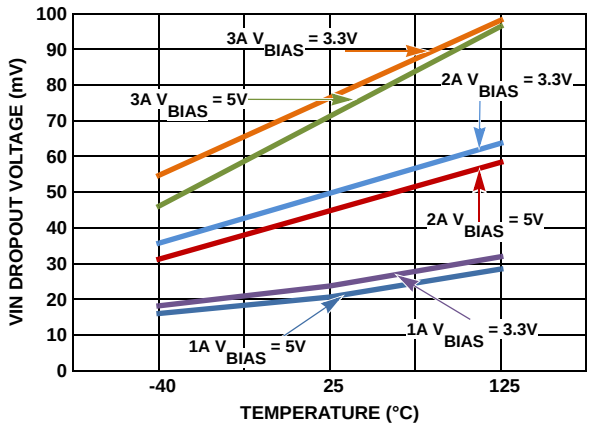


FIGURE 8. DROPOUT vs V_{BIAS}

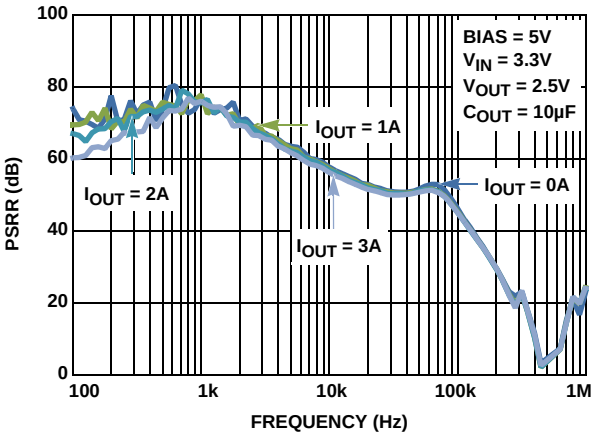


FIGURE 9. V_{IN} PSRR vs LOAD CURRENT

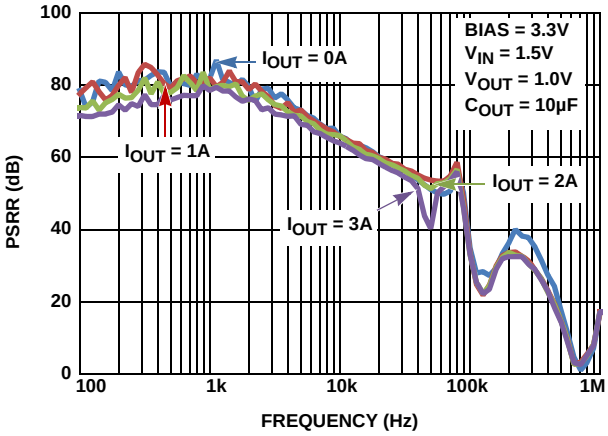


FIGURE 10. V_{VIN} PSRR vs LOAD CURRENT

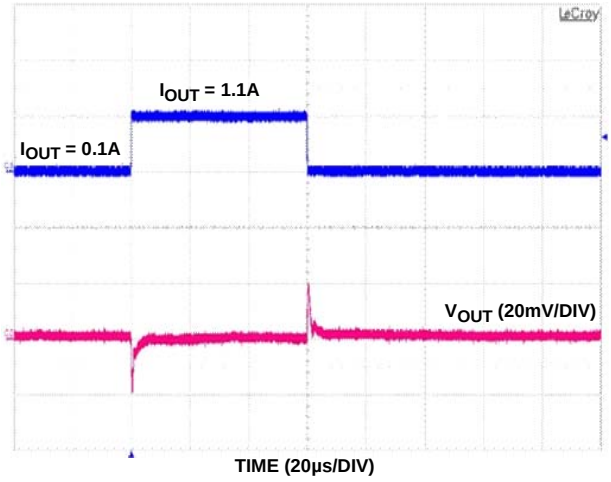


FIGURE 11. 1A LOAD TRANSIENT RESPONSE

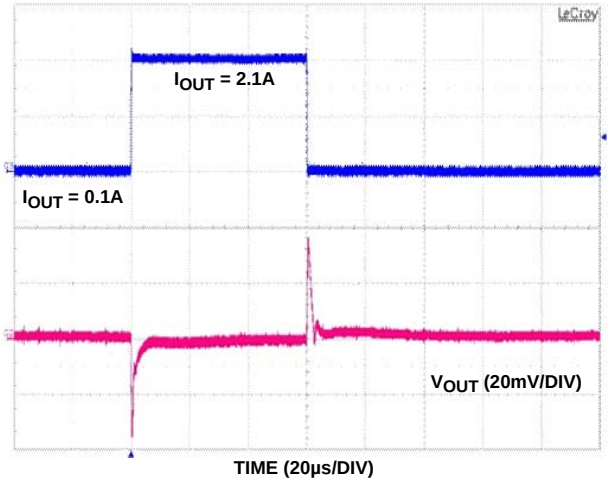


FIGURE 12. 2A LOAD TRANSIENT RESPONSE

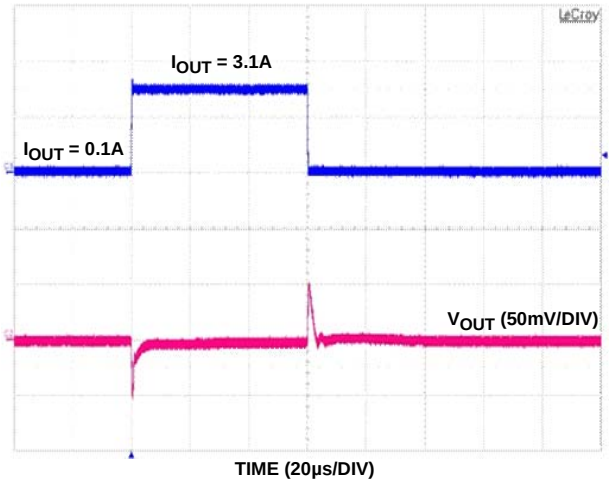


FIGURE 13. 3A LOAD TRANSIENT RESPONSE