

100V N-Channel Enhancement Mode MOSFET

Voltage	100 V	R_{DS(ON)}	4.2 mΩ
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Current	109 A	Q_G (TYP)	58 nC
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Feature

- $R_{DS(ON)} < 4.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- $R_{DS(ON)} < 6.0 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 25 \text{ A}$
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard
- 100% UIS / Rg test in mass production

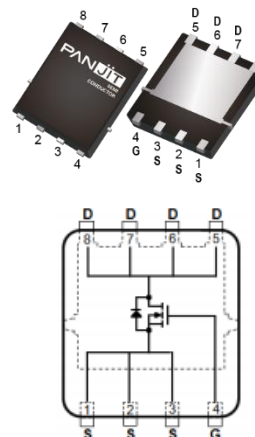
Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 94 mg

Application

- PD Charger / Adapter / Home Appliance / DC-DC converter.

DFN5060-8L



Top side view

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (Note 3)	$T_C = 25^\circ\text{C}$	I_D	109	A
	$T_C = 100^\circ\text{C}$		77	
Pulsed Drain Current	$T_C = 25^\circ\text{C}$	I_{DM}	448	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	35	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	192	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	115	W
	$T_C = 100^\circ\text{C}$		57	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~175	$^\circ\text{C}$

Thermal Characteristics

PARAMETER		SYMBOL	VALUES			UNITS
			MIN.	TYP.	MAX.	
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	-	0.9	1.3	$^\circ\text{C/W}$
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	-	-	50	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0 V, I _D =250 μA	100	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =270 μA	1.1	1.7	2.3	
Drain-Source On-State Resistance (Note 1)	R _{DS(on)}	V _{GS} =10 V, I _D =50 A	-	3.6	4.2	mΩ
		V _{GS} =4.5 V, I _D =25 A	-	4.6	6.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100 V, V _{GS} =0 V	-	-	1	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20 V, V _{DS} =0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g _{fs}	V _{DS} =10 V, I _D =50 A	-	123	-	S
Dynamic Characteristics (Note 6)						
Total Gate Charge	Q _g	V _{DS} =50 V, I _D =50 A, V _{GS} =4.5 V	-	27	-	nC
Gate-Source Charge	Q _{gs}	V _{DS} =50 V, I _D =50 A, V _{GS} =10 V	-	58	76	nC
Gate-Drain Charge	Q _{gd}		-	12.2	-	
Gate Plateau Voltage	V _{plateau}		-	7.2	-	
Input Capacitance	C _{iss}	V _{DS} =50 V, V _{GS} =0 V, f=250 kHz	-	3.0	-	V
Output Capacitance	C _{oss}		-	3800	4940	pF
Reverse Transfer Capacitance	C _{rss}		-	1050	1365	
Output Charge	Q _{oss}	V _{DS} =50 V, V _{GS} =0 V	-	16	-	
Turn-On Delay Time	t _{d(on)}	V _{DD} =50 V, I _D =50 A, V _{GS} =10 V, R _G =3.0 Ω (Note 2)	-	75	98	nC
Rise Time	t _r		-	9.6	-	ns
Turn-Off Delay Time	t _{d(off)}		-	6.2	-	
Fall Time	t _f		-	31	-	
Gate Resistance	R _g	f =1.0 MHz	-	4.8	-	Ω
Drain-Source Diode						
Diode Forward Voltage	V _{SD}	I _S =50 A, V _{GS} =0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q _{rr}	I _F =50 A, V _{DD} =50 V,	-	70	-	nC
Reverse Recovery Time	T _{rr}	di/dt=100 A/μs	-	61	-	ns

NOTES :

- Pulse width ≤ 300 μs, Duty cycle ≤ 2 %
- Essentially independent of operating temperature typical characteristics.
- The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
- E_{AS} is calculated based on the condition of L = 1.0 mH, I_{AS} = 19.6 A, V_{DD} = 50 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 35 A in production.
- Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

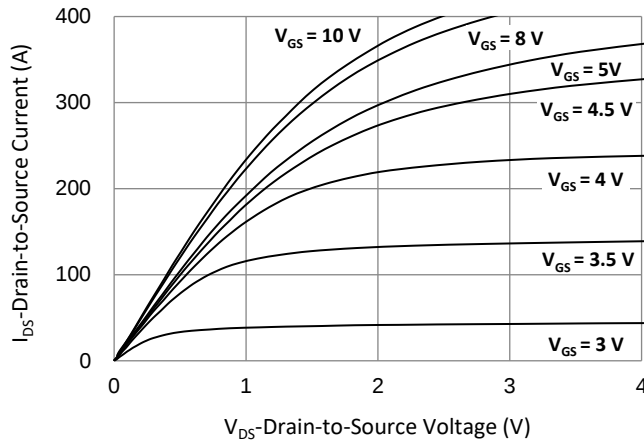


Fig.1 Output Characteristics

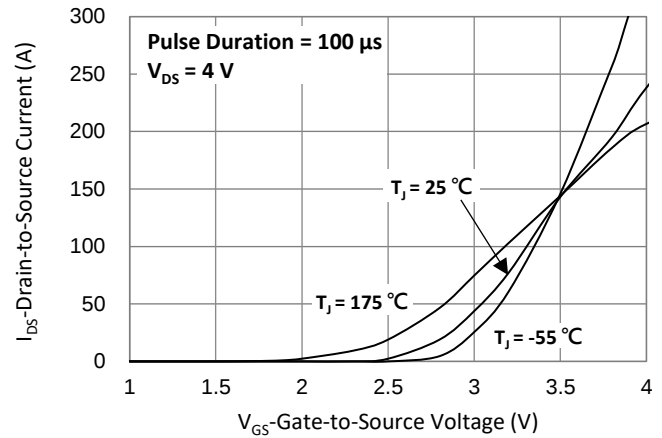


Fig.2 Transfer Characteristics

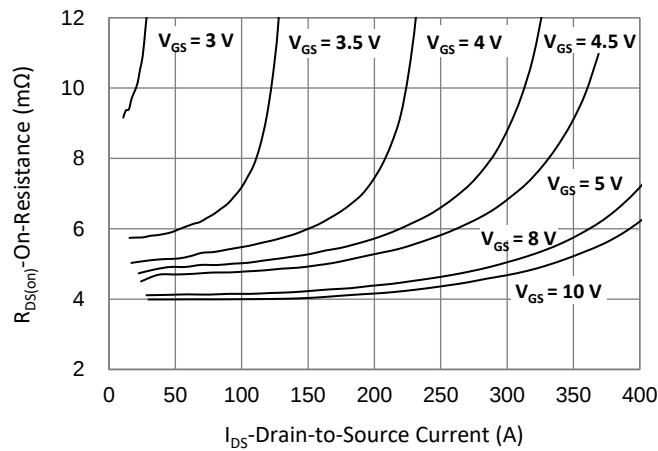


Fig.3 On-Resistance vs. Drain Current

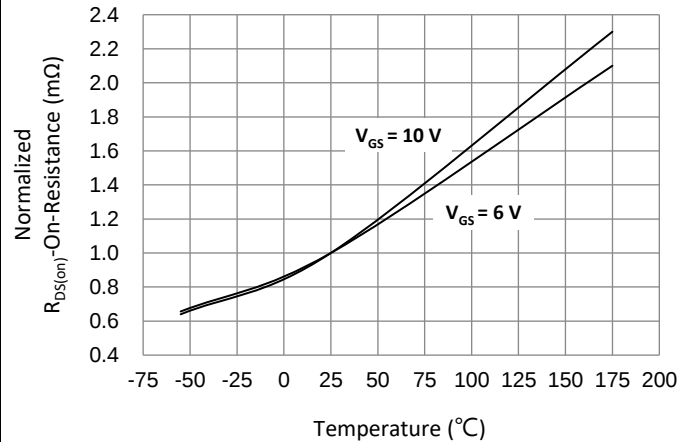


Fig.4 On-Resistance vs. Junction temperature

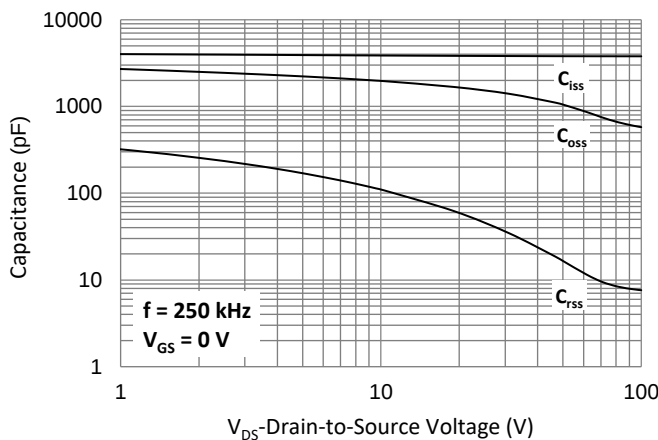


Fig.5 Capacitance vs. Drain-Source Voltage

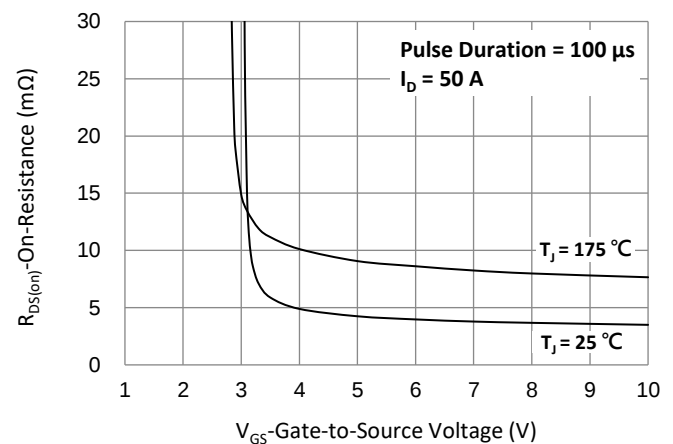
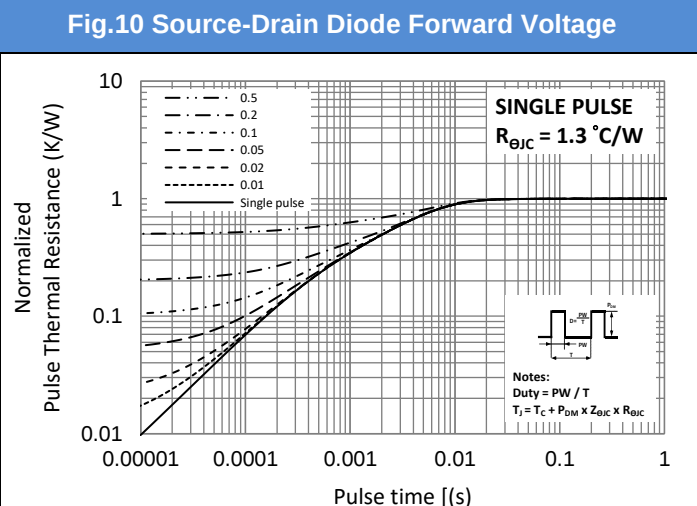
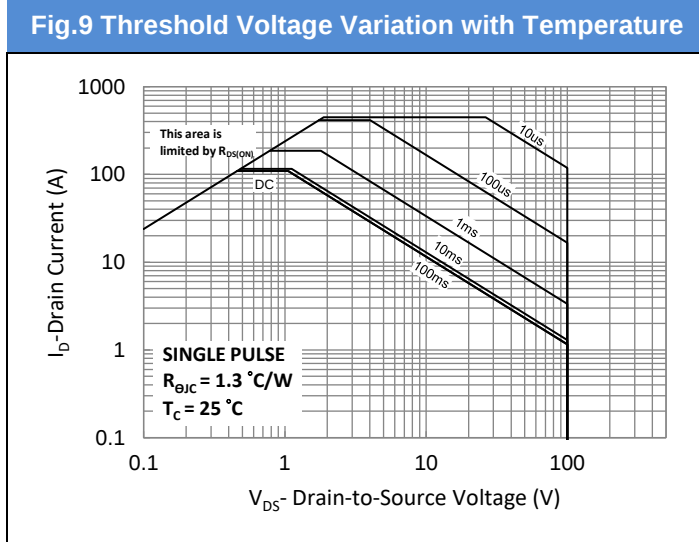
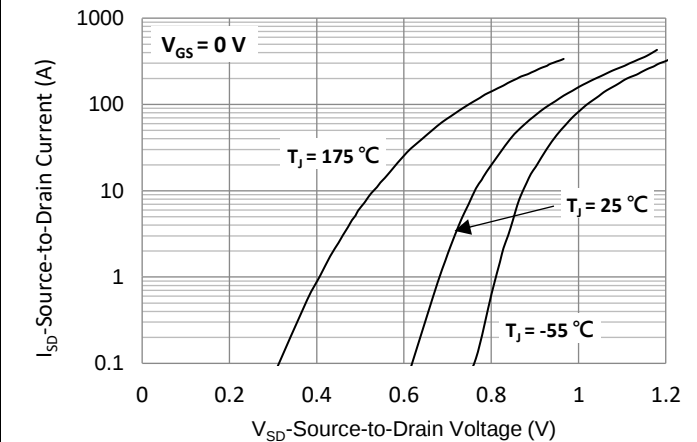
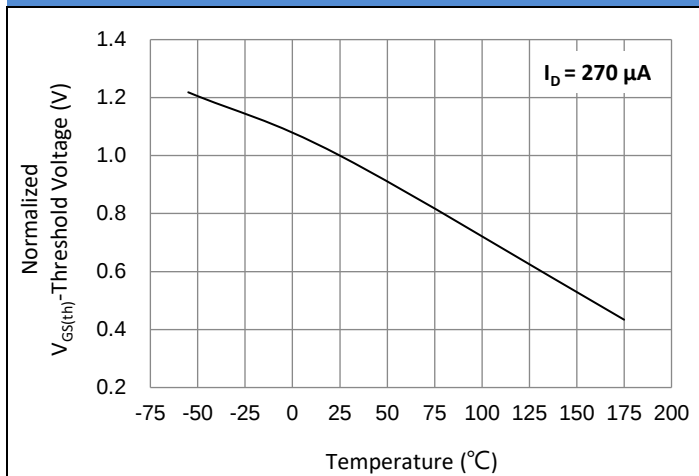
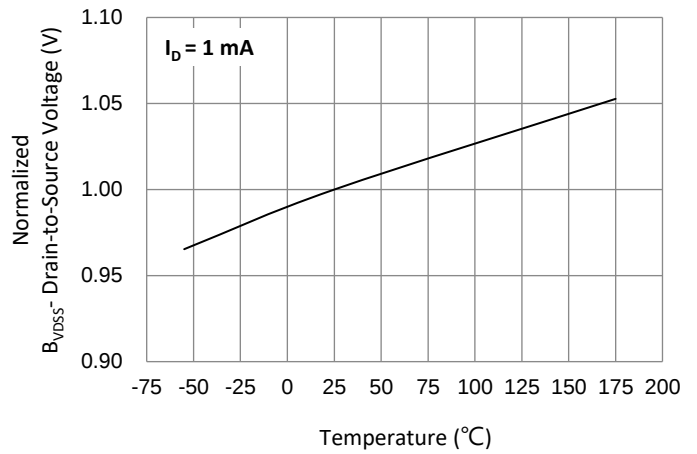
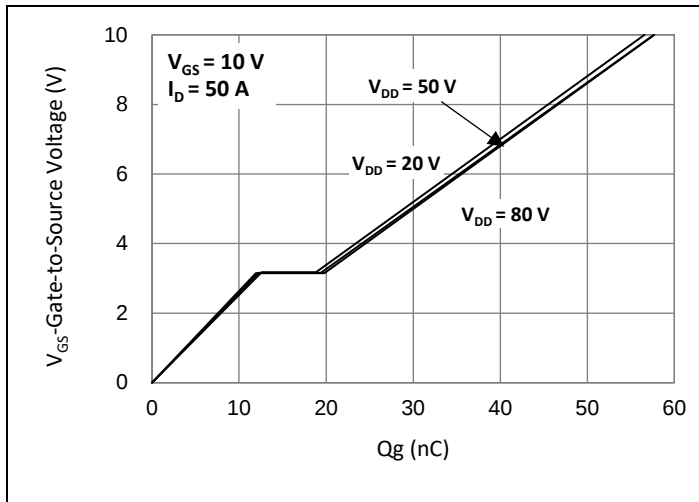


Fig.6 On-Resistance vs. Gate-Source Voltage

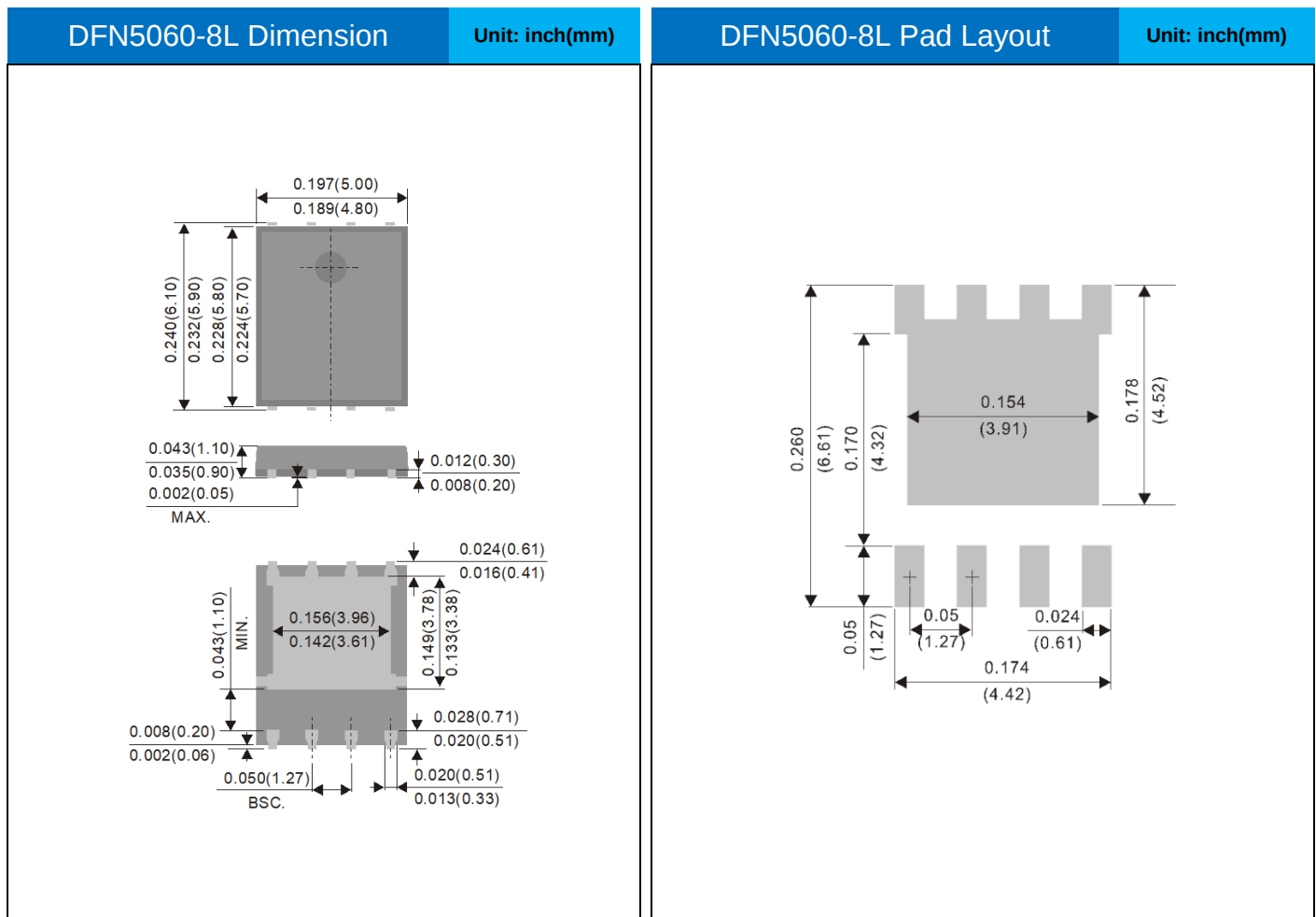
TYPICAL CHARACTERISTIC CURVES



Product and Packing Information

Part No.	Package Type	Packing Type	Marking
PSMQC042N10LS2	DFN5060-8L	3000pcs / 13" reel	042N10LS

Packaging Information & Mounting Pad Layout



Marking Diagram

PJ	Y	= Year Code
042N10LS	W	= Week Code (A~Z)
YWLL x	LL	= Lot Code (00~99)
	x	= Production Line Code

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