

April 2014

Features

Inputs/Outputs

- Accepts two differential or single-ended inputs
 - LVPECL, LVDS, CML, HCSL, LVCMOS
 - Glitch-free switching of references
- Eight precision LVPECL outputs
- Operating frequency up to 750 MHz

Power

- Options for 2.5 V or 3.3 V power supply
- Core current consumption of 122 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

Performance

- Ultra low additive jitter of 121 fs RMS

Ordering Information

| | | |
|------------------------|------------|----------------------------|
| ZL40210LDG1 | 32 Pin QFN | Trays |
| ZL40210LDF1 | 32 Pin QFN | Tape and Reel Matte Tin |
| Package size: 5 x 5 mm | | |
| -40°C to +85°C | | |

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Redundant clock distribution
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3 clock distribution
- Wireless communications
- High performance microprocessor clock distribution

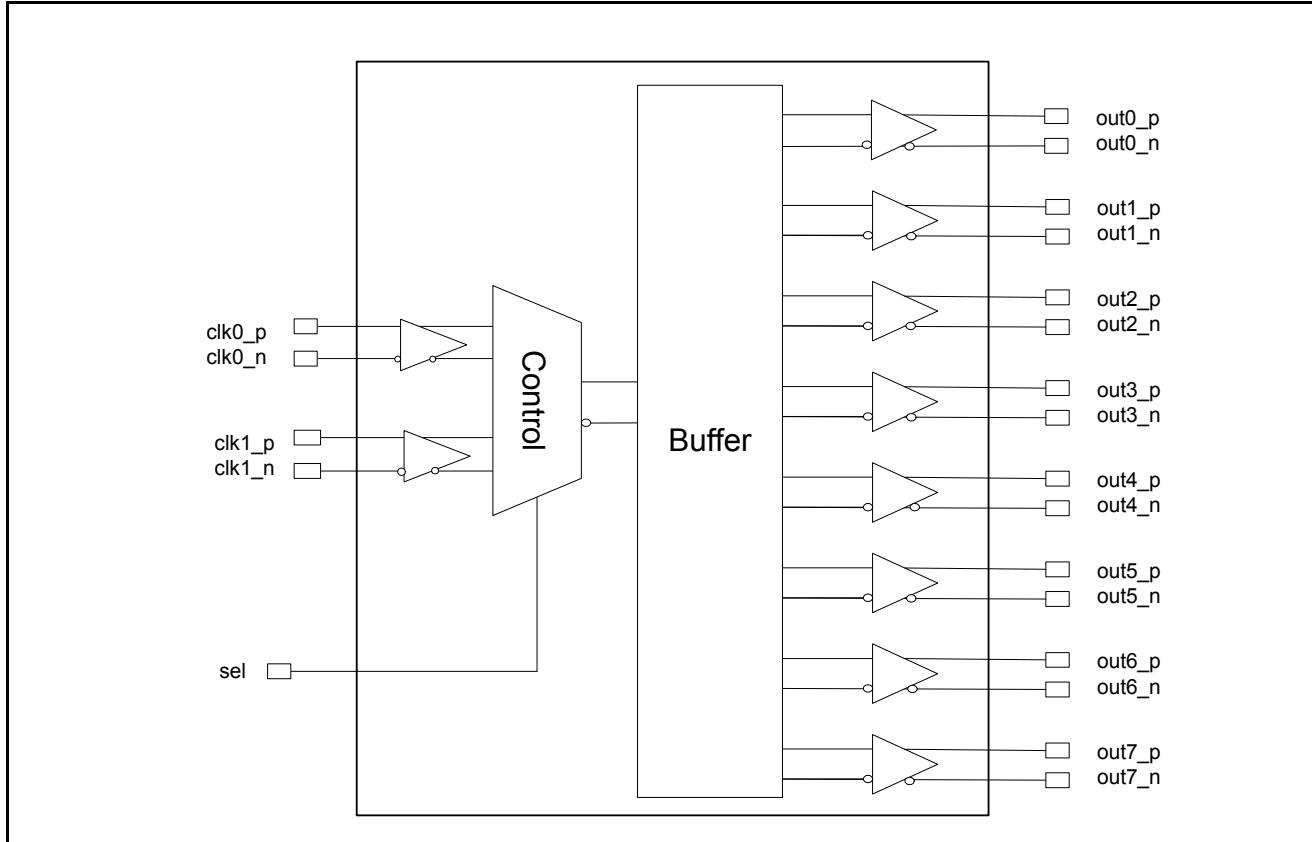


Figure 1 - Functional Block Diagram

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Change Summary

Below are the changes from the February 2013 issue to the April 2014 issue:

| Page | Item | Change |
|------|-----------------------|--|
| 1 | Applications | Added PCI Express clock distribution. |
| 6 | Pin Description | Added exposed pad to Pin Description. |
| 8 | Figure 4 and Figure 5 | Removed 22 ohm series resistors from Figure 4 and 5. These resistors are not required; however, there is no impact to performance if the resistors are included. |
| 15 | Figure 17 | Corrected LVPECL interface circuit. |
| 20 | Figure 22 | Clarification of V_{ID} and V_{OD} . |

Below are the changes from the November 2012 issue to the February 2013 issue:

| Page | Item | Change |
|------|----------|---|
| 8 | Figure 5 | Changed text to indicate the circuit is not recommended for $V_{DD_driver}=2.5V$. |
| 9 | Figure 6 | Changed pull-up and pull-down resistors from 2kOhm to 100Ohm. |

1.0 Package Description

The device is packaged in a 32 pin QFN

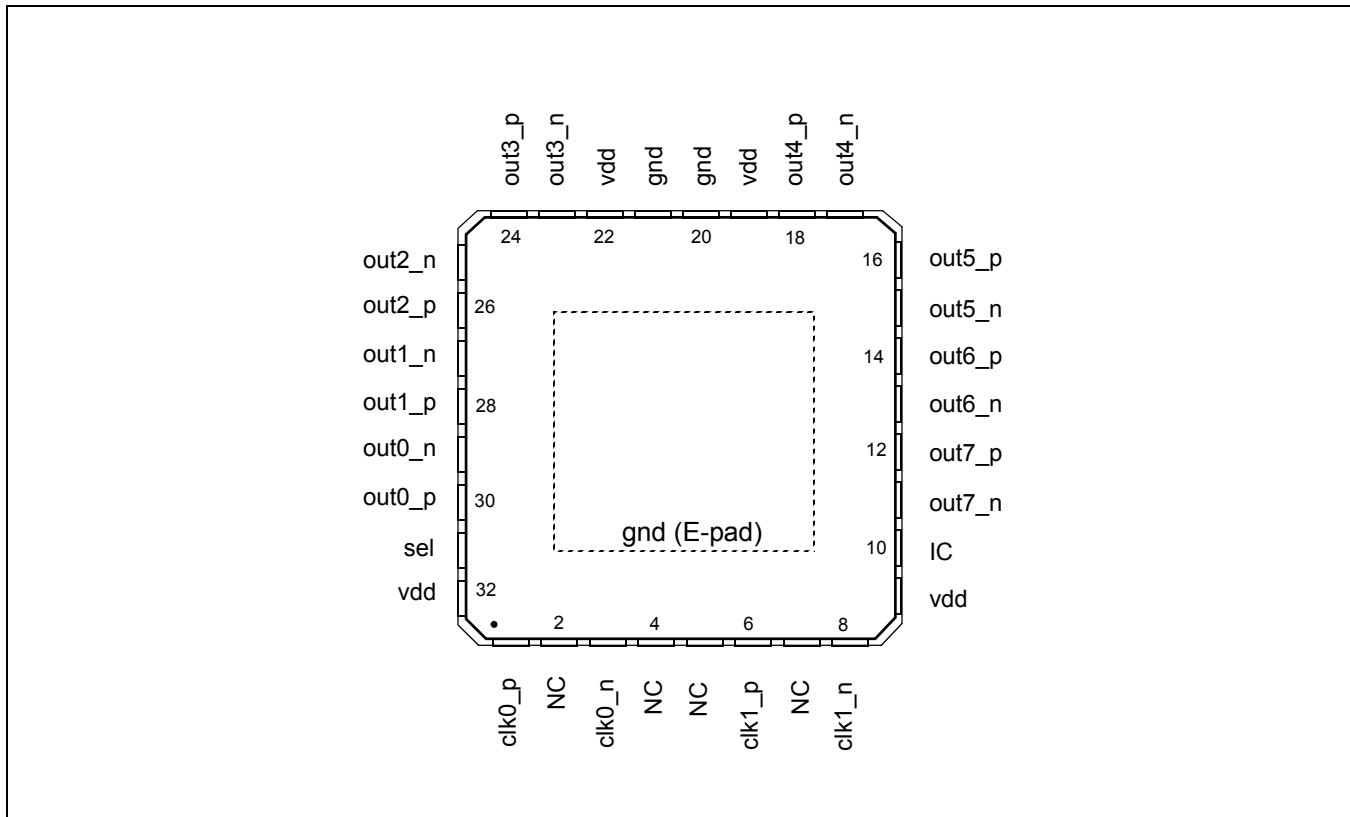


Figure 2 - Pin Connections

2.0 Pin Description

| Pin # | Name | Description |
|---|--|---|
| 1,3, 6, 8 | clk0_p, clk0_n, clk1_p, clk1_n | Differential Input (Analog Input). Differential (or singled ended) input signals. For all input signal configuration see Section 3.1, “Clock Input“. |
| 30, 29, 28, 27, 26, 25, 24, 23, 18, 17, 16, 15, 14, 13, 12, 11 | out0_p, out0_n out1_p, out1_n out2_p, out2_n out3_p, out3_n out4_p, out4_n out5_p, out5_n out6_p, out6_n out7_p, out7_n | Differential Output (Analog Output). Differential outputs. |
| 9, 19, 22, 32 | vdd | Positive Supply Voltage. 2.5V _{DC} or 3.3 V _{DC} nominal. |
| 20, 21 | gnd | Ground. 0 V. |
| 31 | sel | Input Select (Input). Selects the reference input that is buffered; 0: clk0 1: clk1 This pin is internally pulled down to GND. |
| 2, 4, 5, 7, 10 | NC | No Connection. Leave unconnected. |
| Exposed Pad | | Device GND. |

3.0 Functional Description

The ZL40210 is an LVPECL clock fanout buffer with eight output clock drivers capable of operating at frequencies up to 750MHz.

The ZL40210 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

3.1 Clock Input

Inputs to the ZL40210 are externally terminated to allow use of precision termination components and to allow full flexibility of input termination. The ZL40210 can accept DC coupled LVPECL or LVDS and AC coupled LVPECL, LVDS, CML or HCSL input signals; single ended input signals can also be accepted. A pin compatible device with internal termination is also available.

3.1.1 Clock Input Selection

The select line chooses which input clock is routed to the outputs.

| Sel | Active Input |
|-----|--------------|
| 0 | clk0 |
| 1 | clk1 |

Table 1 - Input Selection

The following figure shows the expected clock switching performance. The output stops at the first falling edge of the initial clock after the select pin changes state. During switching there will be a short time when the output clock is not toggling. After this delay, the output will start toggling again with a rising edge of the newly selected clock. This behavior is independent of the frequencies of the input clocks. For instance, the two clocks could be at different frequencies and the behavior would still be consistent with this figure.

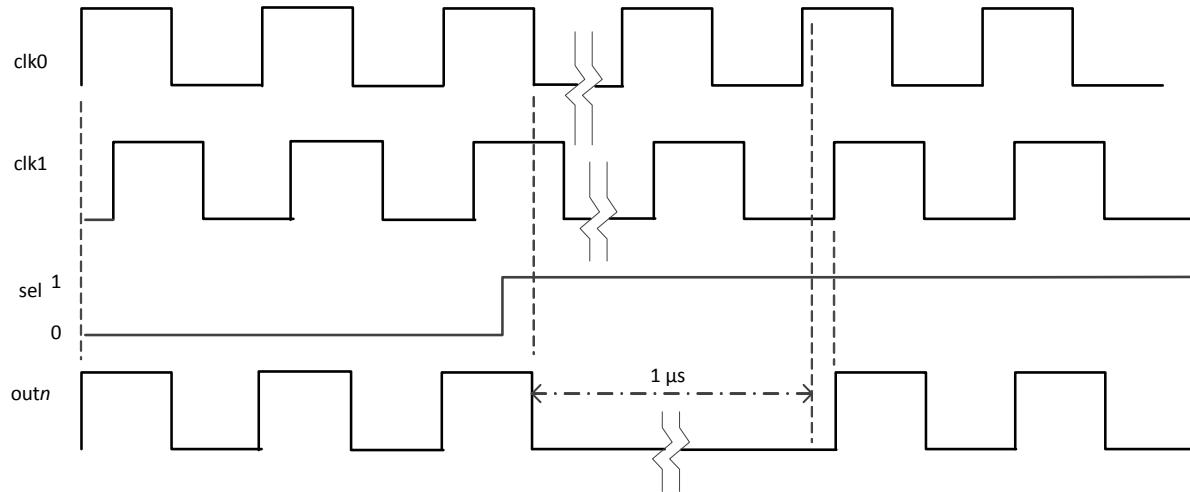


Figure 3 - Output During Clock Switch - Both Clocks Running

3.1.2 Clock Input Termination

The ZL40210 is adaptable to support different types of differential and singled-ended input signals depending on the passive components used in the input termination. The application diagrams in the following figures allow the ZL40210 to accept LVPECL, LVDS, CML, HCSL and single-ended inputs.

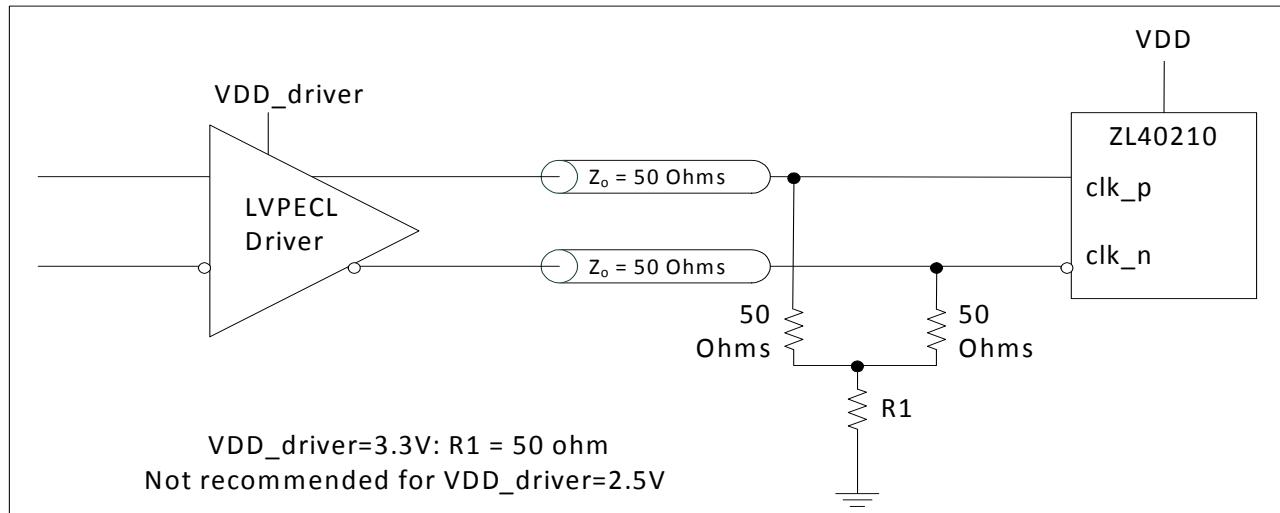


Figure 4 - LVPECL Input DC Coupled Thevenin Equivalent

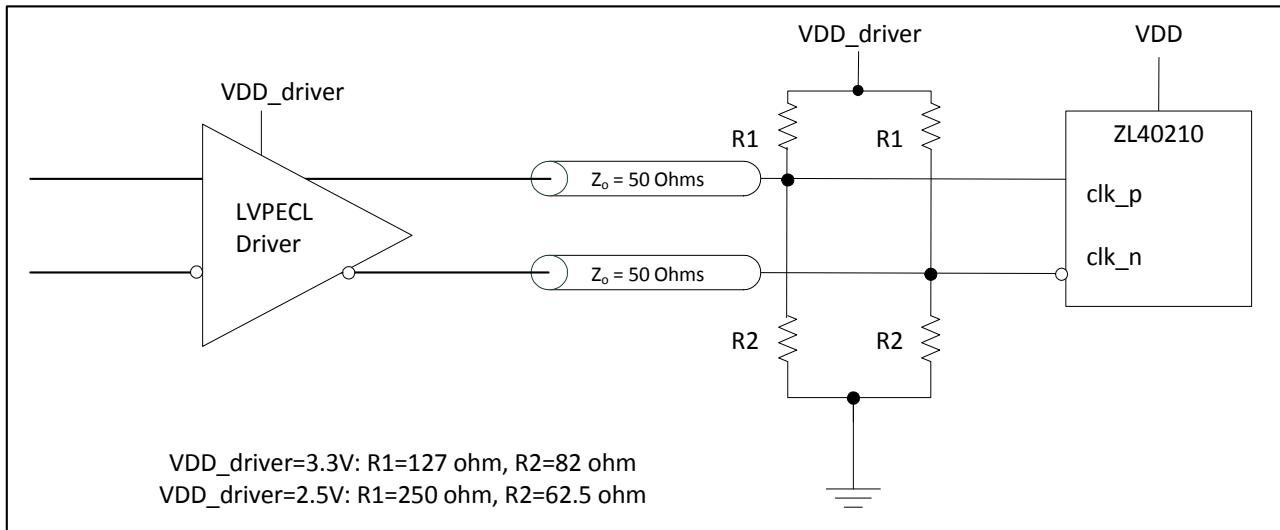


Figure 5 - LVPECL Input DC Coupled Parallel Termination

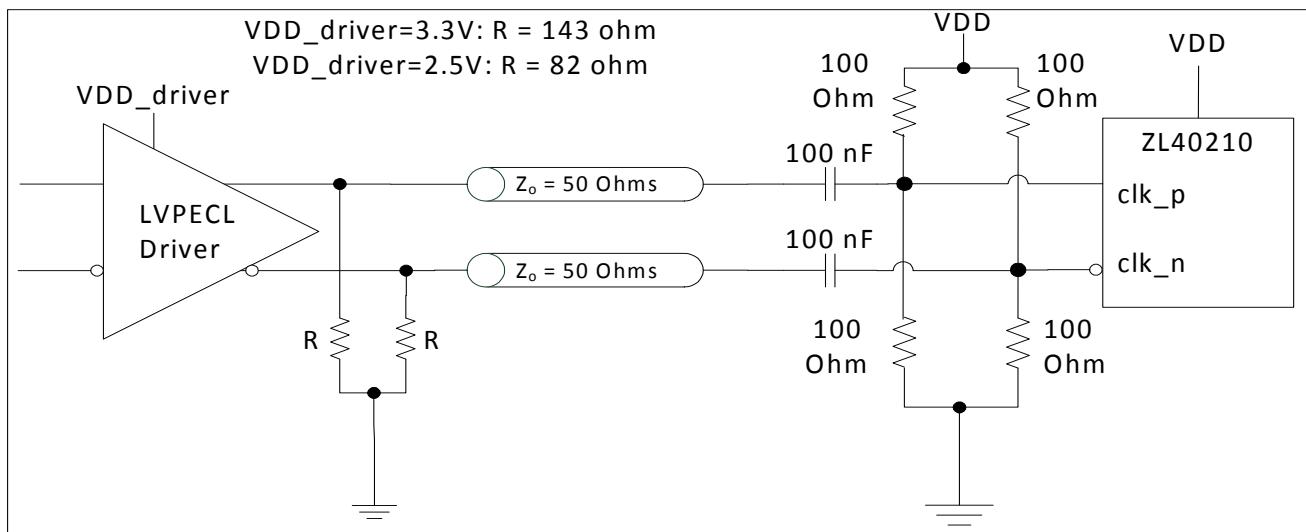


Figure 6 - LVPECL Input AC Coupled Termination

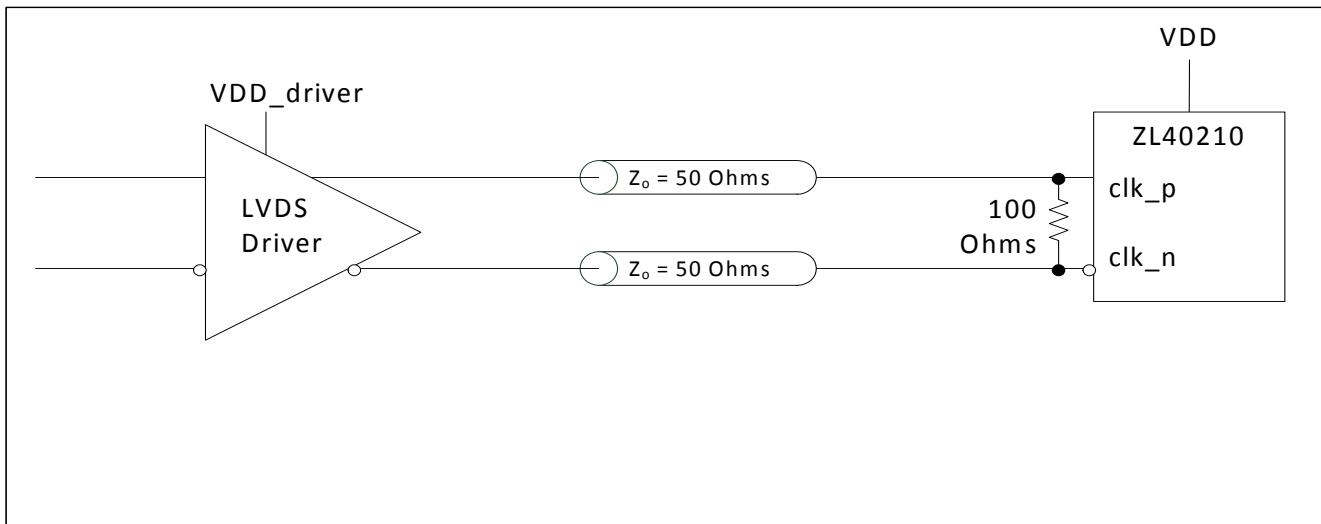


Figure 7 - LVDS Input DC Coupled

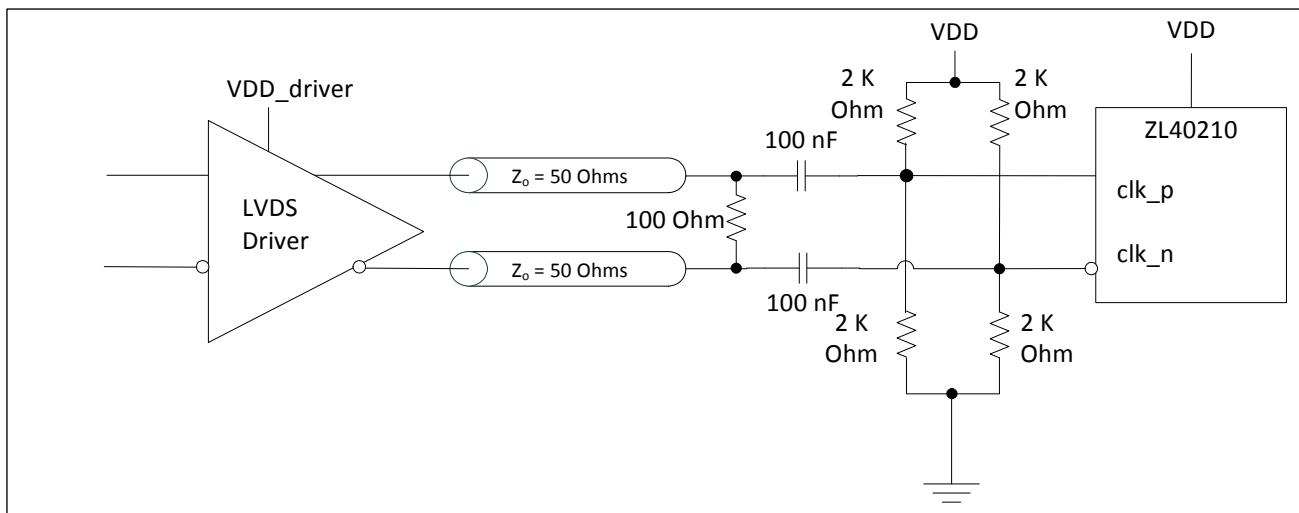


Figure 8 - LVDS Input AC Coupled

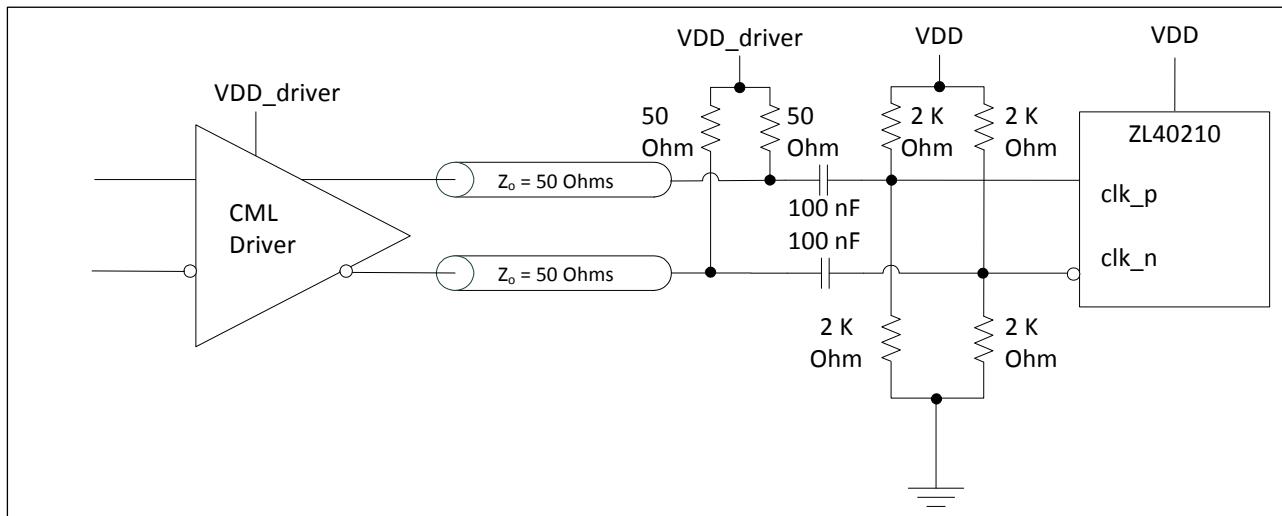


Figure 9 - CML Input AC Coupled

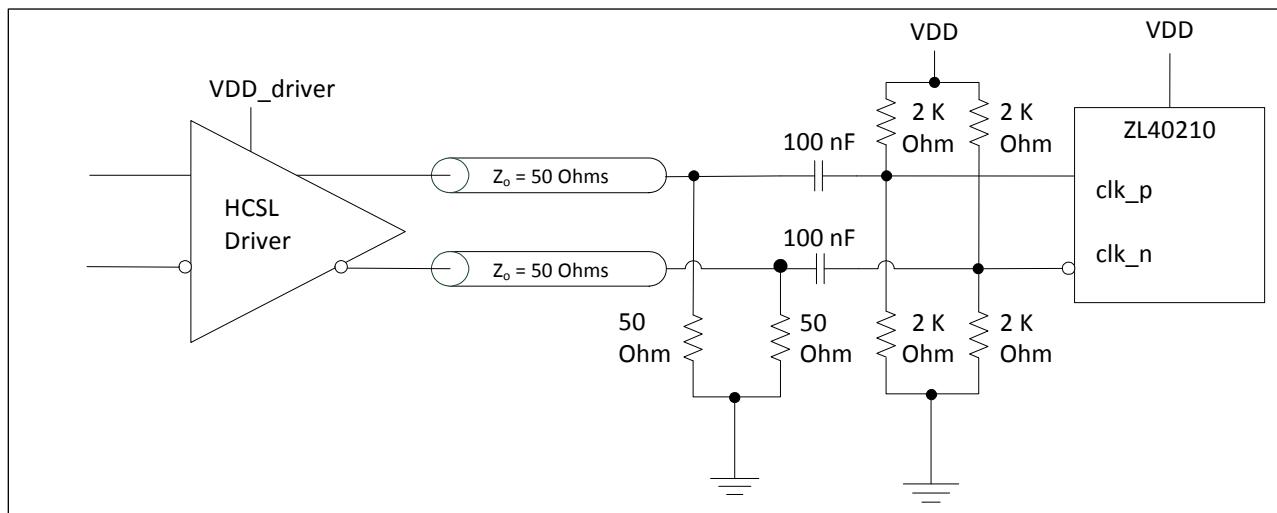


Figure 10 - HCSL Input AC Coupled

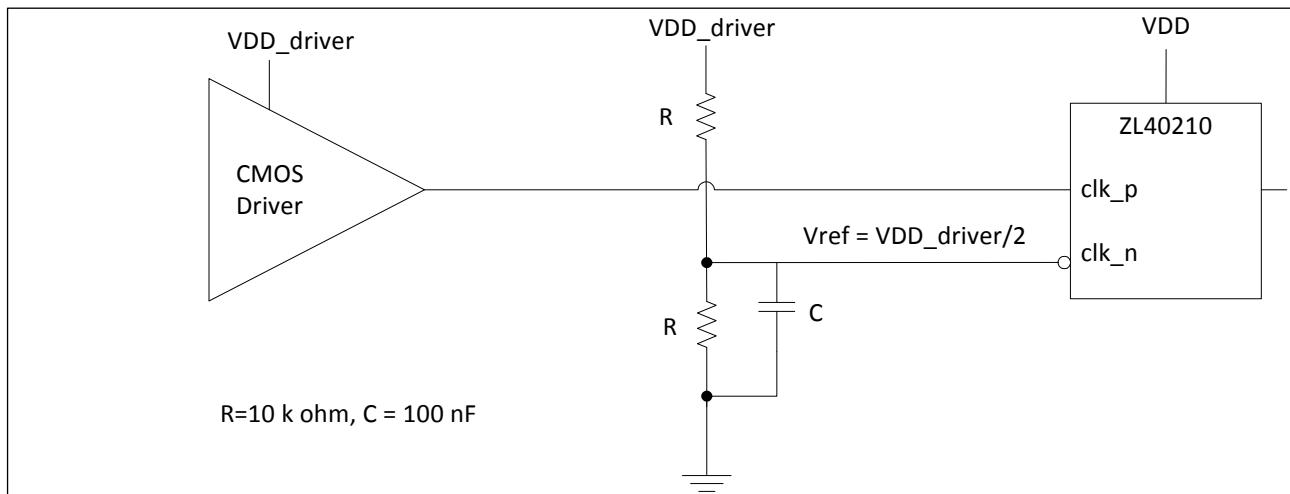


Figure 11 - CMOS Input DC Coupled Referenced to VDD/2

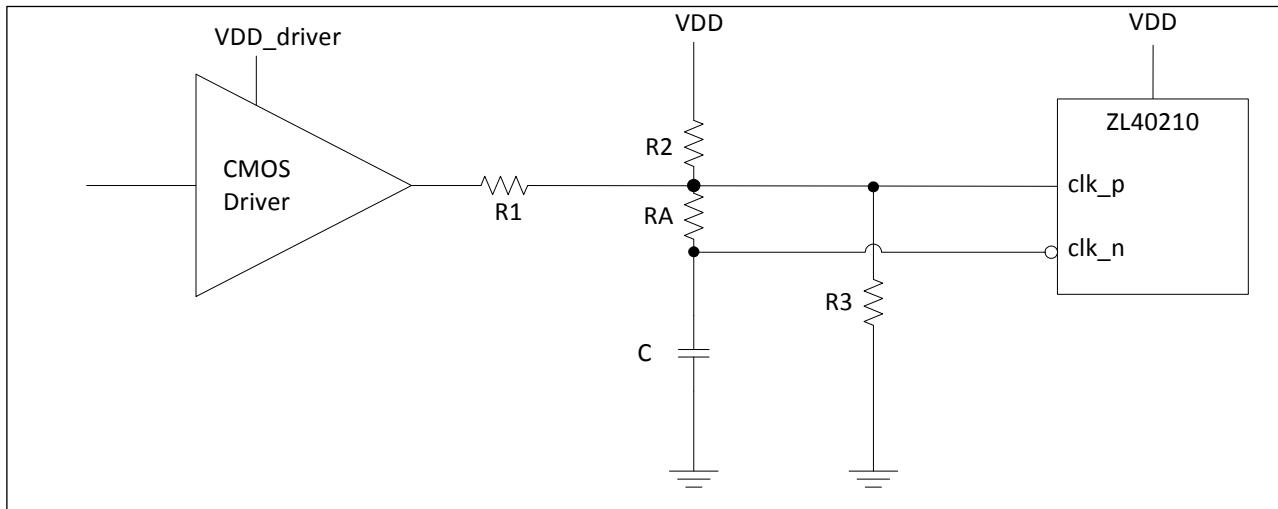


Figure 12 - CMOS Input DC Coupled Referenced to Ground

| VDD_driver | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) | RA (kΩ) | C (pF) |
|------------|---------|---------|---------|---------|--------|
| 1.5 | 1.25 | 3.075 | open | 10 | 10 |
| 1.8 | 1 | 3.8 | open | 10 | 10 |
| 2.5 | 0.33 | 4.2 | open | 10 | 10 |
| 3.3 | 0.75 | open | 4.2 | 10 | 10 |

Table 2 - Component Values for Single Ended Input Reference to Ground

* For frequencies below 100 MHz, increase C to avoid signal integrity issues.

3.2 Clock Outputs

LVPECL has a very low output impedance and a differential signal swing between 1V and 1.6 V. A simplified diagram for the output stage is shown in Figure 13. The LVPECL to LVDS output termination is not shown since there is a separate device that has the same input and LVDS outputs.

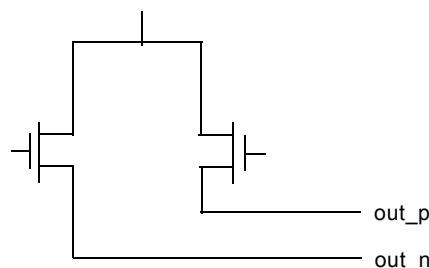


Figure 13 - Simplified Output Driver

The methods to terminate the ZL40210 LVPECL drivers are shown in the following figures.

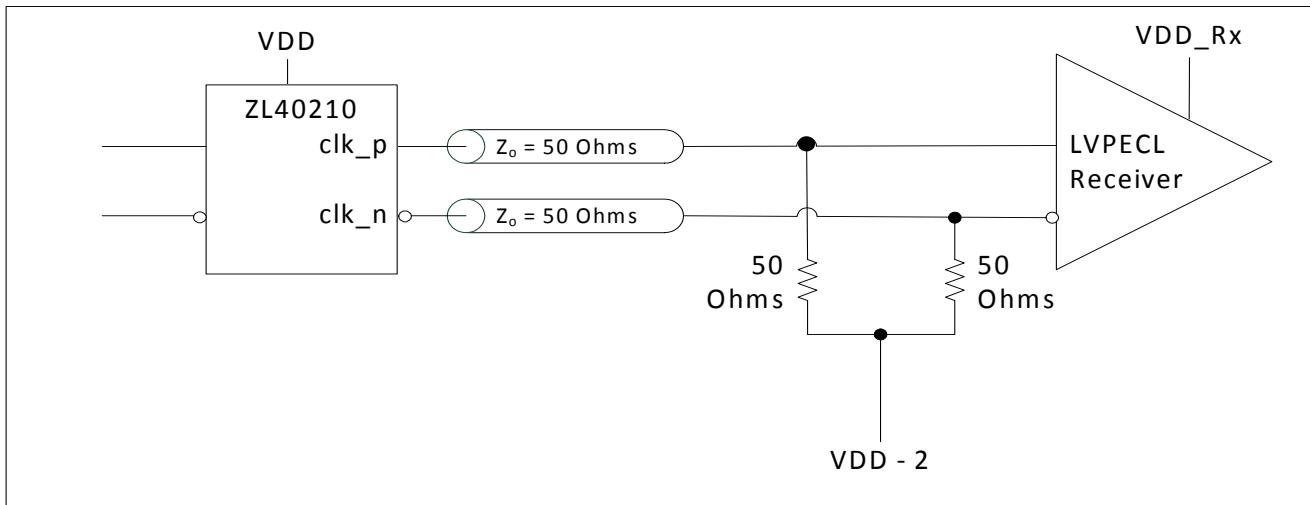


Figure 14 - LVPECL Basic Output Termination

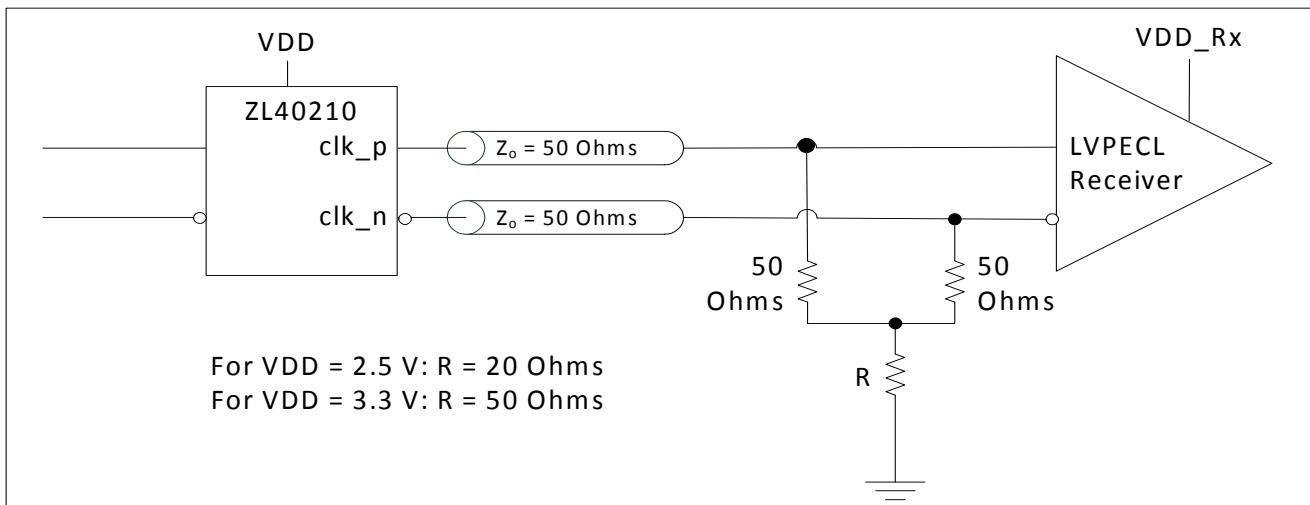


Figure 15 - LVPECL Parallel Output Termination

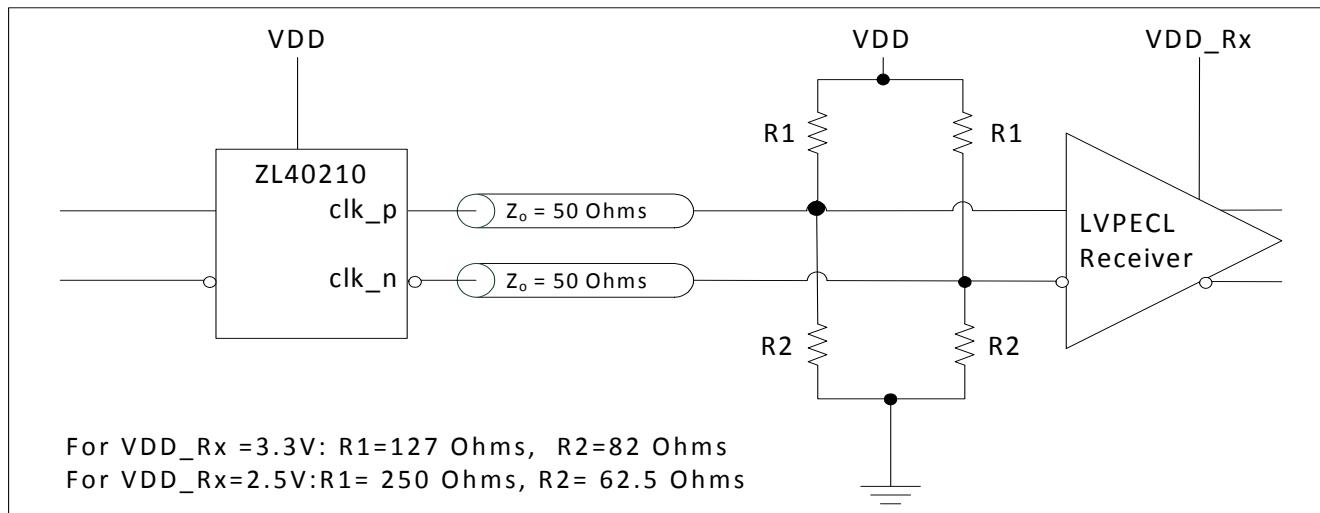


Figure 16 - LVPECL Parallel Thevenin-Equivalent Output Termination

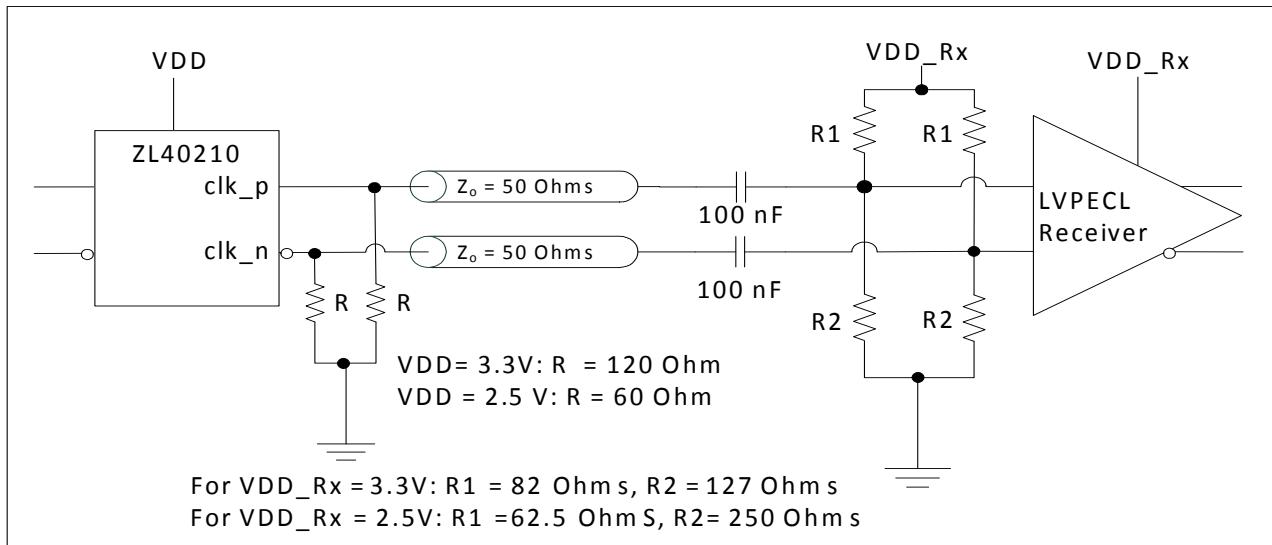


Figure 17 - LVPECL AC Output Termination for Externally Terminated LVPECL Inputs

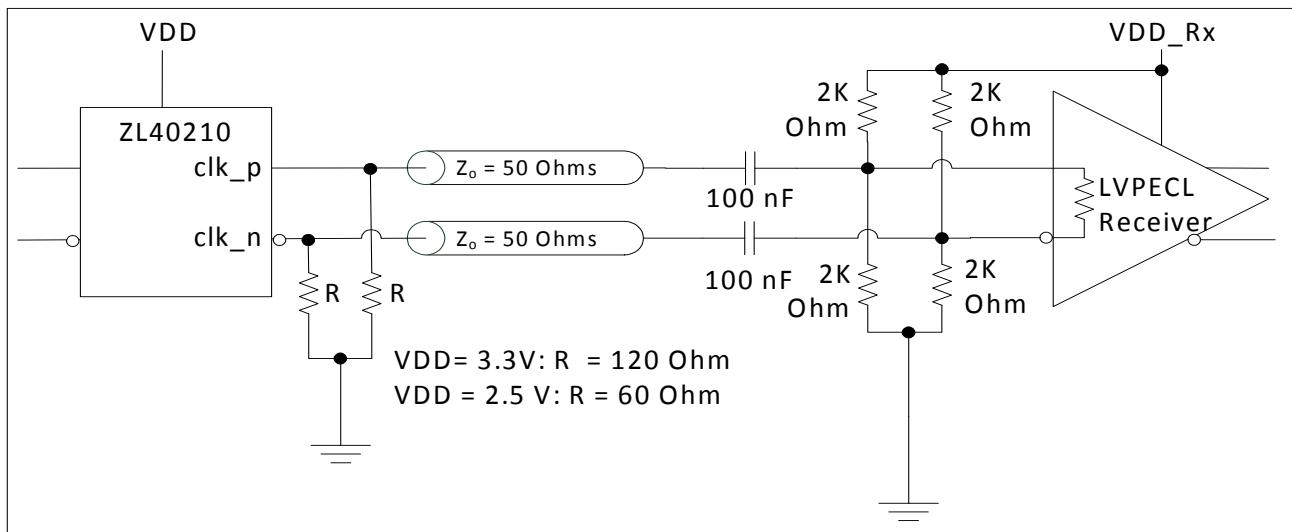


Figure 18 - LVPECL AC Output Termination for Internally Terminated LVPECL Inputs

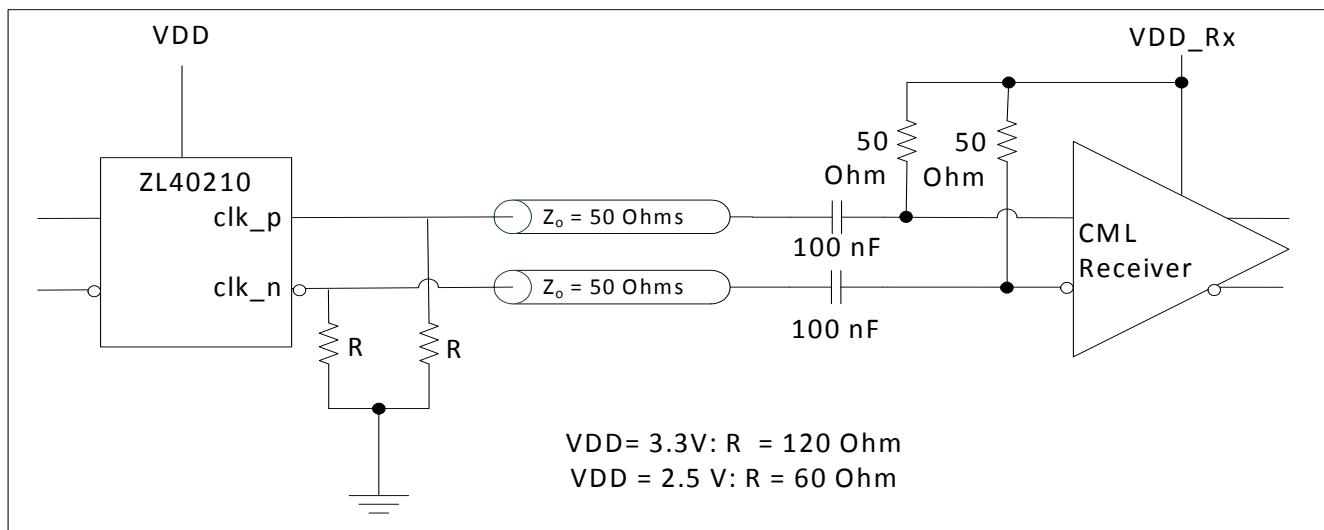


Figure 19 - LVPECL AC Output Termination for CML Inputs

3.3 Device Additive Jitter

The ZL40210 clock fan out buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40210 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40210 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources that are not shown in Figure 20.

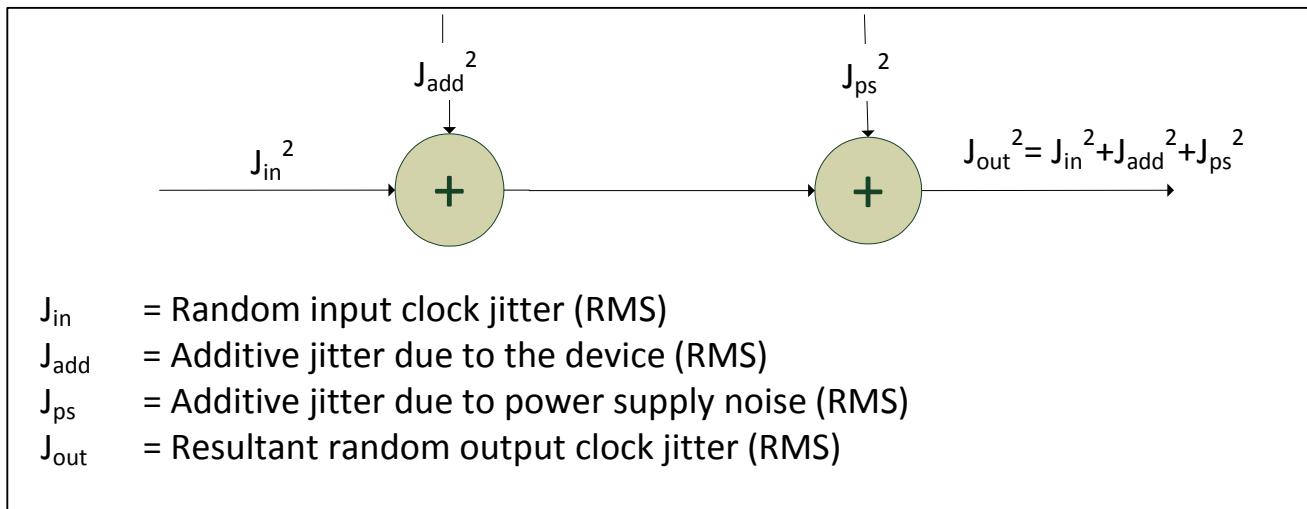


Figure 20 - Additive Jitter

3.4 Power Supply

This device operates with either a 2.5V supply or 3.3V supply.

3.4.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40210 is equipped with a low drop-out (LDO) regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

3.4.2 Power supply filtering

For optimal jitter performance, the ZL40210 should be isolated from the power planes connected to its power supply pins as shown in Figure 21.

- 10 μ F capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1 μ F capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins

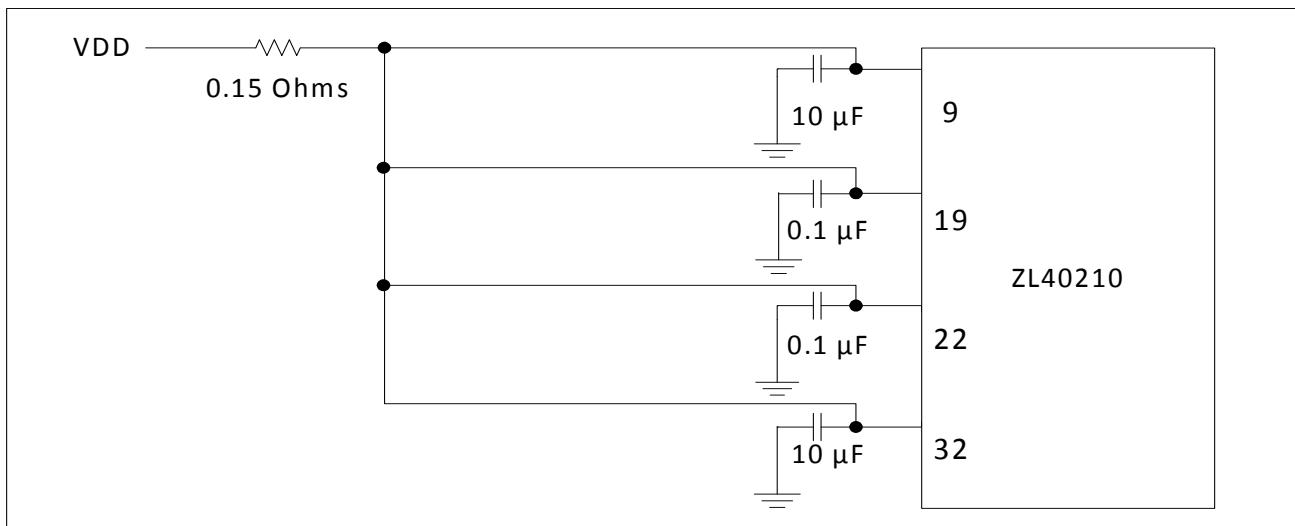


Figure 21 - Decoupling Connections for Power Pins

3.4.3 PCB layout considerations

The power supply filtering shown in Figure 21 can be implemented either as a plane island, or as a routed power topology with equal results.

4.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

| | Parameter | Sym. | Min. | Max. | Units |
|---|----------------------------|-------------|------|----------|-------|
| 1 | Supply voltage | V_{DD_R} | -0.5 | 4.6 | V |
| 2 | Voltage on any digital pin | V_{PIN} | -0.5 | V_{DD} | V |
| 3 | LVPECL output current | I_{out} | | 30 | mA |
| 4 | Soldering temperature | T | | 260 | °C |
| 5 | Storage temperature | T_{ST} | -55 | 125 | °C |
| 6 | Junction temperature | T_j | | 125 | °C |
| 7 | Voltage on input pin | V_{input} | | V_{DD} | V |
| 8 | Input capacitance each pin | C_p | | 500 | fF |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

| | Characteristics | Sym. | Min. | Typ. | Max. | Units |
|---|---------------------------|------------|-------|------|-------|-------|
| 1 | Supply voltage 2.5 V mode | V_{DD25} | 2.375 | 2.5 | 2.625 | V |
| 2 | Supply voltage 3.3 V mode | V_{DD33} | 3.135 | 3.3 | 3.465 | V |
| 3 | Operating temperature | T_A | -40 | 25 | 85 | °C |

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics - Current Consumption

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|------------------|------|------|------|-------|-------------------------------------|
| 1 | Supply current LVPECL drivers - unloaded | I_{dd_unload} | | 122 | | mA | Unloaded |
| 2 | Supply current LVPECL drivers - loaded (all outputs are active) | I_{dd_load} | | 257 | | mA | Including power to $R_L = 50\Omega$ |

DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|-----------|---------------|------|---------------|-------|-----------------------|
| 1 | CMOS control logic high-level input voltage | V_{CIH} | 0.7* V_{DD} | | | V | |
| 2 | CMOS control logic low-level input voltage | V_{CIL} | | | 0.3* V_{DD} | V | |
| 3 | CMOS control logic Input leakage current | I_{IL} | | 1 | | μA | $V_I = V_{DD}$ or 0 V |
| 4 | Differential input common mode voltage | V_{CM} | 1.1 | | 2.0 | V | |

DC Electrical Characteristics - Inputs and Outputs - for 3.3 V Supply

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---------------------------------------|----------|-----------------|------|-----------------|-------|-------|
| 5 | Differential input voltage difference | V_{ID} | 0.25 | | 1 | V | |
| 6 | LVPECL output high voltage | V_{OH} | $V_{DD} - 1.40$ | | | V | |
| 7 | LVPECL output low voltage | V_{OL} | | | $V_{DD} - 1.62$ | V | |
| 8 | LVPECL output differential voltage* | V_{OD} | 0.5 | | 0.9 | V | |

* Parameter measured from 125 MHz to 750 MHz

DC Electrical Characteristics - Inputs and Outputs - for 2.5 V Supply

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|-----------|-----------------|------|-----------------|---------|-----------------------|
| 1 | CMOS control logic high-level input voltage | V_{CIH} | $0.7*V_{DD}$ | | | V | |
| 2 | CMOS control logic low-level input voltage | V_{CIL} | | | $0.3*V_{DD}$ | V | |
| 3 | CMOS control logic Input leakage current | I_{IL} | | 1 | | μA | $V_I = V_{DD}$ or 0 V |
| 4 | Differential input common mode voltage | V_{CM} | 1.1 | | 1.6 | V | |
| 5 | Differential input voltage difference | V_{ID} | 0.25 | | 1 | V | |
| 6 | LVPECL output high voltage | V_{OH} | $V_{DD} - 1.40$ | | | V | |
| 7 | LVPECL output low voltage | V_{OL} | | | $V_{DD} - 1.62$ | V | |
| 8 | LVPECL output differential voltage* | V_{OD} | 0.4 | | 0.9 | V | |

* Parameter measured from 125 MHz to 750 MHz

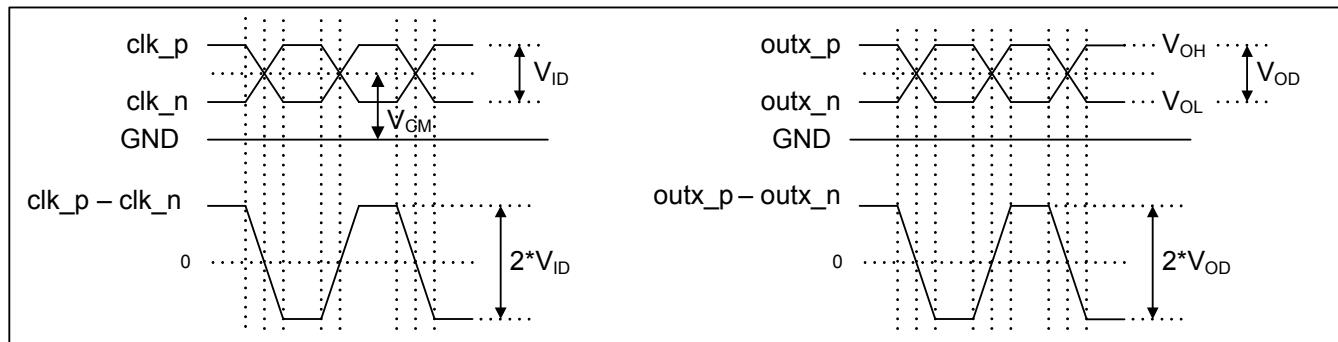


Figure 22 - Differential Output Voltage Parameter

AC Electrical Characteristics* - Inputs and Outputs (see Figure 23) - for 2.5/3.3 V supply.

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|-------------------|------|------|------|---------|-------|
| 1 | Maximum Operating Frequency | $1/t_p$ | | | 750 | MHz | |
| 2 | Input to output clock propagation delay | t_{pd} | 0 | 1 | 2 | ns | |
| 3 | Output to output skew | $t_{out2out}$ | | 50 | 100 | ps | |
| 4 | Part to part output skew | $t_{part2part}$ | | 80 | 300 | ps | |
| 5 | Output clock Duty Cycle degradation | t_{PWH}/t_{PWL} | -2 | 0 | 2 | Percent | |
| 6 | Output slew rate | r_{sl} | 0.75 | 1.2 | | V/ns | |
| 7 | Reference transition time | t_{switch} | | 2 | 3 | us | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions

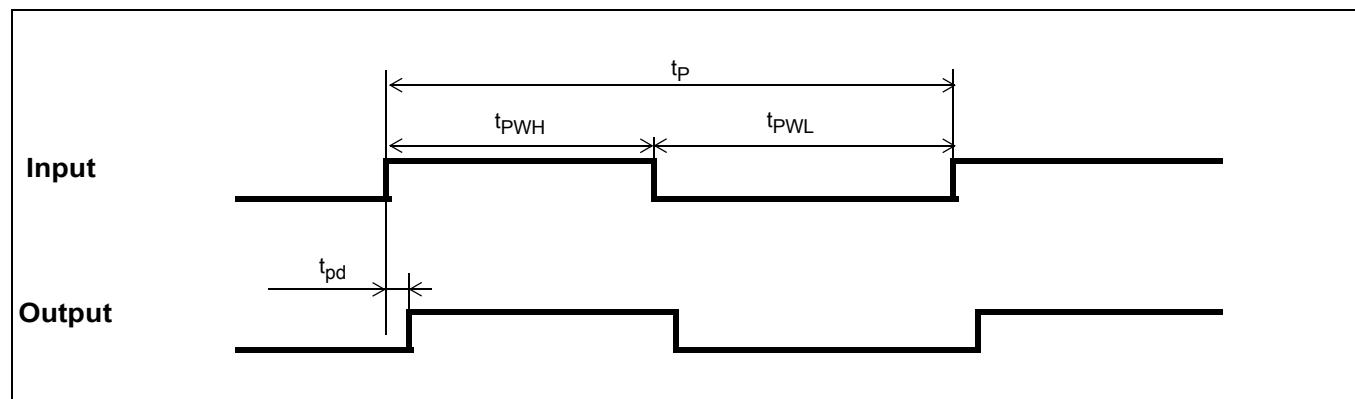


Figure 23 - Input To Output Timing

5.0 Performance Characterization

Additive Jitter at 2.5 V*

| | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|------------------------|---------------------------|------------------|-------|
| 1 | 125 | 12 kHz - 20 MHz | 214 | |
| 2 | 212.5 | 12 kHz - 20 MHz | 188 | |
| 3 | 311.04 | 12 kHz - 20 MHz | 168 | |
| 4 | 425 | 12 kHz - 20 MHz | 151 | |
| 5 | 500 | 12 kHz - 20 MHz | 144 | |
| 6 | 622.08 | 12 kHz - 20 MHz | 135 | |
| 7 | 750 | 12 kHz - 20 MHz | 121 | |

*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

Additive Jitter at 3.3 V*

| | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|------------------------|---------------------------|------------------|-------|
| 1 | 125 | 12 kHz - 20 MHz | 209 | |
| 2 | 212.5 | 12 kHz - 20 MHz | 184 | |
| 3 | 311.04 | 12 kHz - 20 MHz | 176 | |
| 4 | 425 | 12 kHz - 20 MHz | 163 | |
| 5 | 500 | 12 kHz - 20 MHz | 157 | |
| 6 | 622.08 | 12 kHz - 20 MHz | 146 | |
| 7 | 750 | 12 kHz - 20 MHz | 131 | |

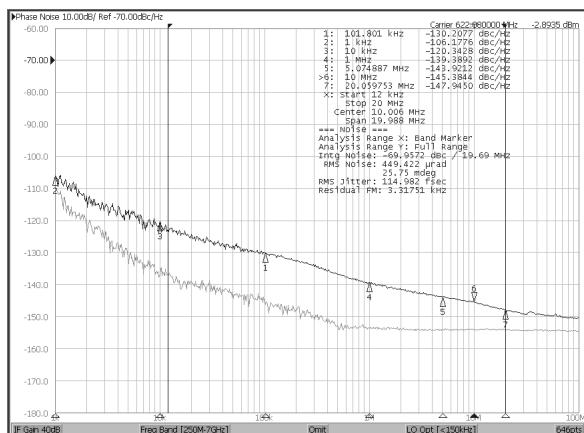
*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

Additive Jitter from a Power Supply Tone*

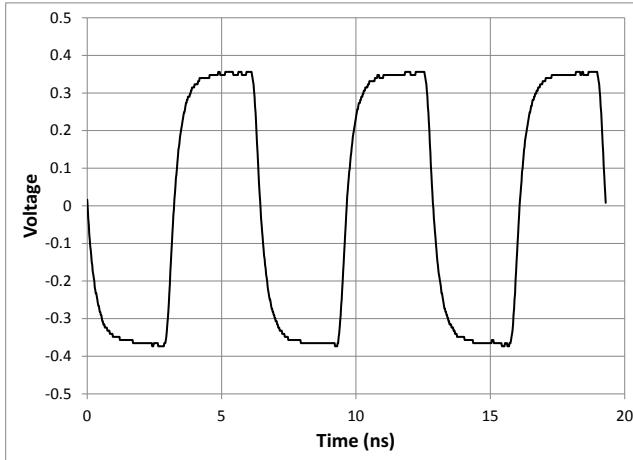
| Carrier frequency | Parameter | Typical | Units | Notes |
|-------------------|------------------|---------|--------|-------|
| 125MHz | 25 mV at 100 kHz | 114 | fs RMS | |
| 750MHz | 25 mV at 100 kHz | 52 | fs RMS | |

* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for $V_{DD} = 2.5$ V. The magnitude of the interfering tone is measured at the DUT.

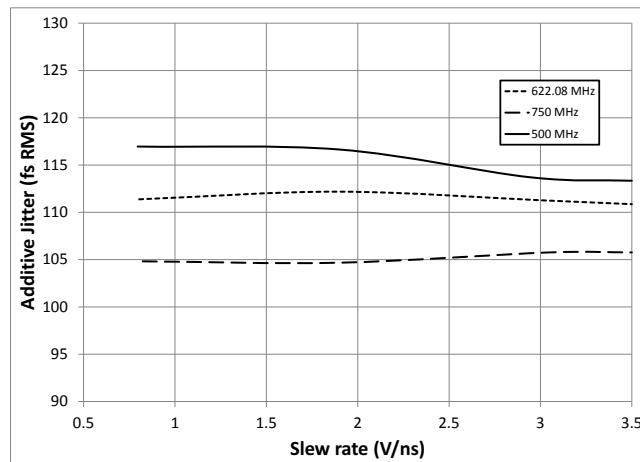
6.0 Typical Behavior



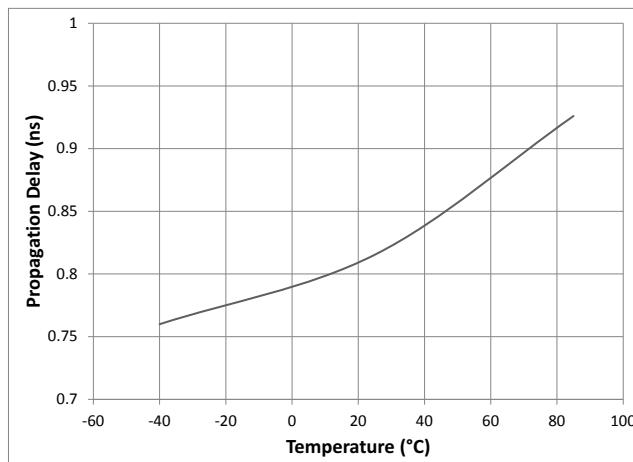
Typical Phase Noise at 622.08 MHz



Typical Waveformat 155.52 MHz

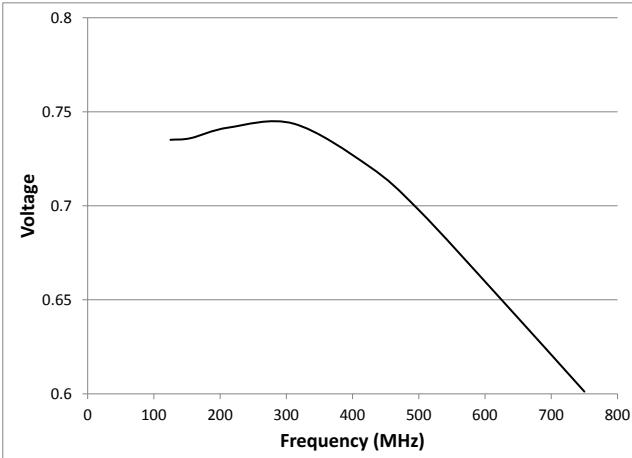


Input Slew Rate versus Additive Jitter

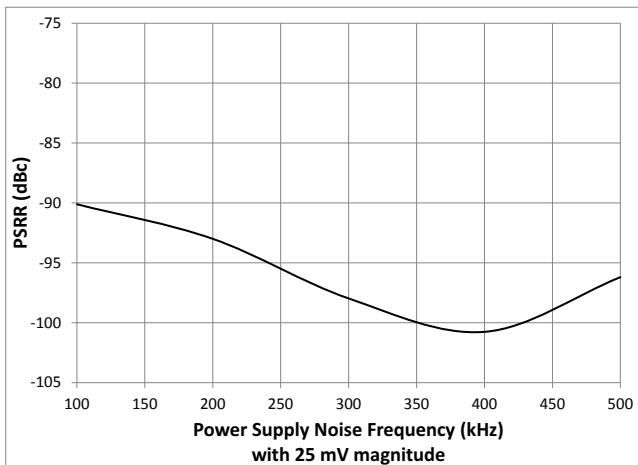


Propagation Delay versus Temperature

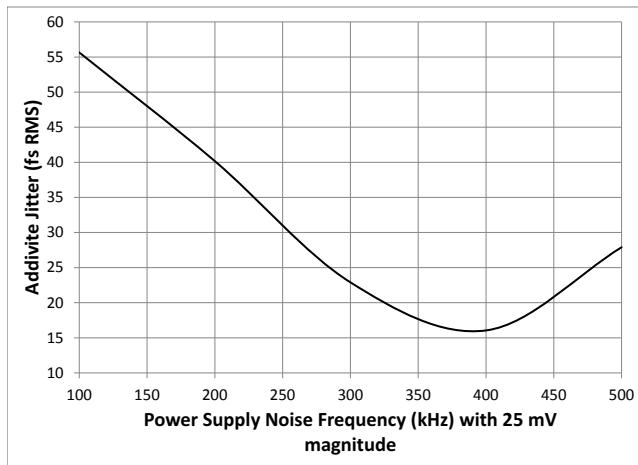
Note: This is for a single device. For more details see the



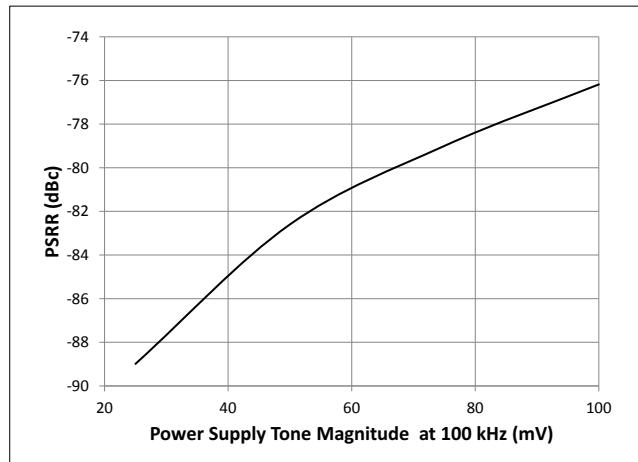
V_{OD} versus Frequency



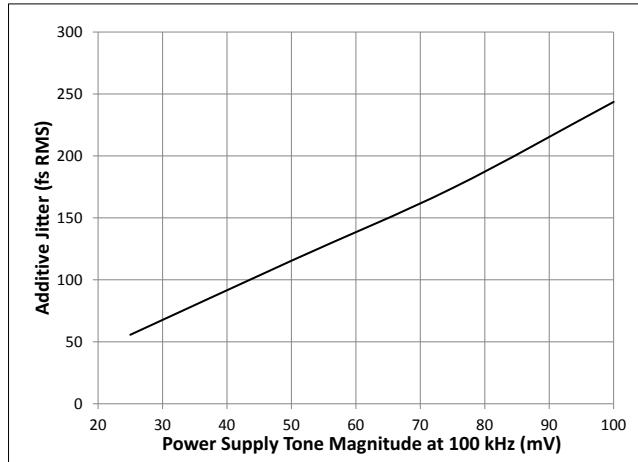
Power Supply Tone Frequency (at 25 mV) versus PSRR at 125 MHz



Power Supply Tone Frequency (at 25 mV) versus Additive Jitter at 125 MHz



Power Supply Tone Magnitude (at 100 kHz) versus PSRR at 125 MHz



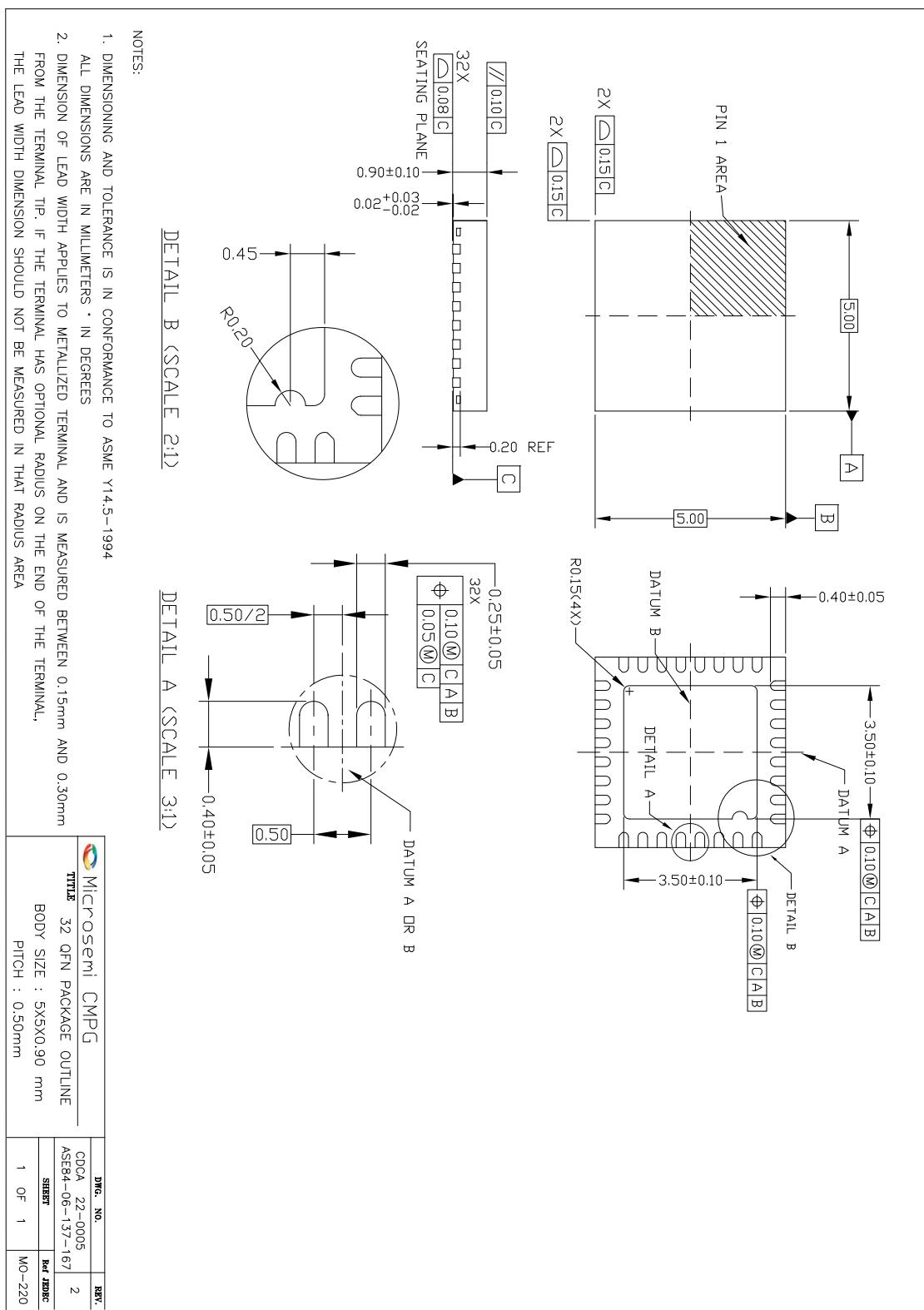
Power Supply Tone Magnitude (at 100 kHz) versus Additive Jitter at 125 MHz

7.0 Package Characteristics

Thermal Data

| Parameter | Symbol | Test Condition | Value | Unit |
|--|---------------|----------------|-------|------|
| Junction to Ambient Thermal Resistance | Θ_{JA} | Still Air | 37.4 | °C/W |
| | | 1 m/s | 33.1 | |
| | | 2 m/s | 31.5 | |
| Junction to Case Thermal Resistance | Θ_{JC} | | 24.4 | °C/W |
| Junction to Board Thermal Resistance | Θ_{JB} | | 19.5 | °C/W |
| Maximum Junction Temperature* | T_{jmax} | | 125 | °C |
| Maximum Ambient Temperature | T_A | | 85 | °C |

8.0 Mechanical Drawing



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