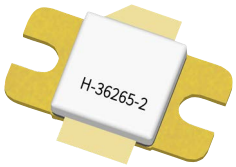
PTVA120501EA

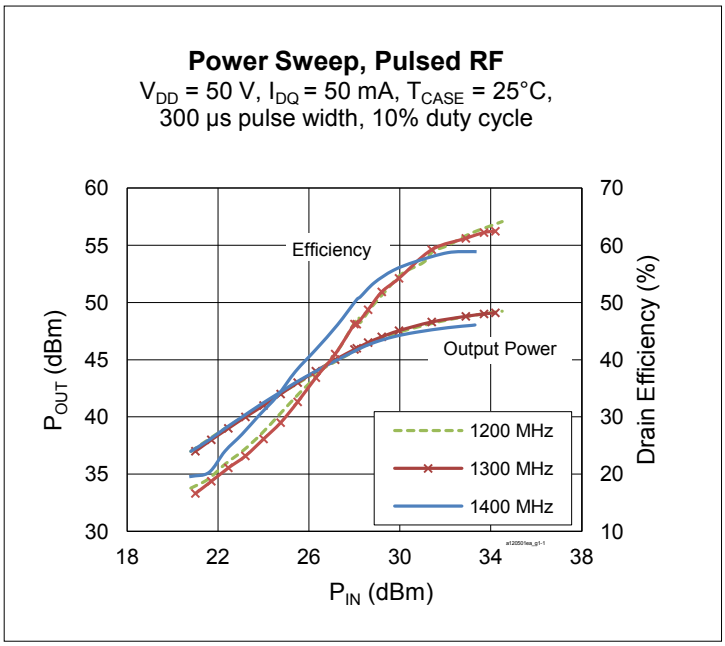
Thermally-Enhanced High Power RF LDMOS FET
50 W, 50 V, 1200 – 1400 MHz

Description

The PTVA120501EA LDMOS FET is designed for use in power amplifier applications in the 1200 to 1400 MHz frequency band. Features include high gain and thermally-enhanced package with bolt-down flange. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTVA120501EA
Package H-36265-2



Features

- Broadband input matching
- High gain and efficiency
- Typical Pulsed CW performance, 1200 – 1400MHz, 50 V, 300 µs pulse width, 10 % duty cycle, class AB
  - Output power at P_{1dB} = 54 W
  - Efficiency = 55%
  - Gain = 16 dB
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant
- Capable of withstanding a 10:1 load mismatch (all phase angles) at 50 W peak under RF pulse, 300 µS, 10% duty cycle.

RF Characteristics

Pulsed RF Performance (tested in the test fixture)

V_{DD} = 50 V, I_{DQ} = 50 mA, P_{OUT} = 50 W, f_1 = 1200 MHz, f_2 = 1300 MHz, f_3 = 1400 MHz, 300 µs pulse width, 10 % duty cycle

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	16.5	17	—	dB
Drain Efficiency	η_D	46	50	—	%
Return Loss	IRL	—	–10	–7	dB

All published data at T_{CASE} = 25°C unless otherwise indicated
ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

Rev. 04, 2023-07-10

RF Characteristics

Typical RF Performance (not subject to production test, verified by design/characterization in the test fixture)
V_{DD} = 50 V, I_{DQ} = 50 mA, Input signal (t_r = 7 ns, t_f = 8 ns), 300 µs pulse width, 10% duty cycle, class AB test

Mode of Operation	f (MHz)	IRL (dB)	P_{1dB}			P_{3dB}			Max $P_{droop\ (pulse)}$ dB @ 50 W	$t_{r\ (ns)}$ @ 50 W*	$t_{f\ (ns)}$ @ 50 W*
			Gain (dB)	Eff (%)	P_{OUT} (W)	Gain (dB)	Eff (%)	P_{OUT} (W)			
Pulsed RF	1200	–8	16	56	60	14	58	78	0.20	5	<2
Pulsed RF	1300	–10	16	57	60	14	58	78	0.20	5	<2
Pulsed RF	1400	–8	16	55	54	14	57	57	0.15	5	<2

** Note = t_r and t_f are defined as Δ between input and output rise and fall times*

Typical RF Performance (not subject to production test, verified by design/characterization in the test fixture)
V_{DD} = 50 V, I_{DQ} = 50 mA, 30 ms pulse width, 33% duty cycle, class AB test

Mode of Operation	f (MHz)	P_{1dB}			P_{3dB}			$P_{droop\ (pulse)}$ dB @ 50 W
		Gain (dB)	Eff (%)	P_{OUT} (W)	Gain (dB)	Eff (%)	P_{OUT} (W)	
Pulsed RF	1200	16	57	57	14	59	75	0.3
Pulsed RF	1300	16	56	55	14	58	75	0.3
Pulsed RF	1400	16	49	50	14	50	55	0.2

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	V_{DS} = 50 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
	V_{DS} = 105 V, V_{GS} = 0 V	I_{DSS}	—	—	10	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.4	—	Ω
Operating Gate Voltage	V_{DS} = 50 V, I_{DQ} = 50 mA	V_{GS}	3.0	3.5	4.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA

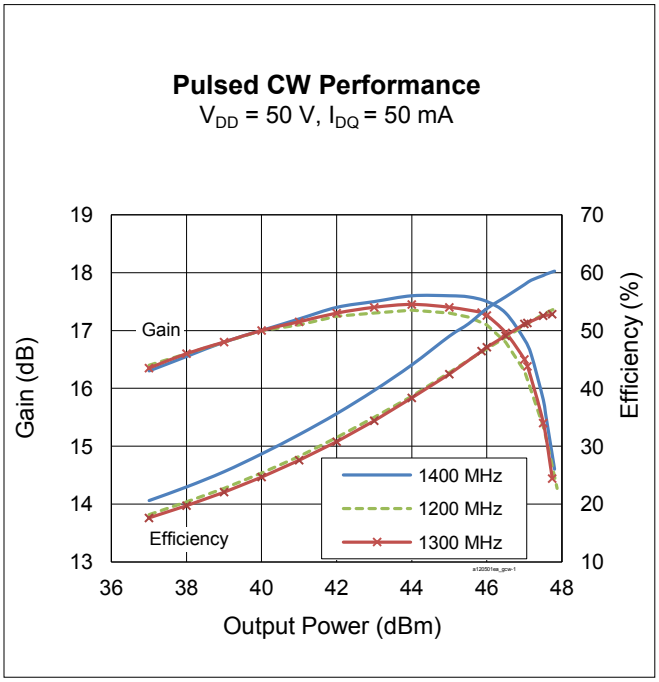
Maximum Ratings

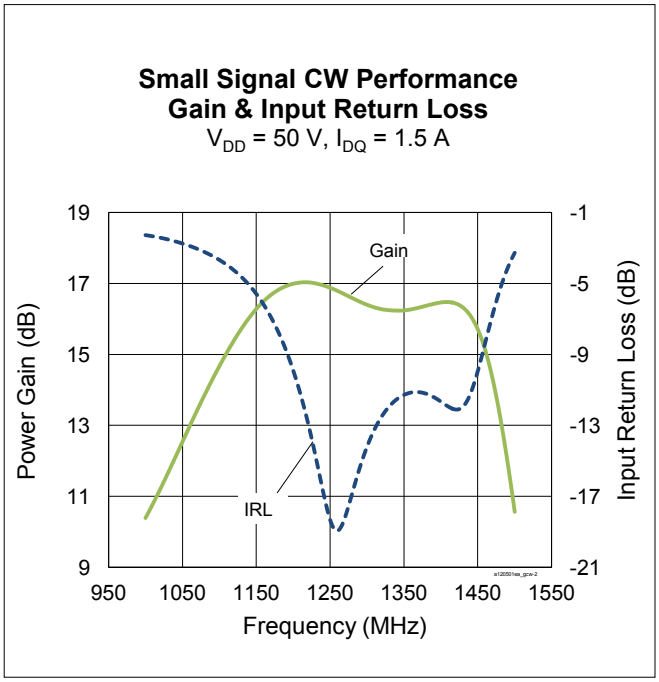
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	105	V
Gate-Source Voltage	V_{GS}	–6 to +12	V
Operating Voltage	V_{DD}	0 to +55	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 50 W CW)	$R_{\theta JC}$	1.37	°C/W

Ordering Information

Type and Version	Order Code	Package Description	Shipping
PTVA120501EA V1 R0	PTVA120501EA-V1-R0	H-36265-2, bolt-down	Tape & Reel, 50 pcs
PTVA120501EA V1 R2	PTVA120501EA-V1-R2	H-36265-2, bolt-down	Tape & Reel, 250 pcs

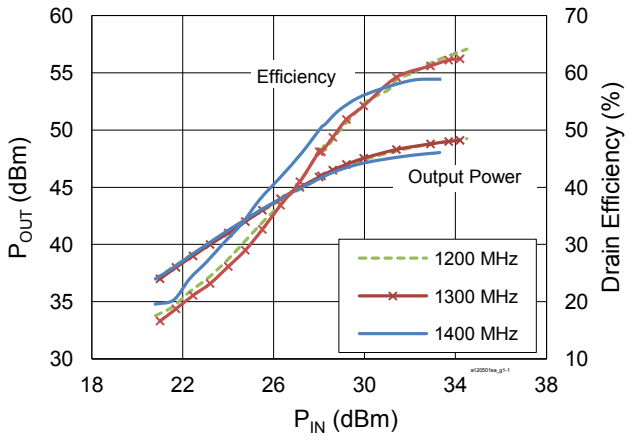
Typical Performance (data taken in a production test fixture)



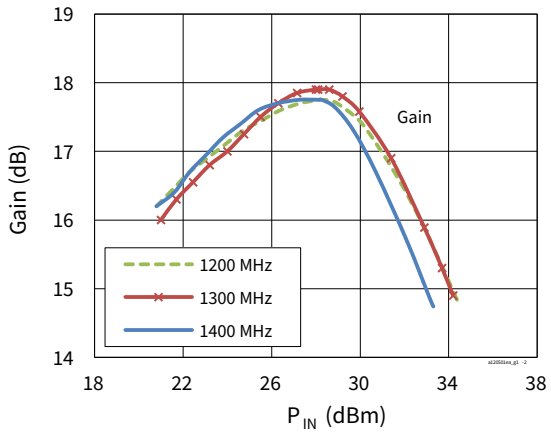


Typical Performance (cont.)

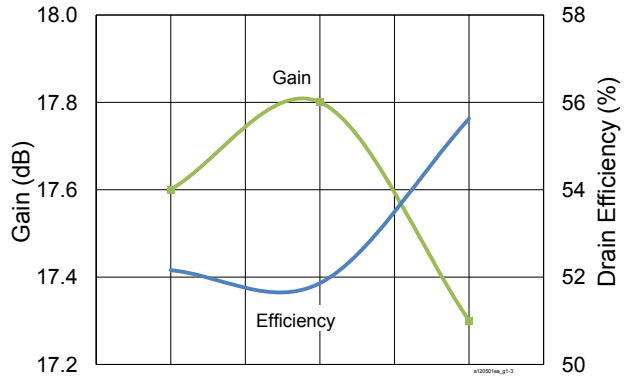
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, T_{CASE} = 25°C,
300 µs pulse width, 10% duty cycle



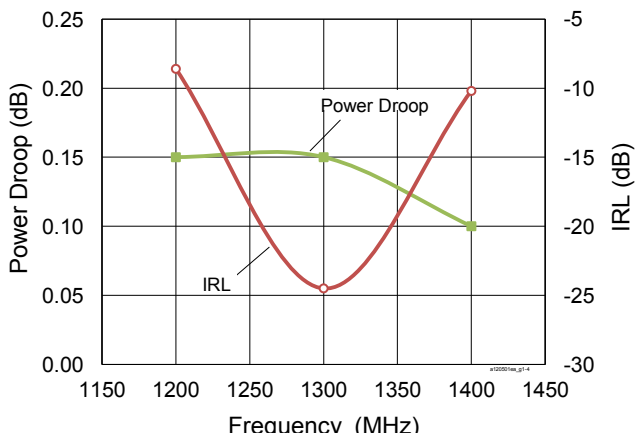
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, T_{CASE} = 25 °C,
300 µs pulse width, 10% duty cycle



Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, P_{OUT} = 50 W,
300 µs pulse width, 10% duty cycle

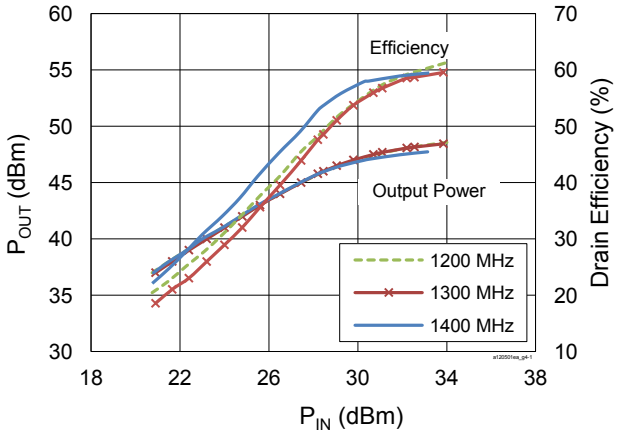


Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, P_{OUT} = 50 W,
300 µs pulse width, 10% duty cycle

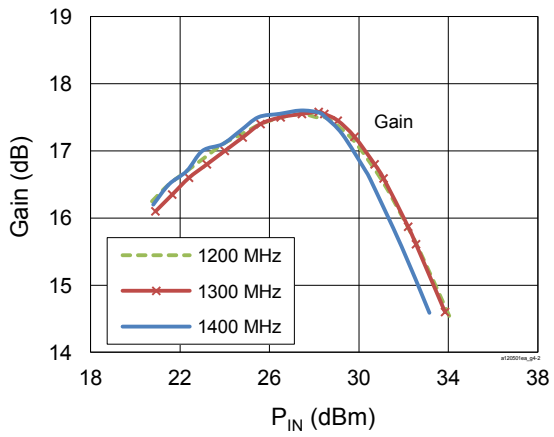


Typical Performance (cont.)

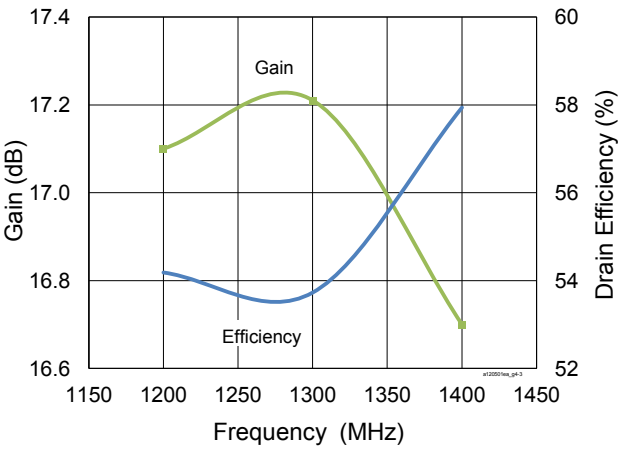
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, T_{CASE} = 25°C,
16 ms pulse width, 50% duty cycle



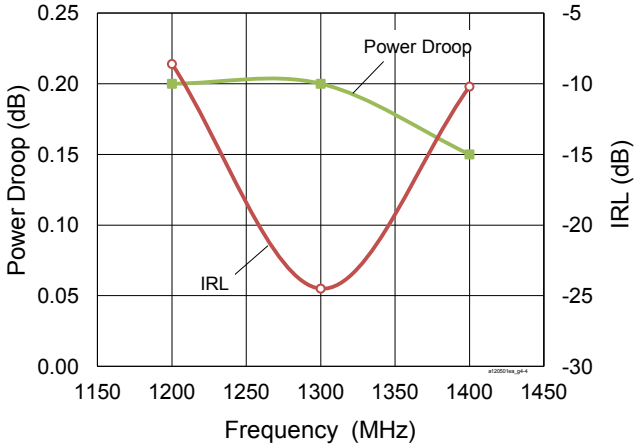
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, T_{CASE} = 25°C,
16 ms pulse width, 50% duty cycle



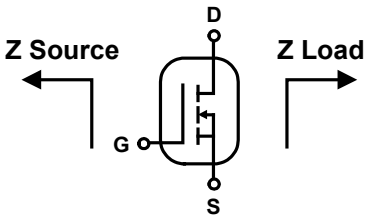
Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, P_{OUT} = 50 W,
16 ms pulse width, 50% duty cycle



Power Sweep, Pulsed RF
V_{DD} = 50 V, I_{DQ} = 50 mA, P_{OUT} = 50 W,
16 ms pulse width, 50% duty cycle



Broadband Circuit Impedance



Freq [MHz]	Z Source Ω		Z Load Ω	
	R	jX	R	jX
1200	8.07	–2.13	3.66	4.97
1300	5.13	–0.95	3.90	4.56
1400	5.64	2.24	3.25	5.36

Load Pull Performance

Load Pull at Max P_{OUT} Point – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 50 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
1200	3.04 – j2.16	30.68	47.30	53.70	16.62	45.56	3.19 – j1.55

Load Pull at Max G_T Point – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 50 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
1200	3.04 – j2.16	27.50	46.10	40.74	18.60	57.50	2.88 – j4.11

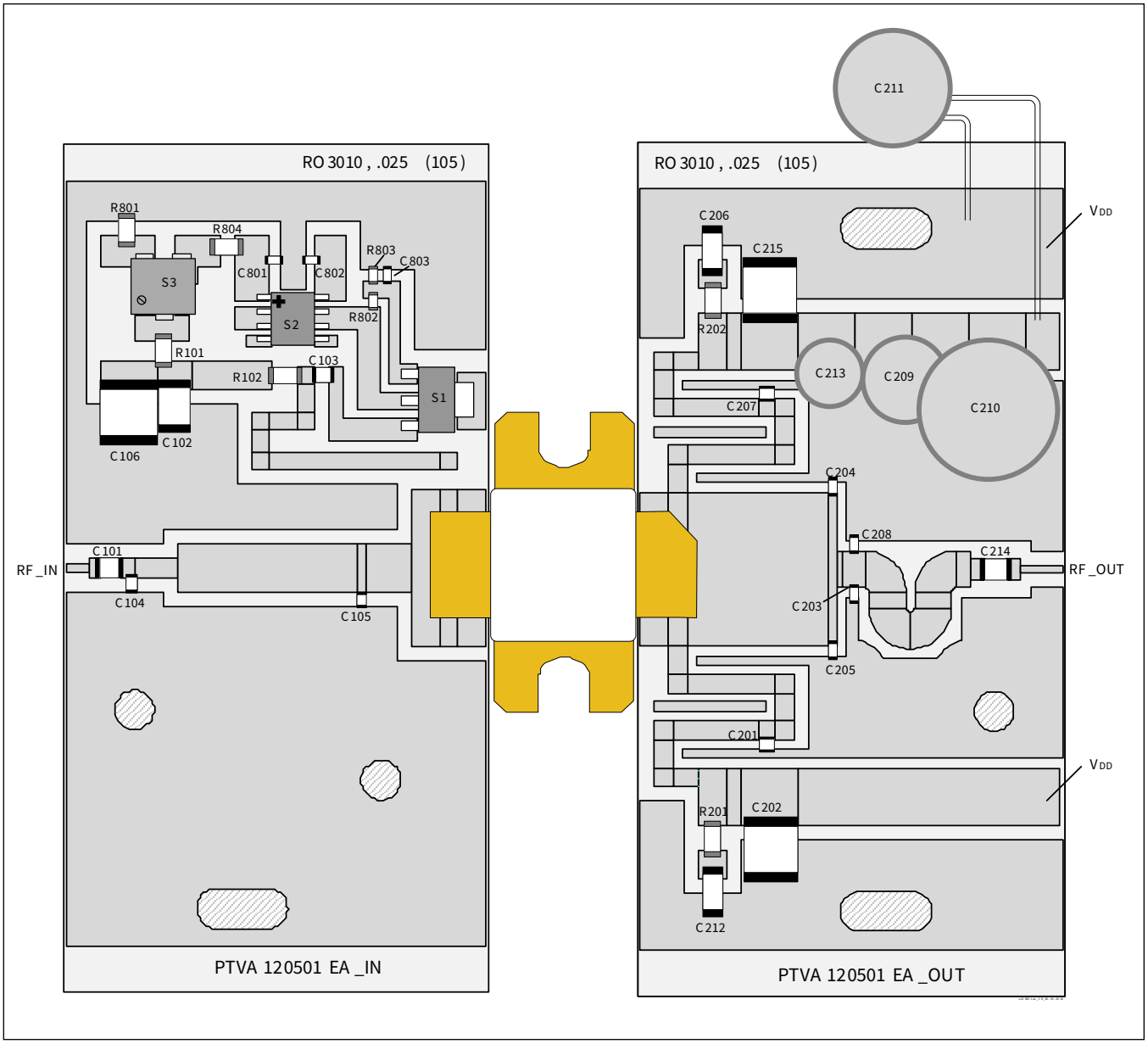
Load Pull at Max Efficiency Point – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 50 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
1200	3.04 – j2.16	27.55	46.15	41.21	18.60	57.20	2.88 – j4.06

Z Optimum – 16 µs pulse width, 10% duty cycle, class AB, V_{DD} = 50 V, 50 mA

Freq [MHz]	Zl [Ω]	P_{IN} [dBm]	P_{OUT} [dBm]	P_{OUT} [W]	P_G [dB]	PAE Eff [%]	Z_{OUT} [Ω]
1200	3.04 – j2.16	28.70	46.57	45.39	17.87	50.46	2.92 – j3.12

Reference Circuit , 1200 – 1400 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

Reference Circuit Assembly

DUT	PTVA120501EA
Test Fixture Part No.	LTN/PTVA120501EA V1
PCB	Rogers 6006, 0.635 mm [0.025"] thick, 2 oz. copper, ε_r = 6.15, ƒ = 1200 – 1400 MHz

Components Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101	Capacitor, 39 pF	ATC	ATC100B390KW500XB
C102	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C103	Capacitor, 33 pF	ATC	ATC100A330JW150XB
C104	Capacitor, 2.7 pF	ATC	ATC800A2R7BT
C105	Capacitor, 10 pF	ATC	ATC800A100JT
C106	Capacitor, 10 µF	TDK Corporation	C5750X5R1H106K230KA
C801, C802, C803	Capacitor, 1000 pF	Panasonic Electronic Components	ECJ-1VB1H102K
R101	Resistor, 1000 Ω	Panasonic Electronic Components	ERJ-8GEYJ102V
R102	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-8GEYJ100V
R801	Resistor, 2000 Ω	Panasonic Electronic Components	ERJ-8GEYJ202V
R802	Resistor, 1200 Ω	Panasonic Electronic Components	ERJ-3GEYJ122V
R803	Resistor, 1300 Ω	Panasonic Electronic Components	ERJ-3GEYJ132V
R804	Resistor, 100 Ω	Panasonic Electronic Components	ERJ-8GEYJ100V
S1	Transistor	Infineon Technologies	BCP56
S2	Voltage Regulator	Texas Instruments	LM78L05ACM
S3	Potentiometer, 2k Ω	Bourns Inc.	3224W-1-202E
Output			
C201, C207	Capacitor, 33 pF	ATC	ATC100A330JW150XB
C202, C215	Capacitor, 10 µF	TDK Corporation	C5750X5R1H106K230KA
C203, C208	Capacitor, 3.9 pF	ATC	ATC800A3R9BT
C204, C205	Capacitor, 6.8 pF	ATC	ATC800A6R8BT
C206, C212	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C209	Capacitor, 22 µF	Cornell Dubilier Electronics (CDE)	SEK220M100ST
C210	Capacitor, 100 µF	Cornell Dubilier Electronics (CDE)	SK101M100ST
C211	Capacitor, 6800 µF	Cornell Dubilier Electronics (CDE)	ECO-S2AP682EA
C213	Capacitor, 10 µF	Cornell Dubilier Electronics (CDE)	SEK100M100ST
C214	Capacitor, 39 pF	ATC	ATC100B390KW500XB
R201, R202	Resistor, 5600 Ω	Panasonic Electronic Components	ERJ-8RQJ5R6V

Package Outline Specifications

Package H-36265-2

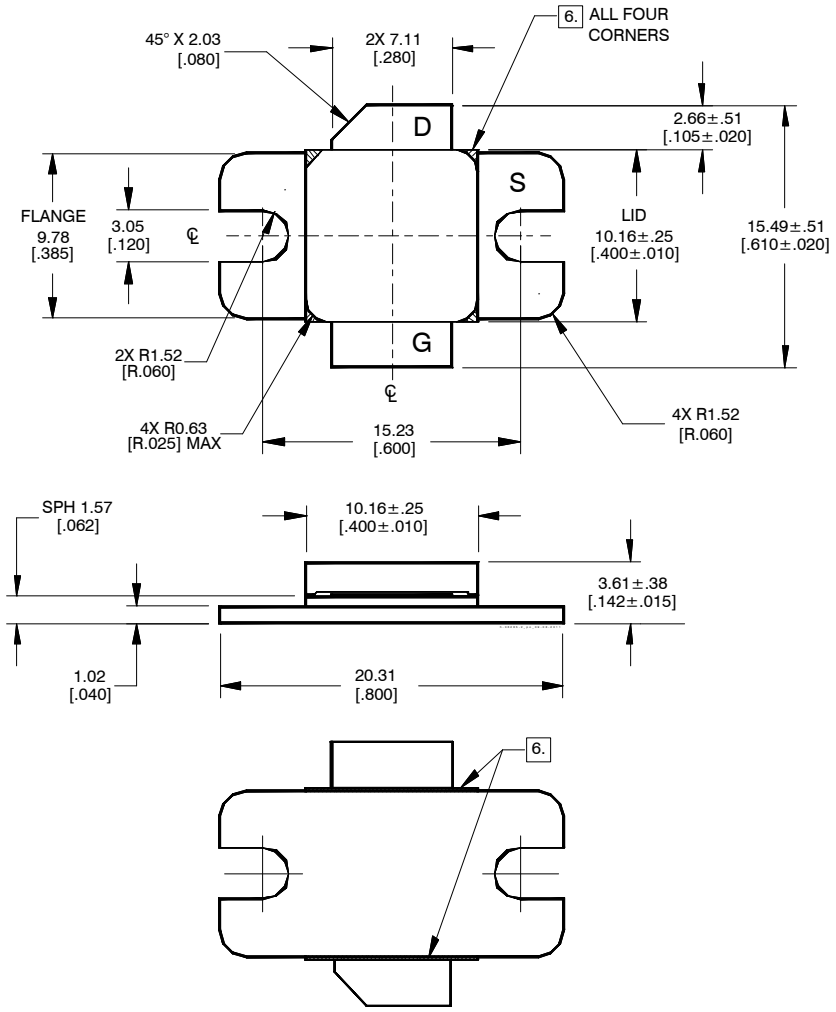


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ±0.127 [0.005] unless specified otherwise.
4. Pins: D – drain; G – gate; S – source
5. Lead thickness: 0.10 + 0.051/–0.025 mm [0.004 + 0.002/–0.001 inch].
6. Exposed metal plane on top and bottom of ceramic insulator.
7. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

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