LAN8770

100BASE-T1 Ethernet PHY Transceiver

Highlights

- Single-chip Ethernet physical layer transceiver
- Compliant with IEEE 802.3bw-2015 (100BASE-T1)
- Supports MII/RMII/RGMII (RGMII LAN8770R only)
- OPEN Alliance TC10 support / wake-up support
- Ultra low power sleep
- FlexPWR® technology power management
- Advanced Signal Quality Indicator (SQI)
- Over-temperature and under-voltage protection
- Comprehensive status interrupt support
- Extended cable reach
- Small footprint 32-pin VQFN (5 x 5 mm) and 36-pin VQFN (6 x 6 mm) with wettable flanks
- AEC-Q100 automotive product qualification
- Grade 1 Automotive temperature range (-40°C to +125°C)
- Microchip Functional Safety Ready

Target Applications

- Advanced Driver-Assistance Systems (ADAS)
- Infotainment
- Telematics & Smart Antennas
- In-Vehicle Backbone
- Gateways

Key Benefits

- High-performance 100BASE-T1 Ethernet PHY
  - Compliant with IEEE 802.3bw-2015
  - 100Mbps over single balanced twisted pair cable
  - OPEN Alliance TC10 sleep/wake-up support
  - Supports cable lengths up to at least 15m
  - 3-level Pulse Amplitude Modulation (PAM-3) line coding
  - Echo cancellation
  - Jumbo frame support up to 16KB
  - On-chip termination resistors for balanced UTP cable
- MII/RMII/RGMII Interfaces (RGMII LAN8770R only)
  - 125MHz reference clock output (LAN8770R only)
  - 25MHz / 50MHz RMII clock mode
  - Reverse MII mode for back-to-back connection of two PHYs (LAN8770M only)
  - SMI interface for rapid register access
- Low RF Emissions
  - Integrated transmission filtering
  - MII/RMII/RGMII drive strength adjust
  - 125MHz RGMII clock slew rate adjust
- EtherGREEN™ Energy Efficiency
  - Ultra low-power sleep mode (typical 12µA) with local wake-up support (OPEN Alliance TC10)
  - Sleep request recognition
  - IDLE detection on MDI
  - **WAKE_IN** pulse detection wakeup
  - **INH** output for enable/disable of ECU supply
  - **ENABLE** dedicated PHY enable/disable input pin
- Resets
  - Pin reset (**RESET_N**)
  - Power-On Reset (POR) with brownout protection
  - Software reset
- Packaging
  - LAN8770M: 32-pin (5 x 5 mm) wettable VQFN
  - LAN8770R: 36-pin (6 x 6 mm) wettable VQFN
- Environmental
  - AEC-Q100 Grade 1 Automotive temperature range (-40°C to +125°C)
- Functional Safety
  - FMEDA Computation Spreadsheet (Evaluation of Random Hardware Failures Metric)
  - Functional Safety Manual

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1.0 INTRODUCTION

1.1 General Description

The Microchip LAN8770 is a compact, cost-effective, single-port 100BASE-T1 Ethernet physical layer transceiver compliant with the IEEE 802.3bw-2015 specification. The device provides 100 Mbit/s transmit and receive capability over a single Unshielded Twisted Pair (UTP) cable, supporting cable lengths of up to at least 15m. The LAN8770 is available in a Grade 1 Automotive (-40°C to +125°C) temperature range and is optimized for AEC-Q100 automotive use cases such as Automated Driver-Assistance Systems (ADAS), infotainment, telematics, smart antennas, and in-vehicle backbones.

The LAN8770 supports communication with an Ethernet MAC via standard MII/RMII/RGMII interfaces (RGMII LAN8770R only). An optional 125MHz or 50MHz reference clock output is provided for RGMII and RMII applications, respectively. Reverse MII mode (LAN8770M only) provides the ability to connect two PHYs back-to-back. An integrated SMI interface provides rapid register access and configuration.

Microchip's LAN8770 EtherGREEN™ energy efficient technology provides low-power 100BASE-T1 PHY operation along with an ultra low-power sleep mode with local wake-up support (partial networking), sleep request recognition, and various wake/enable signals for low power modes. FlexPWR® variable I/O and core power supply voltages provide flexible design options and power saving opportunities.

Advanced PHY diagnostics provide the user with troubleshooting capabilities such as cable defect detection of shorts or opens, a receiver Signal Quality Indicator (SQI), over-temperature, under-voltage protection, comprehensive status interrupt support, and various loopback and test modes.

The Microchip LAN8770 family includes the following devices:

- LAN8770M
- LAN8770R

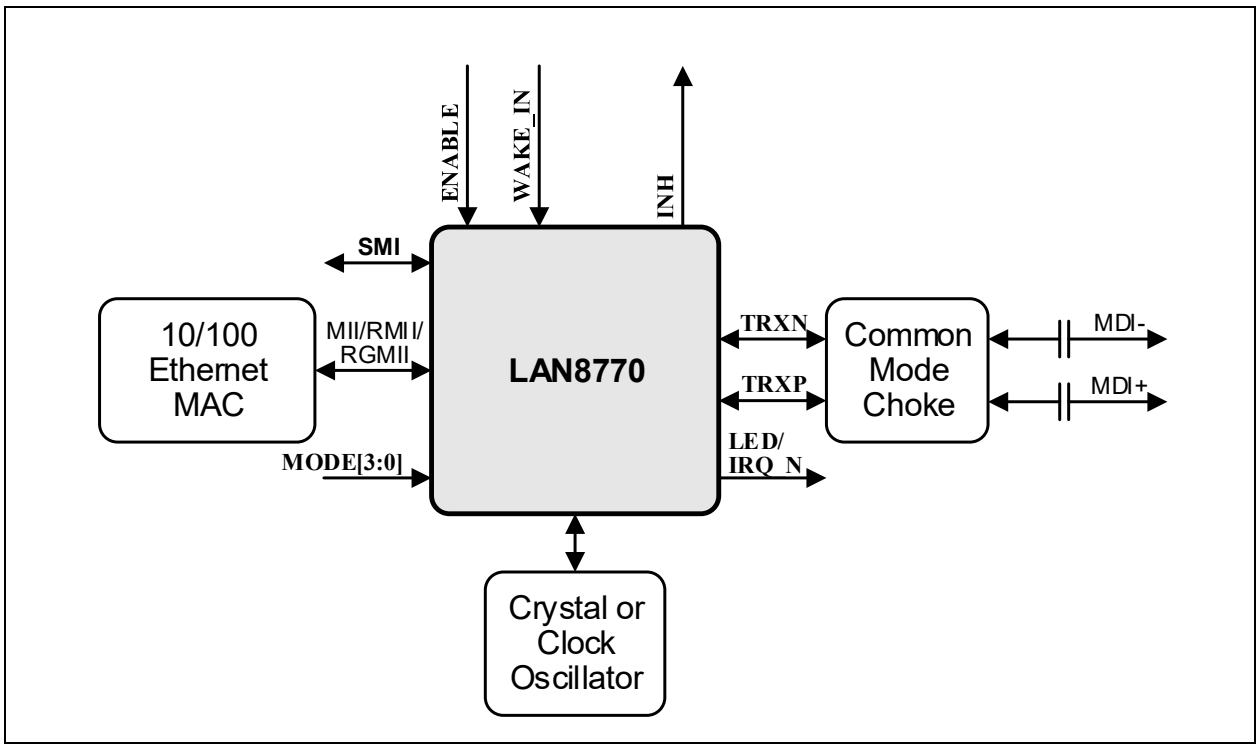
Device specific features that do not pertain to the entire LAN8770 family are called out independently throughout this document. Table 1-1 provides a summary of the feature differences between family members:

TABLE 1-1: LAN8770 FAMILY FEATURE MATRIX

Part Number	Package	MII Support	RMII Support	RGMII Support	125MHz Reference Clock Output	Reverse MII Mode	Internal 1.1V Regulator Disable Option	ENABLE Pin Support	INH Pin Support	WAKE_IN Pin Support	AEC-Q100 -40° To 125°C
LAN8770M	32-VQFN	X	X			X		X	X	X	X
LAN8770R	36-VQFN	X	X	X	X		X	X	X	X	X

A system-level block diagram is shown in Figure 1-1.

FIGURE 1-1: LAN8770 SYSTEM-LEVEL BLOCK DIAGRAM

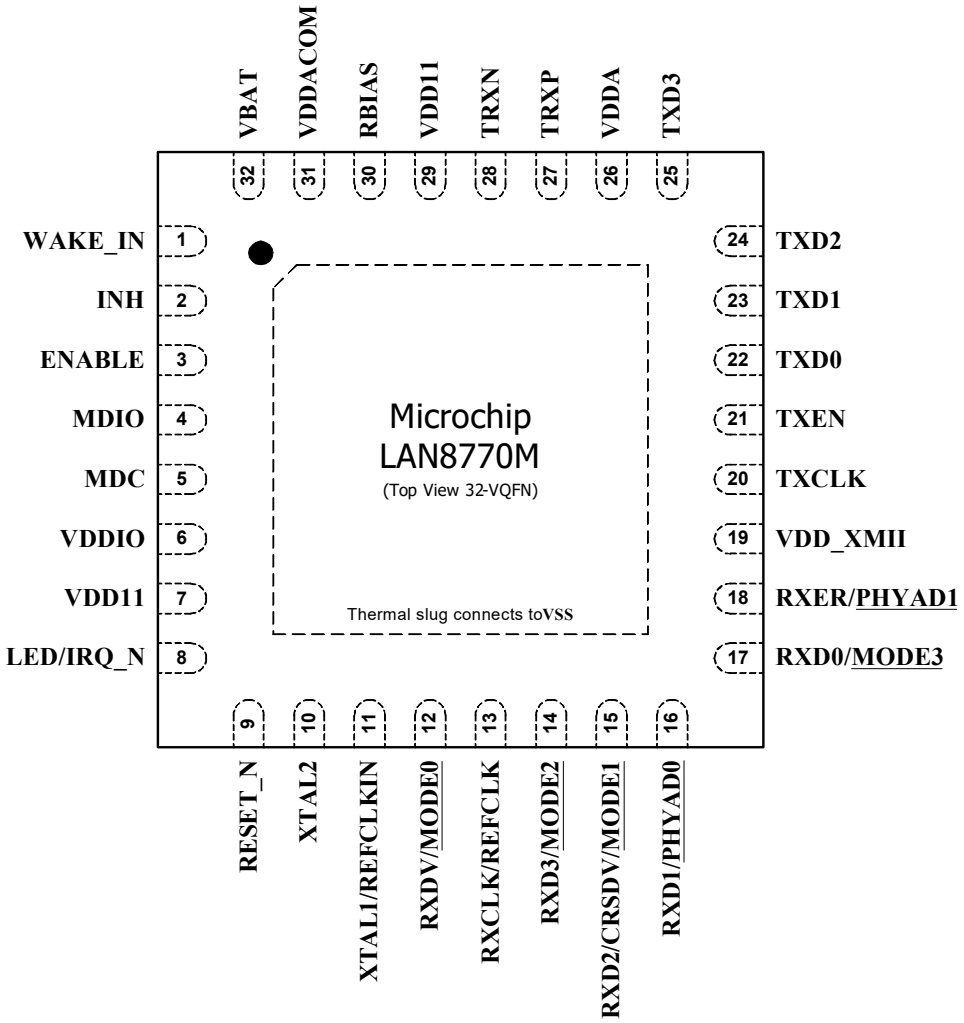


2.0 PIN DESCRIPTIONS

The pin assignments for the LAN8770M are detailed in Section 2.1, LAN8770M Pin Assignments. The pin assignments for LAN8770R are detailed in Section 2.2, LAN8770R Pin Assignments. Pin descriptions are provided in Section 2.3, Pin Descriptions.

2.1 LAN8770M Pin Assignments

FIGURE 2-1: LAN8770M 32-VQFN PIN ASSIGNMENTS



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

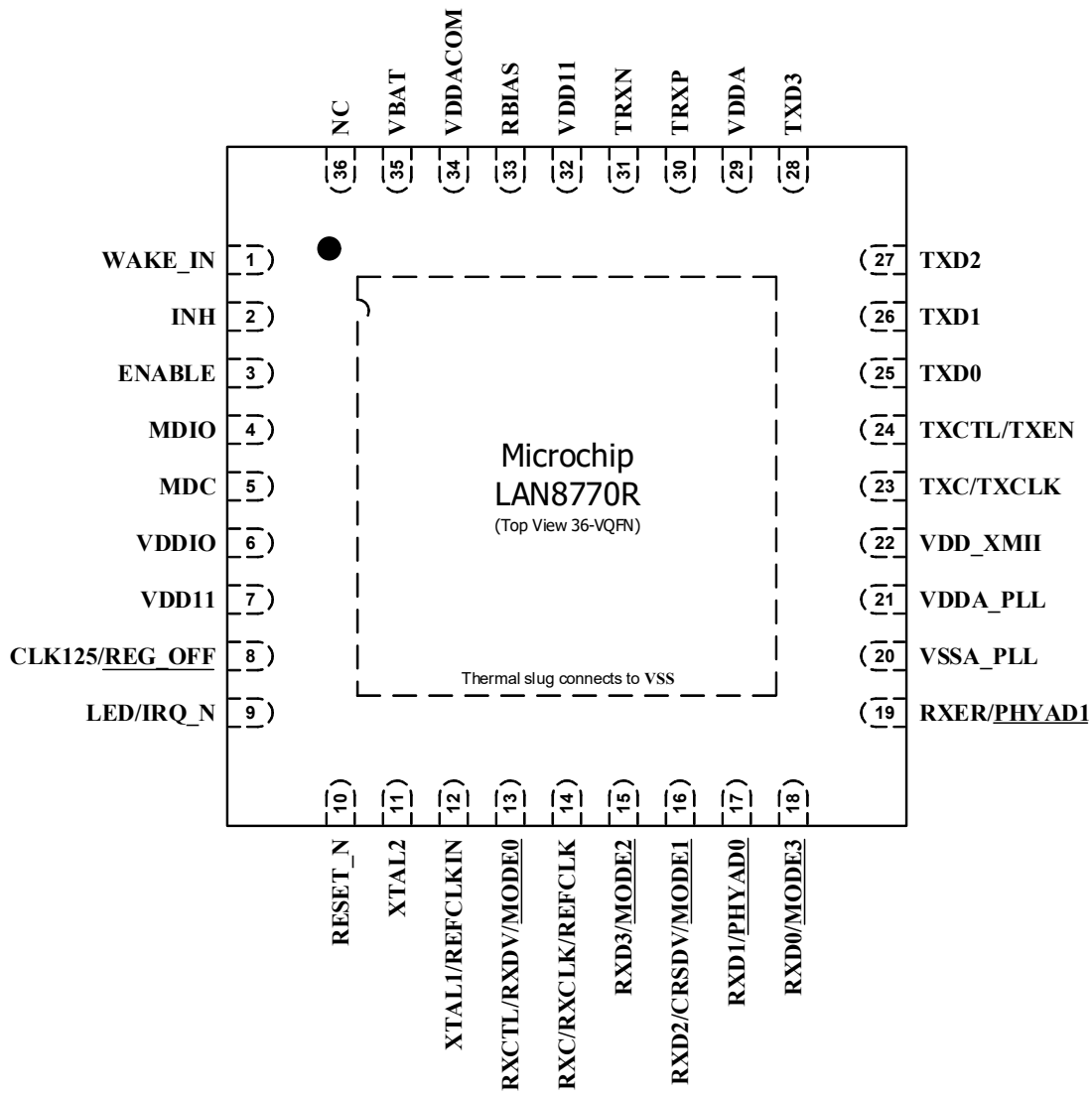
Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 2-1: LAN8770M 32-VQFN PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	**WAKE_IN**	17	**RXD0/MODE3**
2	**INH**	18	**RXER/PHYAD1**
3	**ENABLE**	19	**VDD_XMII**
4	**MDIO**	20	**TXCLK**
5	**MDC**	21	**TXEN**
6	**VDDIO**	22	**TXD0**
7	**VDD11**	23	**TXD1**
8	**LED/IRQ_N**	24	**TXD2**
9	**RESET_N**	25	**TXD3**
10	**XTAL2**	26	**VDDA**
11	**XTAL1/REFCLKIN**	27	**TRXP**
12	**RXDV/MODE0**	28	**TRXN**
13	**RXCLK/REFCLK**	29	**VDD11**
14	**RXD3/MODE2**	30	**RBIAS**
15	**RXD2/CRSDV/MODE1**	31	**VDDACOM**
16	**RXD1/PHYAD0**	32	**VBAT**
Exposed Pad (**VSS**) must be connected to ground.			

2.2 LAN8770R Pin Assignments

FIGURE 2-2: LAN8770R 36-VQFN PIN ASSIGNMENTS



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 2-2: LAN8770R 36-VQFN PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	WAKE_IN	19	RXER/PHYAD1
2	INH	20	VSSA_PLL
3	ENABLE	21	VDDA_PLL
4	MDIO	22	VDD_XMII
5	MDC	23	TXC/TXCLK
6	VDDIO	24	TXCTL/TXEN
7	VDD11	25	TXD0
8	CLK125/REG_OFF	26	TXD1
9	LED/IRQ_N	27	TXD2
10	RESET_N	28	TXD3
11	XTAL2	29	VDDA
12	XTAL1/REFCLKIN	30	TRXP
13	RXCTL/RXDV/MODE0	31	TRXN
14	RXC/RXCLK/REFCLK	32	VDD11
15	RXD3/MODE2	33	RBIAS
16	RXD2/CRSDV/MODE1	34	VDDACOM
17	RXD1/PHYAD0	35	VBAT
18	RXD0/MODE3	36	NC
Exposed Pad (VSS) must be connected to ground.			

2.3 Pin Descriptions

This section contains descriptions of the various LAN8770 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 2-3: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
MII/RMII/RGMII Signals			
Transmit Data 0	**TXD0**	VIS-VDD_XMII	Transmit data bus bit 0 (all modes)
Transmit Data 1	**TXD1**	VIS-VDD_XMII	Transmit data bus bit 1 (all modes)
Transmit Data 2 (MII/RGMII Modes)	**TXD2**	VIS-VDD_XMII	Transmit data bus bit 2 (MII/RGMII modes) **Note:** In RMII mode, this signal is not used and must be grounded.
Transmit Data 3 (MII/RGMII Modes)	**TXD3**	VIS-VDD_XMII	Transmit data bus bit 3 (MII/RGMII modes) **Note:** In RMII mode, this signal is not used and must be grounded.
Transmit Enable (MII/RMII Modes)	**TXEN**	VIS-VDD_XMII	Indicates that valid transmission data is present on **TXD[3:0]**. In RMII mode, only **TXD[1:0]** provide valid data. **Note:** When the LAN8770R is in RGMII mode, the TXEN and TXER functions are combined into the **TXCTL** pin.
Transmit Clock (MII Mode)	**TXCLK**	VO-VDD_XMII	25MHz clock used to latch data from the MAC into the transceiver. **Note:** This signal is not used in RMII mode.
Receive Data 0	**RXD0**	VO-VDD_XMII	Receive data bus bit 0 (all modes)
Receive Data 1	**RXD1**	VO-VDD_XMII	Receive data bus bit 1 (all modes)
Receive Data 2 (MII/RGMII Modes)	**RXD2**	VO-VDD_XMII	Receive data bus bit 2 (MII/RGMII modes) **Note:** This signal is not used in RMII mode.
Receive Data 3 (MII/RGMII Modes)	**RXD3**	VO-VDD_XMII	Receive data bus bit 3 (MII/RGMII modes) **Note:** This signal is not used in RMII mode.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Receive Error (MII/RMII Modes)	**RXER**	VO-VDD_XMII	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver. **Note:** This signal is optional in RMII mode. **Note:** When the LAN8770R is in RGMII mode, the RXDV and RXER functions are combined into the **RXCTL** pin.
Receive Data Valid (MII Mode)	**RXDV**	VO-VDD_XMII	Indicates that recovered and decoded data is available on the **RXD[3:0]** pins. **Note:** When the LAN8770R is in RGMII mode, the RXDV and RXER functions are combined into the **RXCTL** pin.
Receive Clock (MII Mode)	**RXCLK**	VO-VDD_XMII	In MII mode, this pin is the 25MHz receive clock output.
Reference Clock (RMII Mode)	**REFCLK**	VO-VDD_XMII	50MHz RMII reference clock output.
Carrier Sense / Receive Data Valid (RMII Mode)	**CRSDV**	VO-VDD_XMII	This signal is asserted to indicate the receive medium is non-idle in RMII mode.
Transmit Clock (RGMII Mode)	**TXC**	VIS-VDD_XMII	25MHz clock used to latch data from the MAC into the PHY. **Note:** This pin is available in the LAN8770R only.
Transmit Control (RGMII Mode)	**TXCTL**	VIS-VDD_XMII	Indicates both the transmit data enable (TXEN) and transmit error (TXER) functions per the RGMII specification. Indicates the presence of valid transmit data and control signals. **Note:** This pin is available in the LAN8770R only.
Receive Clock (RGMII Mode)	**RXC**	VO-VDD_XMII	25MHz clock used to transfer data to the MAC. **Note:** This pin is available in the LAN8770R only.
Receive Control (RGMII Mode)	**RXCTL**	VO-VDD_XMII	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification. Indicates the presence of valid receive data and carrier sense. **Note:** This pin is available in the LAN8770R only.
125MHz Reference Clock Output (RGMII Mode)	**CLK125**	RGMII	125MHz RGMII reference clock output to the SoC MAC. **Note:** This clock is enabled by default when the device is strapped into RGMII mode. It may be disabled via register settings. **Note:** This pin is available in the LAN8770R only.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet			
Ethernet TX/RX Positive Terminal	**TRXP**	AIO	Positive terminal for transmit/receive signal.
Ethernet TX/RX Negative Terminal	**TRXN**	AIO	Negative terminal for transmit/receive signal.
Serial Management Interface			
SMI Data Input/ Output	**MDIO**	VIS-VDDIO/ VO-VDDIO	Serial Management Interface data input/output.
SMI Clock	**MDC**	VIS-VDDIO	Serial Management Interface clock.
Miscellaneous			
External 25MHz Crystal Input	**XTAL1**	ICLK	External 25MHz crystal input.
External Clock Input	**REFCLKIN**	ICLK	Single-ended clock oscillator input. A frequency of 25MHz should be used in all modes except RMII, which requires 50MHz. **Note:** When using a single-ended clock oscillator, **XTAL2** should be left unconnected. **Note:** This input is 3.3V tolerant, but any input must meet the V_{IH} and V_{IL} parameters for the ICLK buffer type.
External 25MHz Crystal Output	**XTAL2**	OCLK	External 25MHz crystal output.
Enable	**ENABLE**	AI	Enable. When asserted, the part is enabled. If this pin is driven low then the part is placed into its lowest power consuming state (DISABLE). **Note:** This pin must remain high during Sleep mode. If an external pull-up is used for this pin, pull up to **VBAT**, not **VDDIO**.
Inhibit	**INH**	VO-VBAT	Inhibit. Used to switch on/off the main external power supply unit. **INH** drives high during normal operation to enable the external power supply. It is high-Z during the sleep state to switch off the external power supply. Inhibit means inhibit shutdown of the external power supply. **Note:** This pin operates off of **VBAT** domain. **Note:** **RESET_N** assertion does not affect the state of this pin. **Note:** This signal is active high. **Note:** This pin is open-source. An external pull-down to ground is needed.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Wake Input	**WAKE_IN**	VIS-VBAT	Wakeup Input. Asserted to move the part out of sleep. This pin implements the optional wake input described in the TC10 specification. **Note:** This pin operates off of the **VBAT** domain.
LED	**LED**	VOD	LED output. Active low and open-drain. The default function for this pin is IRQ_N.
Interrupt	**IRQ_N**	VOD	Device interrupt. Active low and open drain. **Note:** Float pin when unused.
System Reset	**RESET_N**	VIS-VDDIO	System rest. This pin is active low. **Note:** If unused, this pin must be pulled-up to **VDDIO**.
Reference Resistor	**RBIAS**	AI	Reference resistor connection pin. This pin requires connection of a 6.49KΩ ±0.1% resistor to ground.
No Connect	**NC**	-	No connect. This pin must be left unconnected for proper operation.
Configuration Straps			
Operating Mode Configuration Straps 3-0	**MODE[3:0]**	VIS-VDD_XMII (PD)	These configuration straps are used to select the device's default mode of operation.
PHY Address Configuration Straps 1-0	**PHYAD[1:0]**	VIS-VDD_XMII (PD)	These configuration straps are used to select the device's default PHY address.
Regulator Off Configuration Strap	**REG_OFF**	VIS-VDDIO (PD)	This configuration strap is used to disable the internal 1.1V regulator. **Note:** This configuration strap is available in the LAN8770R only.
Power/Ground			
+1.1V Digital Core Power Supply	**VDD11**	P	+1.1V digital core power supply. Both **VDD11** pins should be connected together with a 1uF capacitor to ground. **Note:** **VDD11** is supplied via the internal voltage regulator when REG_OFF is strapped low for the LAN8770R. When REG_OFF is strapped high, an external +1.1V source is required. For the LAN8770M the internal regulator cannot be disabled.
+1.8V to +3.3V Variable I/O Power Supply Input	**VDDIO**	P	+1.8V to +3.3V variable I/O power supply input.

TABLE 2-3: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+1.8V to +3.3V Variable MII/RMII/RGMII Power Supply Input	**VDD_XMII**	P	+1.8V to +3.3V variable MII/RMII/RGMII power supply input.
+2.5V to +3.3V Variable VBAT Power Supply Input	**VBAT**	P	+2.5V to +3.3V variable VBAT power supply input.
+2.5V to +3.3V Variable T1 AFE Power Supply Input	**VDDA**	P	+2.5V to +3.3V variable T1 Analog Front End (AFE) power supply input.
+2.5V to +3.3V Variable T1 Common Power Supply Input	**VDDACOM**	P	+2.5V to +3.3V variable T1 common power supply input.
+2.5V to +3.3V Variable PLL Power Supply Input	**VDDA_PLL**	P	+2.5V to +3.3V variable PLL power supply input. **Note:** This pin is available in the LAN8770R only.
PLL Ground	**VSSA_PLL**	P	PLL ground. **Note:** This pin is available in the LAN8770R only. **Note:** DO NOT connect this pin to ground on the board. Let it float, and decouple it to **VDDA_PLL** with a 100nF capacitor.
Ground	**VSS**	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

2.4 Buffer Types

TABLE 2-4: LAN8770 BUFFER TYPE DESCRIPTIONS

BUFFER	DESCRIPTION
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin
PU	70K (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	70K (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
RGMII	RGMII reference clock output pin
VIS-VDDIO	Variable voltage Schmitt-triggered input (**VDDIO** power domain)
VIS-VDD_XMII	Variable voltage Schmitt-triggered input (**VDD_XMII** power domain)
VIS-VBAT	Variable voltage Schmitt-triggered input (**VBAT** power domain)
VO-VDDIO	Variable voltage output with 2/4/8/10 mA sink and 2/4/8/10 mA source (**VDDIO** power domain)
VO-VDD_XMII	Variable voltage output with 2/4/8/10 mA sink and 2/4/8/10 mA source (**VDD_XMII** power domain)
VO-VBAT	Variable voltage output with 2/4/8/10 mA sink and 2/4/8/10 mA source (**VBAT** power domain)
VOD	Variable open-drain output

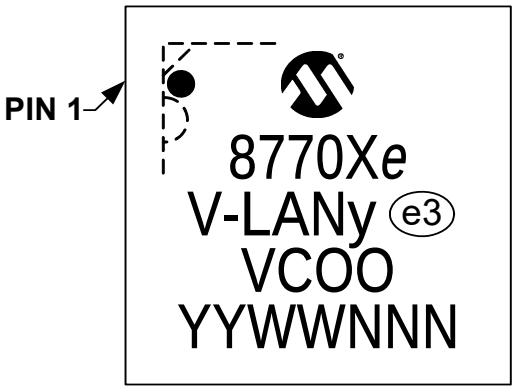
Note: Digital signals are not 5V tolerant unless specified.

Note: Sink and source capabilities are dependent on the supplied voltage.

3.0 PACKAGE INFORMATION

3.1 Top Marking

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.



Legend:	X	"R" for LAN8770R (36-QFN), "M" for LAN8770M (32-QFN)
	e	Temperature range designator
	y	Product revision
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	V	Plant of assembly
	COO	Country of origin
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

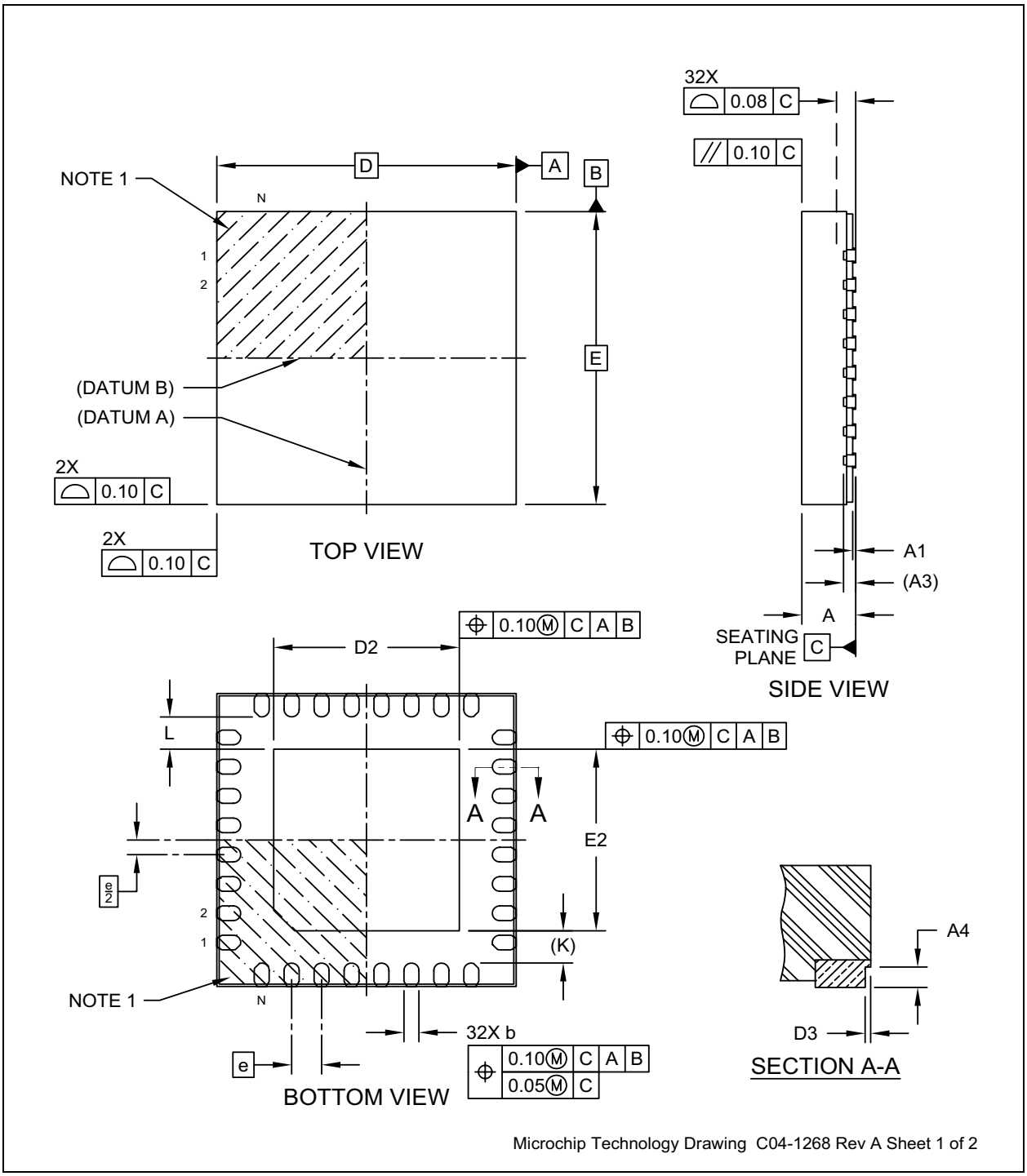
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

3.2 32-VQFN (LAN8770M Only)

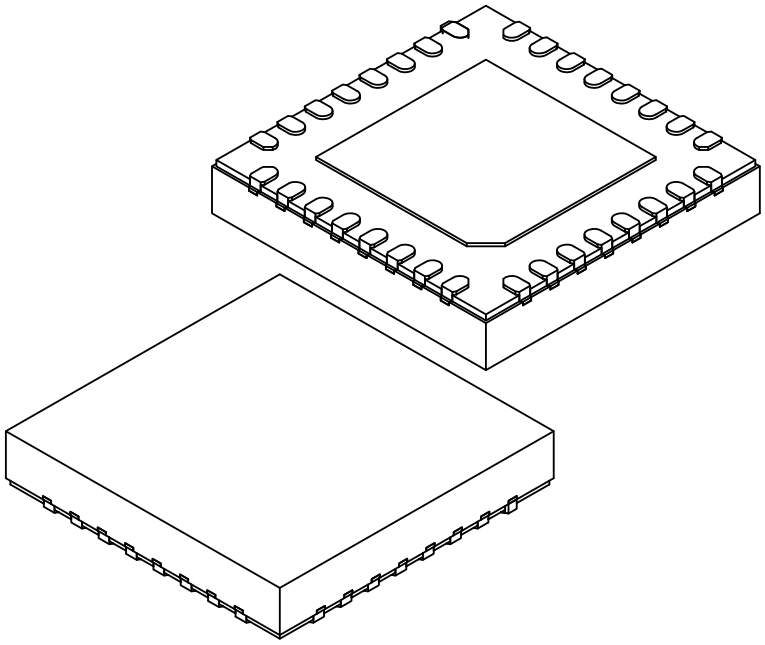
Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 3-1: 32-VQFN PACKAGE (DRAWING)



Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 3-2: 32-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.00	3.10	3.20
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.00	3.10	3.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.55 REF	
Step Height	A4	0.10	0.125	0.15
Step Length	D3	-	-	0.04

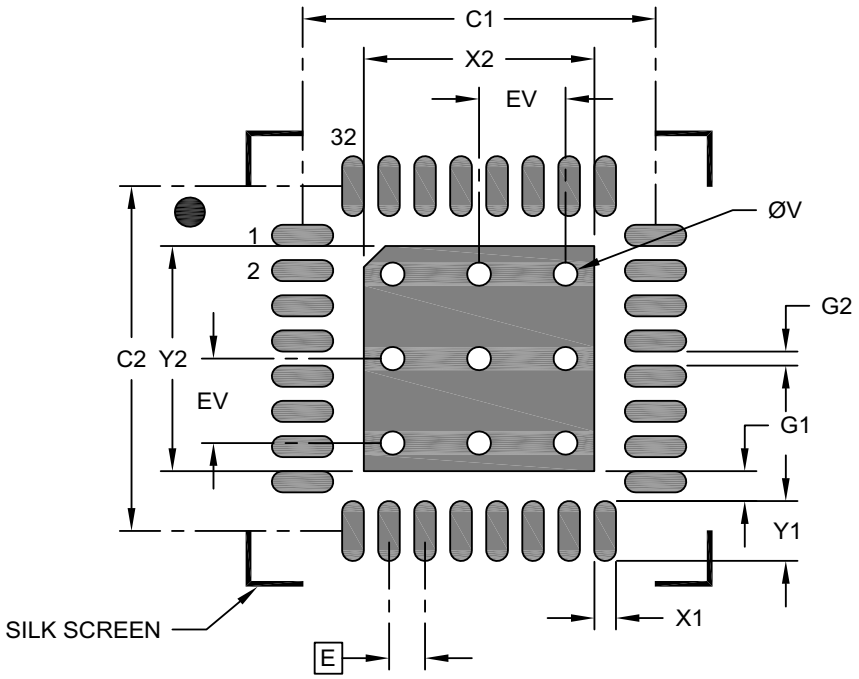
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1268 Rev A Sheet 2 of 2

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 3-3: 32-VQFN PACKAGE (LAND-PATTERN)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			3.20
Optional Center Pad Length	Y2			3.20
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.43		
Contact Pad to Center Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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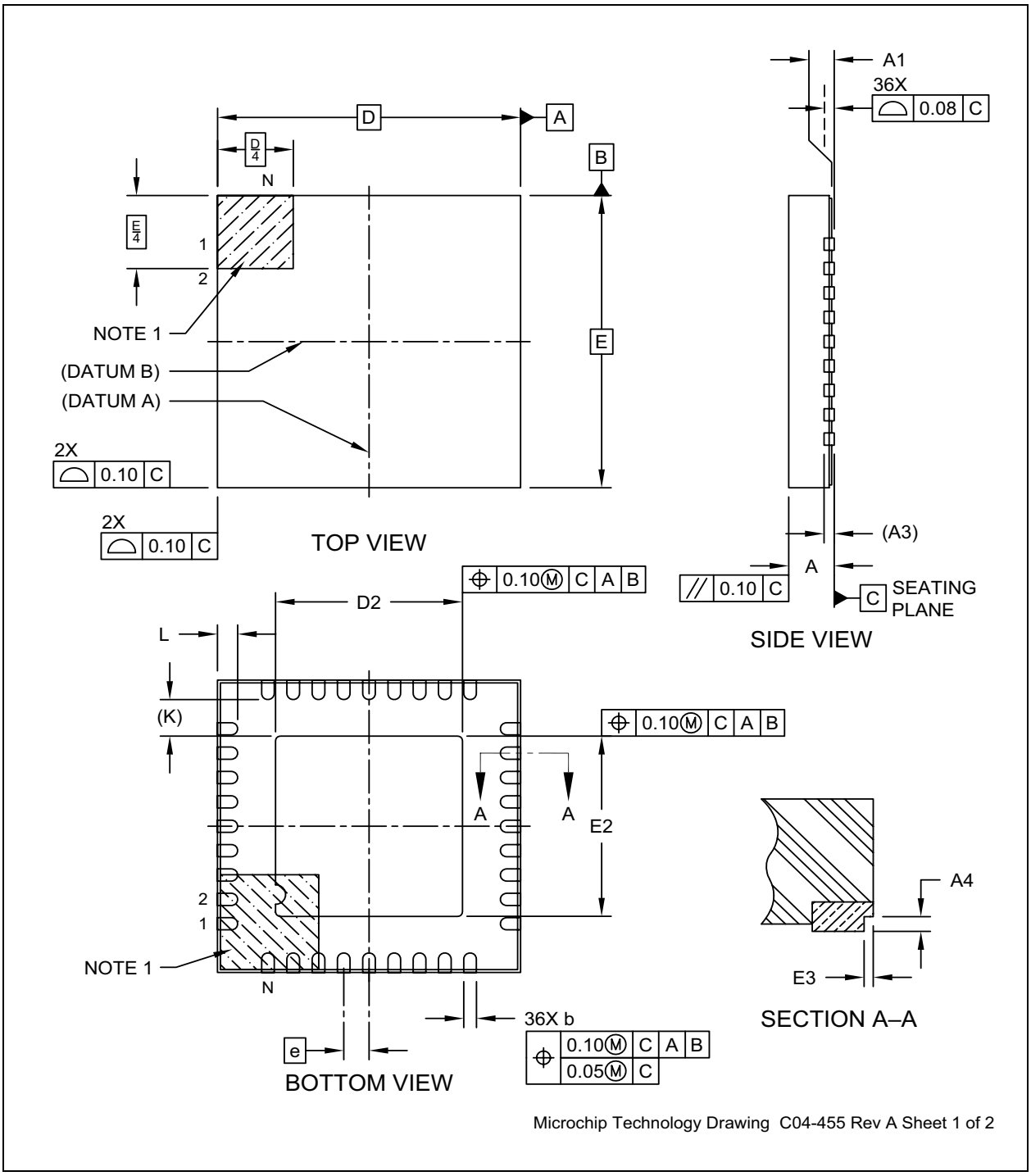
3.3 36-VQFN (LAN8770R Only)

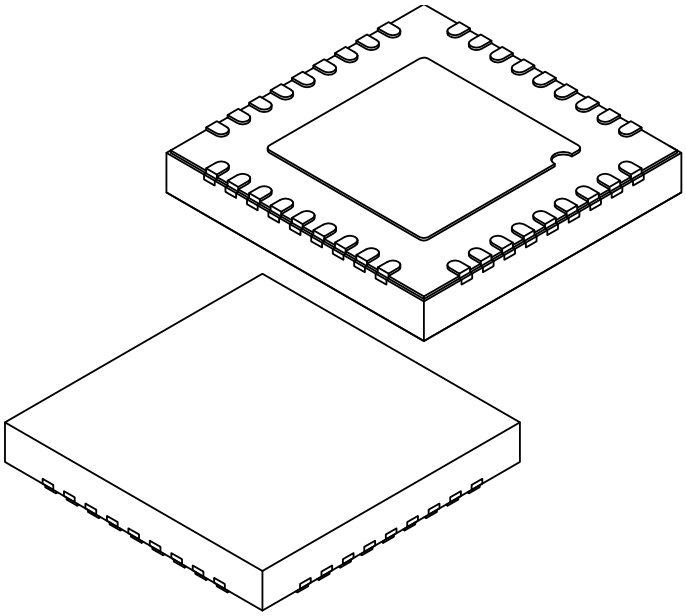
Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 3-4: 36-VQFN PACKAGE (DRAWING)



Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 3-5: 36-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.75 REF	
Wettable Flank Step Cut Depth	A4	0.10	0.125	0.15
Wettable Flank Step Cut Width	E3	-	-	0.04

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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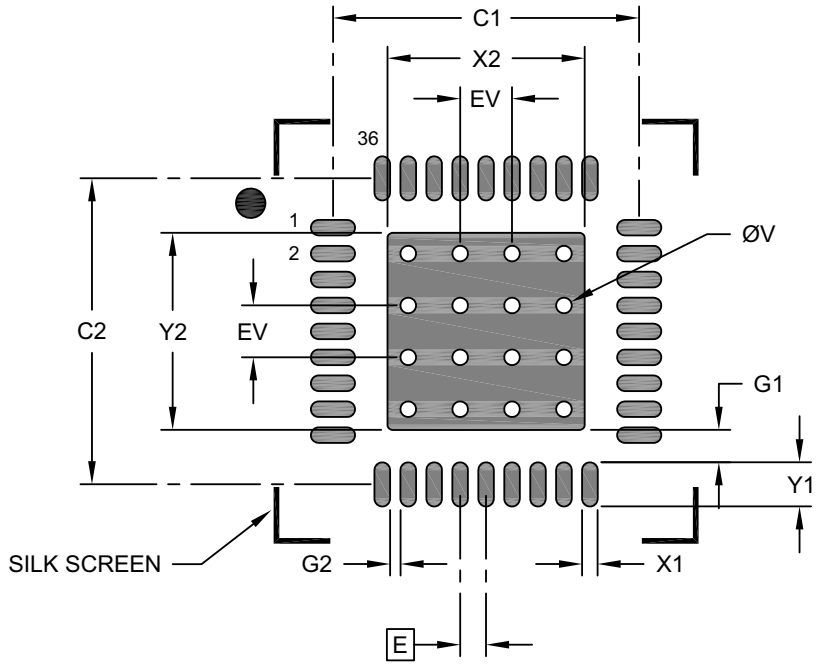
Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 3-6: 36-VQFN PACKAGE (LAND-PATTERN)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			0.85
Contact Pad to Center Pad (X36)	G1	0.20		
Contact Pad to Contact Pad (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

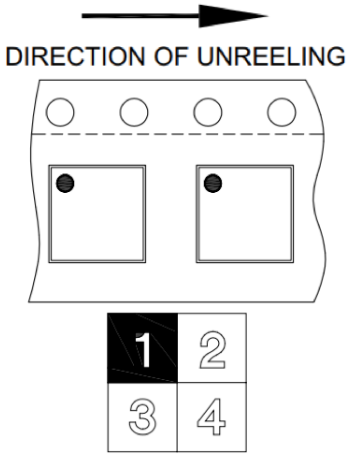
Revision Level & Date	Section/Figure/Entry	Correction
DS00002550C (07-14-20)	Features	“Microchip Functional Safety Ready” - added to Highlights and Key Benefits “LinkMD” feature removed from Highlights
	Section 1.0, Introduction	Mention of “LinkMD” removed
DS00002550B (04-15-20)	Public Release	
DS00002550A (09-20-17)	All	Initial Release

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX	XXX
Device	Tape and Reel Option		Temperature Range		Package	Automotive Code

Device:	LAN8770M = MII/RMII Interface LAN8770R = MII/RMII/RGMII Interface	
Tape and Reel Option:	Blank = Standard packaging (tray) T = Tape and Reel(Note 1)	
Temperature Range:	E = -40°C to +125°C	(AEC-Q100 Grade 1 Automotive)
Package:	PRA = 32-pin VQFN (LAN8770M only) 5KX = 36-pin VQFN (LAN8770R only)	
Automotive Code:	Vxx = 3 character code with “V” prefix, specifying automotive product.	



Examples:

a) LAN8770M-E/PRAVAO
Tray, -40°C to +125°C, 32-pin VQFN

b) LAN8770MT-E/PRAVAO
Tape & reel, -40°C to +125°C, 32-pin VQFN

c) LAN8770R-E/5KXVAO
Tray, -40°C to +125°C, 36-pin VQFN

d) LAN8770RT-E/5KXVAO
Tape & reel, -40°C to +125°C, 36-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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