HVP-56F80748-UM

HVP-56F80748 Board User Manual

Rev. 0 — 13 December 2022 **User manual**

Document information

Information	Content
Keywords	MC56F80748, MC56F80xxx, high-voltage platform, motor control, digital power
Abstract	This document describes the features and functional description of the HVP-56F80748 controller card, which is a development platform for the DSC 56F8xxxx family.

1 Overview

The NXP high-voltage development platform is a set of software and hardware tools for the evaluation and development of high-voltage motor control and power conversion algorithms. NXP designed this platform for the rapid prototyping of high-voltage microcontroller-based applications.

The HVP-56F80748 controller card is a development platform for the DSC 56F8xxxx family, which in combination with HVP-MC3PH high-voltage development platform provides ready-made software and hardware development for high-voltage motor control and power conversion applications. In addition, HVP controller card is also compatible with the NXP totem-pole bridgeless PFC converter and LLC resonant converter with synchronous rectifier boards.

1.1 Acronyms and abbreviations

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Term	Description
ADC	Analog-to-digital converter
CMP	Comparator
DSC	Digital signal controller
EMI	Electromagnetic interference
GPIO	General-purpose input/output
HVP	High-voltage development platform
JTAG	Joint test access group
MCU	Microcontroller unit
OPAMP	Operational amplifier
PFC	Power factor correction
PWM	Pulse width modulation
SDK	Software development kit
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
VCP	Virtual COM port

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on the board. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document	Description	Link / how to access
MC56F80xxx Reference Manual	Intended for system software and hardware developers and applications programmers who want to develop products with this device.	MC56F80XXXRM
MC56F80xxx Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	MC56F80XXX
MCUXpresso Software Development Kit (SDK) documentation	The MCUXpresso SDK is a comprehensive software enablement package designed to simplify and accelerate application development with NXP MCUs	mcuxpresso.nxp.com

1.3 Board kit contents

The table below lists the items included in the HVP-56F80748 board kit.

Table 3. Board kit contents

Item description	Quantity
HVP-56F80748 board hardware assembly	1
HVP-56F80748 Quick Start Guide	1

1.4 Block diagram

The figure below shows the HVP-56F80748 block diagram.

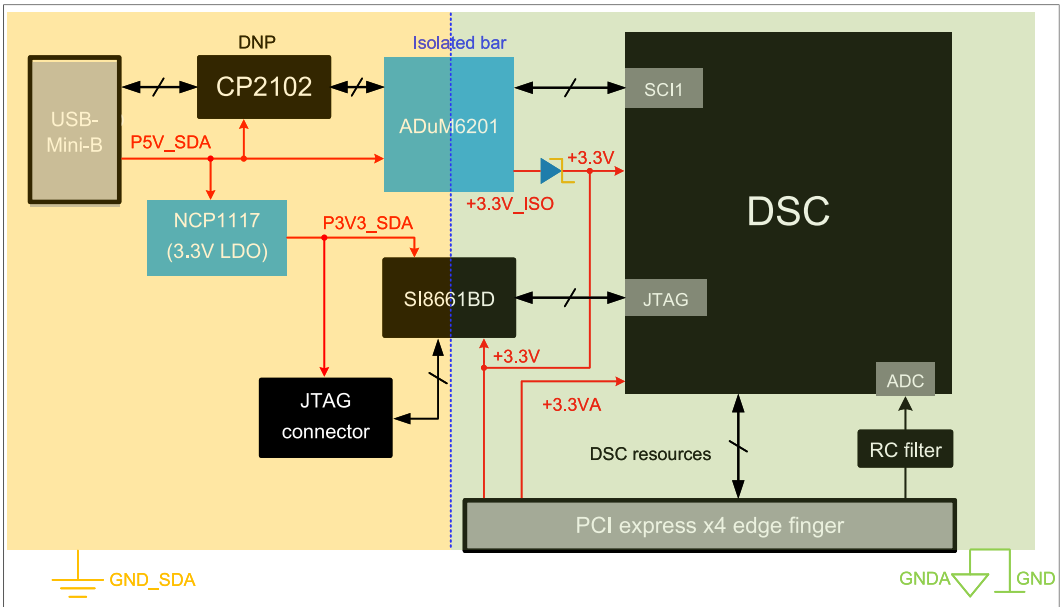


Figure 1. HVP-56F80748 block diagram

1.5 Board features

The table below describes the features of the HVP-56F80748 board.

Table 4. HVP-56F80748 features

HVP-56F80748 feature	Target MCU feature used	Description
MC56F80748 DSC		The processor is based on 32-bit 56800EF core of up to 100 MIPS at 100 MHz core frequency Note: For details on the MC56F80748 DSC, refer to *MC56F80XXX Reference Manual*.
Power supply		• 5 V (P5V_SDA) input power supply from USB-Mini-B connector (J2) • +3.3 V power supply for DSC digital circuits from one of the following: – PCI Express connector (J3) from the compatible board – +3.3V_ISO from the ADuM6201 • +3.3VA power supply for DSC analog circuits from PCI Express connector (J3) • P3V3_SDA power supply from 3V3 regulator NCP1117ST33T3G (U4) for the following: – JTAG connector (J1) – Side 1 of Si8661BD (U2, lower-power six-channel digital isolator)
Isolated program and debug interface		JTAG connector (J1) to program and debug MC56F80748
Isolated virtual COM port (VCP)		• USB-to-UART device (CP2102N) (Not populated by default) – Provides an isolated virtual serial port through USB connector (J2), which uses QSCI1 in MC56F80748
PCI Express connector		The edge finger is used to connect with power stage, such as HVP-MC3PH
RC filter circuit	High-speed analog-to-digital converter (ADC)	Provide low-pass filters between the sampled analog signals from PCI Express connector pins and ADC input pins
LED		• Two LEDs are used to indicate the power state • One user LED
PCB		HVP-56F80748: 86.6 mm × 40.3 mm, 2 layer
Orderable part number		HVP-56F80748

1.6 Board picture

The figure below shows the top-side view of the HVP-56F80748 with connectors, LEDs, and key chips highlighted.

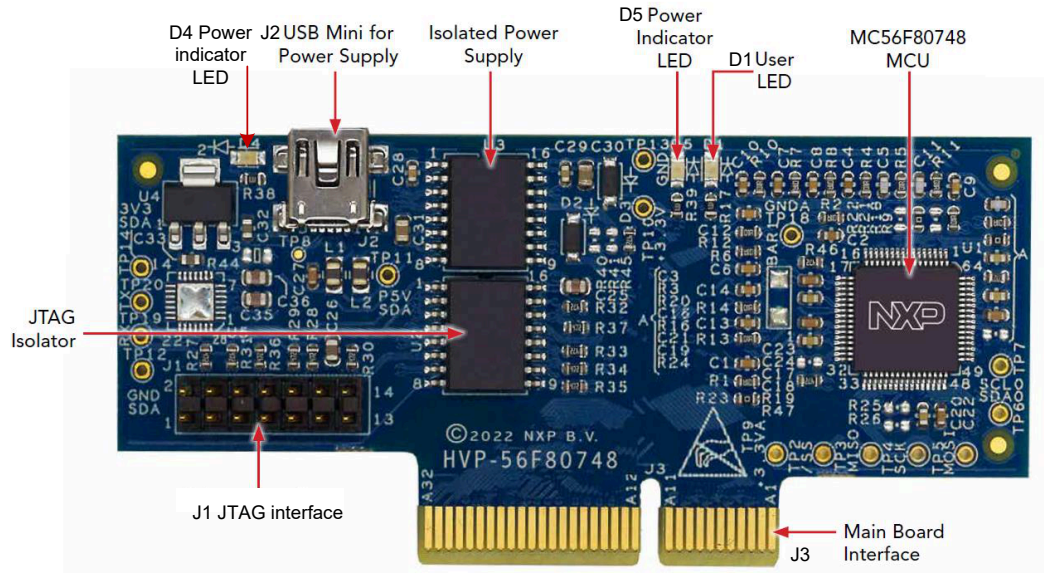


Figure 2. HVP-56F80748 top view

1.7 Connectors

The following table describes the onboard connectors. Figure 2 highlights the connectors location on the board.

Table 5. HVP-56F80748 connectors

Part identifier	Connector type	Description	Reference section
J1	2x7 connector	JTAG connector to program and debug the MC56F80748 DSC.	Section 2.4
J2	USB-Mini-B connector	USB connector for USB-to-UART CP210x device, which provides an isolated virtual serial port. Also, used as an external 5 V power connector. ***Note:*** *CP210x USB-to-UART bridge VCP drivers are needed. CP210x is NOT populated by default on the board.*	Section 2.2
J3	PCI Express connector	I/O interfaces compatible with the power stage boards (mother boards)	Input/output headers

1.8 LEDs

The following table describes the onboard LEDs. Figure 2 highlights the LEDs location on the board.

Table 6. HVP-56F80748 LEDs

Part identifier	LED color	LED name	Description
D1	RED	USER LED	User-programmable LED connected with GPIOC1. A high level turns on the LED.

Table 6. HVP-56F80748 LEDs*...continued*

Part identifier	LED color	LED name	Description
D4	GREEN	LED INDICATOR ISOLATED	Indicates that P3V3_SDA (3.3 V) supply is available
D5	GREEN	LED INDICATOR NON-ISOLATED	Indicates that +3.3V (3.3 V) supply is available

2 HVP-56F80748 functional description

This chapter describes the features and functions of the HVP-56F80748 board. For details of the MC56F80748 MCU features, see *MC56F80xxx Reference Manual*.

2.1 Power supplies

The HVP-56F80748 board can be powered in two ways, which is shown in Section 1.4.

- Through USB-Mini-B connector J2. The 5 V input voltage (P5V_SDA) from the USB connector powers the CP2102N (USB-to-UART bridge controller), NCP1117 (5 V to 3.3 V voltage regulator), and ADuM6201 (Isolators with integrated DC-to-DC converter).
  - The converted P3V3_SDA (3.3 V) from NCP1117 shares the same ground (GND_SDA) with USB connector. It gives power to side 1 of Si8661BD (six-channel digital isolator) and JTAG connector.
  - The converted +3.3V_ISO (3.3 V) from ADuM6201is an isolated power source which shares the same ground (GND) with DSC 56F80748. This isolated +3.3V_ISO is used to power the digital circuits of the DSC through diode D3 as well as side 2 of Si8661BD.
- Through PCI Express connector J3. When the HVP-56F80748 card is plugged into a mother board, such as HVP-MC3PH, both the digital and analog circuits inside DSC are powered up through +3.3V and +3.3VA that come from the PCI Express connector.

Note:

- *When HVP-56F80748 is not plugged into a mother board, it can only be powered through the USB connector, and only the digital circuit inside DSC is powered up. Therefore, the analog part (example, ADC) of the DSC would not work properly in this case.*
- *When HVP-56F80748 is plugged into a mother board and the mother board is also powered up, both the digital and analog circuits of MC56F80748 are powered up through +3.3V and +3.3VA from J3 connector.*
- *HVP-56F80748 can be powered through USB connector J2 and PCI Express connector J3 at the same time. A diode D3 is placed between +3.3V_ISO and +3.3V to mitigate the conflict.*
- *Always provide power input from USB connector J2 when you want to program DSC through JTAG connector, because pin 11 of JTAG connector comes from P3V3_SDA which is originated from USB connector.*

The table below provides power supply details of the HVP-56F80748 board.

Table 7. Power supplies

Part identifier	Device/ Power source	Power supply rail	Description
J2	USB-Mini-B connector providing 5 V power supply	P5V_SDA	• Power supply for CP2102N (USB-to-UART bridge controllers) • Power supply for NCP1117(5 V to 3.3 V voltage regulator) • Power supply for ADuM6201(Isolators with integrated DC-to-DC converter)
U4	NCP1117	P3V3_SDA	• Power supply for side 1 of the SI8661BD (six-channel digital isolator) • Power supply for JTAG interface
U3	ADuM6201	+3.3V_ISO	Source of the +3.3V
D3	MBR120VLSFT1G	+3.3V	• Power supply for digital circuits of the DSC • Power supply for side 2 of the SI8661BD
J3	PCIe connector		
J3	PCIe connector	+3.3VA	Power supply for analog circuits of the DSC

2.2 Isolated USB-to-UART interface

The HVP-56F80748 board supports an isolated USB-to-UART function through CP2102N and ADuM6201. CP2102N is not populated by default.

CP2102N provides a virtual COM interface between the host computer and MC56F80748 through USB port (J2) by using SCI1 on MC56F80748. It includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, and universal asynchronous receiver/ transmitter (UART) in a small package.

Note:

CP2102N device requires installing the VCP device drivers that can be downloaded from https://www.silabs.com/developers/usb-to-uart-bridge-vcp-drivers?tab=downloads. After the driver for CP2102N is installed, the host computer will enumerate COM ports when the USB cable is plugged into the J2 USB port. This makes the device appear as a VCP. You can use these ports to communicate with the processor with USB interface via a standard PC serial emulation port (for example, Putty and Tera Term).

The following figure shows the circuit diagram of CP2102N USB-to-UART device using SCI1 interface.

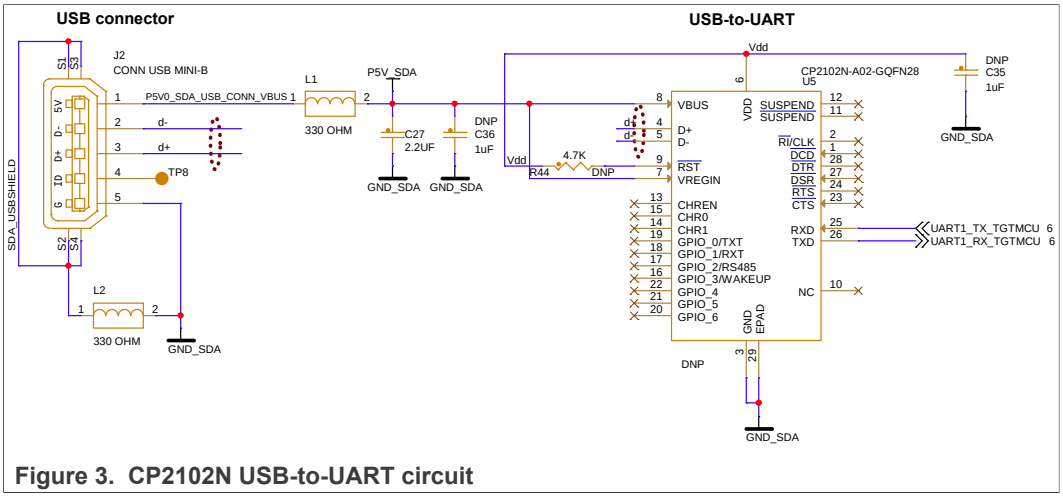
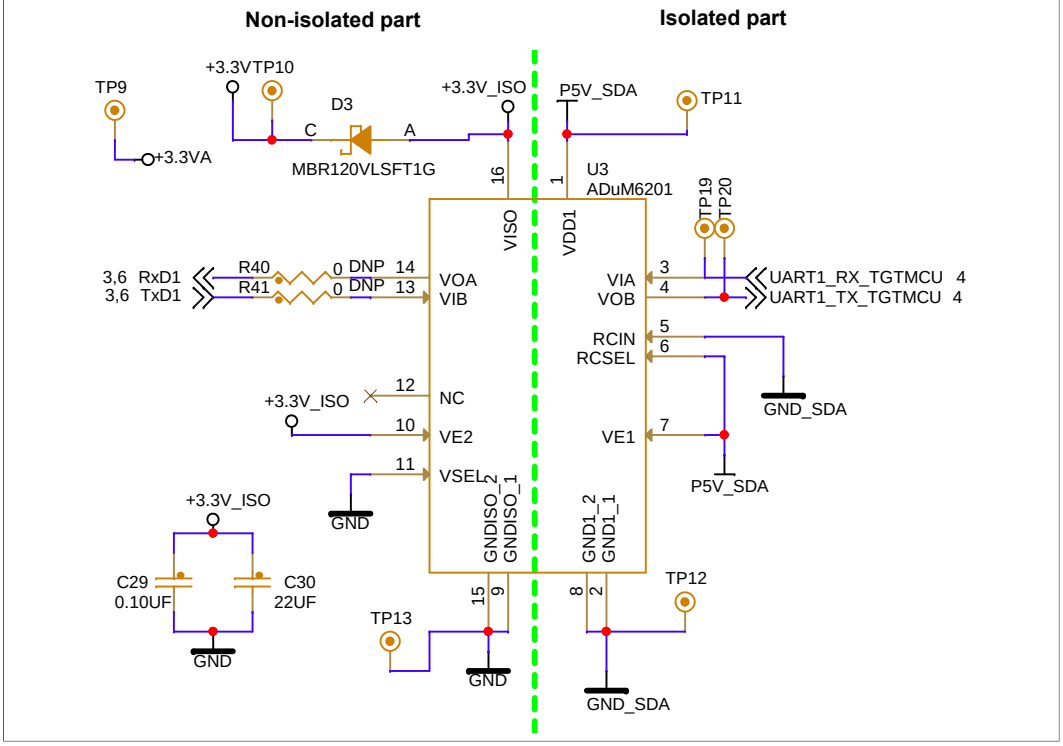


Figure 3. CP2102N USB-to-UART circuit

The motor control and power conversion are high voltage and high EMI applications. To ensure the safety and reliable communication, the connection between the host computer and the DSC is isolated. ADuM6201(U3) is used to isolate the RXD and TXD signals of DSC from the host.

The following figure shows the USB-to-UART isolated circuit.

Figure 4. USB-to-UART isolated circuit



The following table describes the connection of the SCI signals.

Table 8. USB-to-UART pin connection

CP2102N side		DSC side		Description
CP2102N pin	ADuM6201 pin	ADuM6201 pin	MC56F80748 pin	
RXD	VOB	VIB	GPIOC11 (TXD1)	QSCI1 transmit data output on DSC
TXD	VIA	VOA	GPIOC12 (RXD1)	QSCI1 receive data input on DSC

Note:

Even though this virtual serial communication circuit is not available by default, the TXD and RXD signals of QSCI0 in DSC 56F80748 are routed to the mother board through PCI Express connector, which can also be used to realize isolated USB-to-UART communication together with the HVP-MC3PH board.

2.3 Input/output headers

The HVP-56F80748 daughter card is compatible with the mother boards through the PCI Express connector. The mother board can be any of the following:

- HVP-MC3PH
- Totem-Pole Bridgeless PFC Converter
- LLC Resonant Converter with Sync Rectifier

Peripheral pins of DSC such as PWM, ADC, OPAMP, and CMP are connected to the PCI Express connector for the development of the motor control and power conversion applications.

The following table describes the HVP-56F80748 PCI Express connector pinout.

Table 9. PCI Express connector pinout

Pin	Signal	DSC GPIO mapping	Pin	Signal	DSC GPIO mapping
B1	-	-	A1	+3.3VA	
B2	GNDA	-	A2	GNDA	
B3	AN0 - I_dcb	GPIOB3, GPIOA5	A3	AN1 - I_phA	GPIOA1
B4	AN2 - U_dcb	GPIOA3	A4	AN3 - I_phB	GPIOB2
B5	AN4 - U_dcb/2	GPIOB1	A5	AN5 - I_phC	GPIOB7, GPIOA6
B6	AN6 - BEMF_A	GPIOA0	A6	AN7 – TACHO	GPIOA2
B7	AN8 - BEMF_B	GPIOA4	A7	AN9 - V_in	GPIOB4
B8	AN10 - BEMF_C	GPIOA7, optional connected to GPIOB0	A8	AN11 - I_pfc1	GPIOB5
B9	AN12 - Temp_ IPM	GPIOB0, optional connected to GPIOA5	A9	AN13 - I_pfc2	GPIOB6
B10	-	-	A10	-	-
B11	GNDA	-	A11	GNDA	-

Table 9. PCI Express connector pinout*...continued*

Pin	Signal	DSC GPIO mapping	Pin	Signal	DSC GPIO mapping
B12	+3.3V	-	A12	-	-
B13	GND	-	A13	GND	-
B14	TM0	GPIOC4	A14	PWM0	GPIOE1
B15	TM1	GPIOC5	A15	PWM1	GPIOE0
B16	TM2	GPIOC13	A16	PWM2	GPIOE3
B17	MB_TP_29	GPIOC15	A17	PWM3	GPIOE2
B18	-	-	A18	PWM4	GPIOE5
B19	-	-	A19	PWM5	GPIOE4
B20	USER_LED	GPIOC0	A20	-	
B21	MB_TP_27/ MISO	GPIOC8	A21	-	
B22	MB_TP_26/ MOSI	GPIOC10	A22	PWM8	GPIOE6
B23	SCK	GPIOC9	A23	PWM9	GPIOE7
B24	/SS	GPIOC7	A24	GND	-
B25	MCU_BRAKE	GPIOF0	A25	FAULT_1	GPIOF6
B26	TxD	GPIOC2	A26	FAULT_2	GPIOF7
B27	RxD	GPIOC3	A27	-	-
B28	Relay	GPIOF1	A28	-	-
B29	-	-	A29	MB_TP_24	GPIOF2, optional connected to GPIOF5
B30	-	-	A30	MB_TP_22	GPIOF3, optional connected to GPIOF4
B31	-	-	A31	TxD1	GPIOC11
B32	GND	-	A32	RxD1	GPIOC12

2.4 Isolated debug interface

The MC56F80748 processor has five GPIO pins multiplexed with the four JTAG signals and one reset signal:

- RESETB input (default signal on GPIOD4 pin)
- TMS input (default signal on GPIOD3 pin)
- TCK input (default signal on GPIOD2 pin)
- TDO output (default signal on GPIOD1 pin)
- TDI input (default signal on GPIOD0 pin)

The GPIOD[4:0] signals are connected on the HVP-56F80748 board to the 14-pin JTAG connector (J1) through a six-channel digital isolator SI8661BD. A standalone debug tool is needed to program and debug HVP-56F80748 board, such as Multilink development interface, and power P5V_SDA must be provided through USB connector J2.

The following table describes the JTAG header pinout.

Table 10. JTAG header (J1) pinout

Pin number	Signal name	Description
1	GPIOD0/TDI	TAP data In
2	GND_SDA	Ground
3	GPIOD1/TDO	TAP data out
4	GND_SDA	Ground
5	GPIOD2/TCK	TAP clock
6	GND_SDA	Ground
7	-	Not connected
8	-	Not connected
9	GPIOD4/RESET	Reset signal
10	GPIOD3/TMS	TAP machine state
11	P3V3_SDA	Power supply
12	-	Not connected
13	-	Not connected
14	-	Not connected

Similar to the USB-to-UART circuit, the Si8661BD is used in debug circuit to isolate the JTAG signals between the host PC and the DSC.

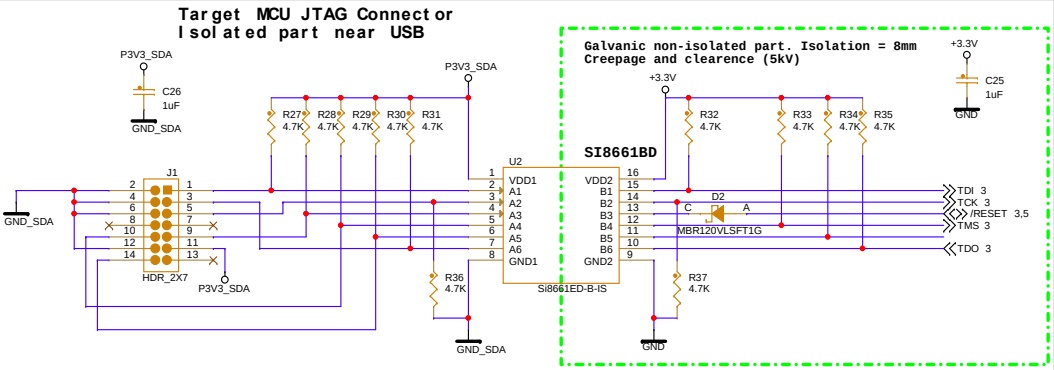


Figure 5. JTAG isolated circuit

3 Revision history

The table below summarizes the revisions to this document.

Revision history

Revision	Date	Description
0	13 December 2022	Initial public release.

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