

iW-RainboW-G55S

AM62Ax

Single Board Computer

Datasheet



AM62Ax based SBC Datasheet

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1. INTRODUCTION

1.1 Purpose

This document is the datasheet for the Single Board Computer based on the TI's AM62Ax Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the AM62Ax SBC from a Hardware Systems perspective.

1.2 SBC Overview

The Compact is a versatile small form factor SBC (Single Board Computer) definition targeting application that require low power, low costs, and high performance. The SBCs are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GbE, CSI and RGB display connectors are concentrated on the SBC.

iWave's AM62Ax Single Board computer is rich with AM62Ax features along with RAM, eMMC, Ethernet connector, USB2.0 connector, Wi-Fi & BT module and comes in compact 100mm x 72mm form factor.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4

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Acronyms	Abbreviations
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OSM	Open standard Module
OTG	On-The-Go
PCB	Printed Circuit Sheet
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SD	Secure Digital
SoC	System on Chip
SBC	Single Board Computer
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
MIPI	Mobile Industry Processor Interface Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on SBC.

1.5 References

- AM62Ax Sitara™ Processors datasheet
- AM62Ax Sitara Processors Technical Reference Manual
- iW-RainboW-G55M_AM62Ax_OSM_LGA_Module-HardwareUserGuide

1.6 Important Note

In this document, wherever AM62Ax SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

"Functionality Name"

Example: ENET_TXC

In this signal, ***ENET_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

"Functionality Description (GPIO Number)"

Example: BCONFIG_0(GPIO1_9)

In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about AM62Ax SBC features and Hardware architecture with high level block diagram.

2.1 AM62Ax SBC Block Diagram

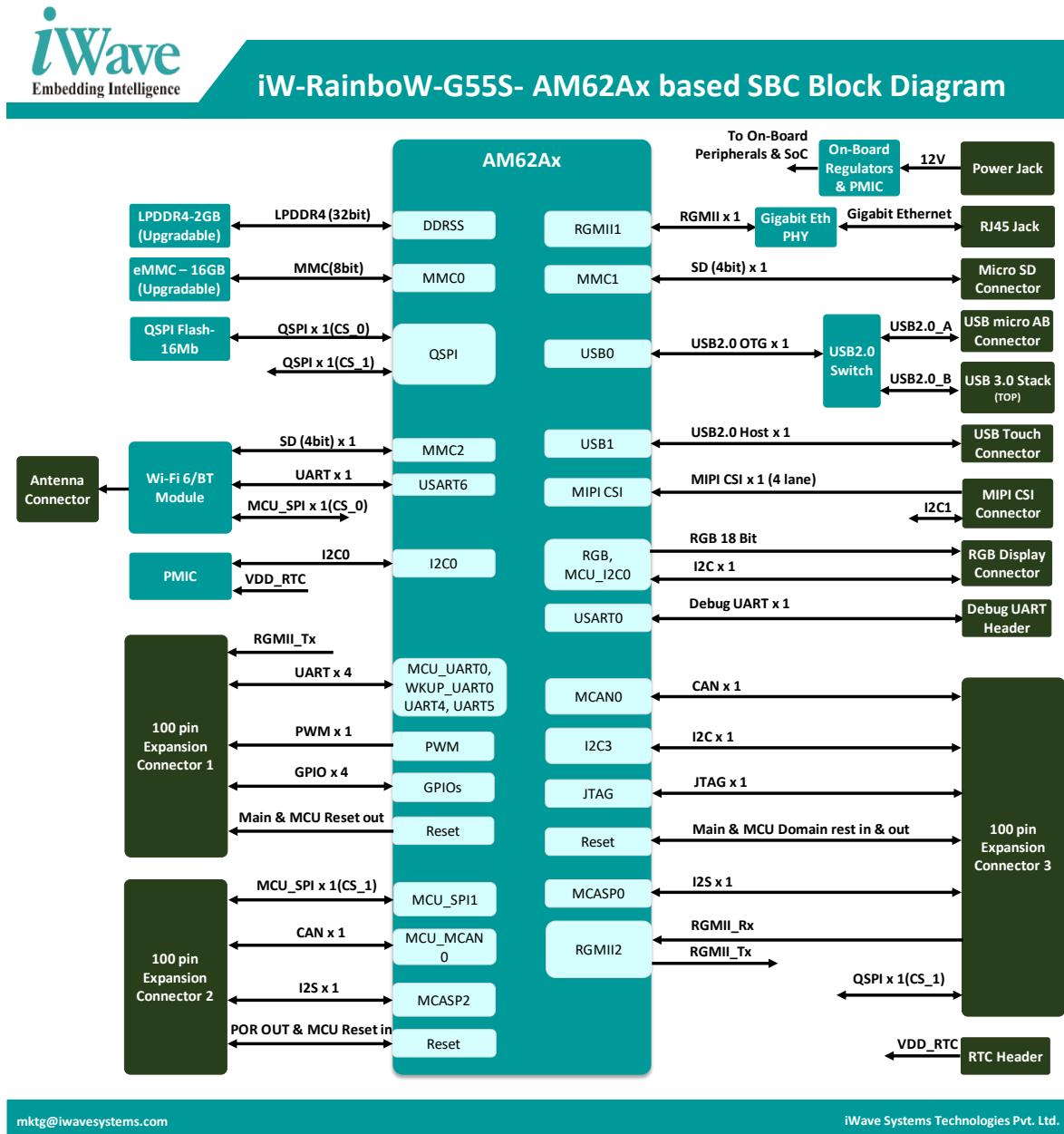


Figure 1: AM62Ax SBC Block Diagram

2.2 AM62Ax SBC Features

AM62Ax SBC supports the following features.

CPU

- AM62Ax Applications Processor¹
 - AM62A74 Quad Core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
 - AM62A72 Dual Core: 2 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
 - AM62A34 Quad core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS
 - AM62A32 Dual core: 2 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS
 - AM62A31 Single core: 1 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS

Power

- TPS6593-Q1 PMIC

Memory

- LPDDR4 With Inline ECC - 2GB (Expandable up to 8GB)²
- eMMC Flash - 16GB (Expandable up to 128GB)²
- Micro SD slot
- 16Mb QSPI Flash

Network & Communication

- IEEE 802.11 a/b/g/n/ac/ax Wi-Fi + BT 5.3 + IEEE802.15.4
- Gigabit Ethernet PHY Transceiver with RJ45 Magjack Connector
- USB 2.0 (USB 3.0 stack top port)
- USB 2.0 OTG port through – micro AB Receptacle Connector
- USB 2.0 Header x 1

Audio/Video Features

- 36pin MIPI_CSI Camera Connector
- 50pin RGB Display Connector

Expansion Connector Interfaces

- Expansion Connector 1 Interfaces
 - UART x 4 Port (1 With CTS & RTS)
 - PWM x 1 Port
 - GPIO x 5
 - RGMII_Tx

- Expansion Connector 2 Interfaces
 - MCU_SPI x 1(CS_1)
 - MCU_CAN x 1 Port
 - I2S x 1
- Expansion Connector 3 Interfaces
 - QSPI x 1(CS_1)
 - CAN x 1 Port
 - I2C x 1 Port
 - JTAG x 1
 - I2S x 1
 - RGMII_Rx

Miscellaneous Interfaces

- RTC Controller with RTC Battery Header
- Debug UART Header

General Specification

- Power Supply : 12V,2A³
- Form Factor : 85mm x 56mm

- ^{1.} There are five configurations of AM62Ax SoC supported by TI, hence in this document AM62A7/ AM62A73 Q/D/S/ is used to represent either of one based on SBC Part Number.
- ^{2.} Memory Size will differ based on iWave's SBC Product Part Number.
- ^{3.} The AM62Ax SBC can support input power 7V to 24V. By default, it is designed to support 12V.

2.3 AM62Ax SoC

iW-RainboW-G55S SBC can support AM62Ax SoCs from TI. The AM62Ax Family consists of two processors: AM62A7 Quad & AM62A3 Quad. The Major Difference between AM62Ax SoCs are:

- AM62A74 Quad Core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 2 TOPS
- AM62A34 Quad core: 4 x Cortex-A53, 2 x Cortex-R5F, 1 x C7x DSP, VPU & ISP, up to 1 TOPS

The AM62Ax processors along with ARM core supports integrated single core Deep Learning Accelerator (C7x256v) of up to 2 TOPs, Image Signal Processor, 4Kp30 video encode and decode capable VPU, 1 x display controllers. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI, eMMC 5.1, SD 3.0, USB 2.0 and Dual core MCU domain integrated with FFI & Device Management.

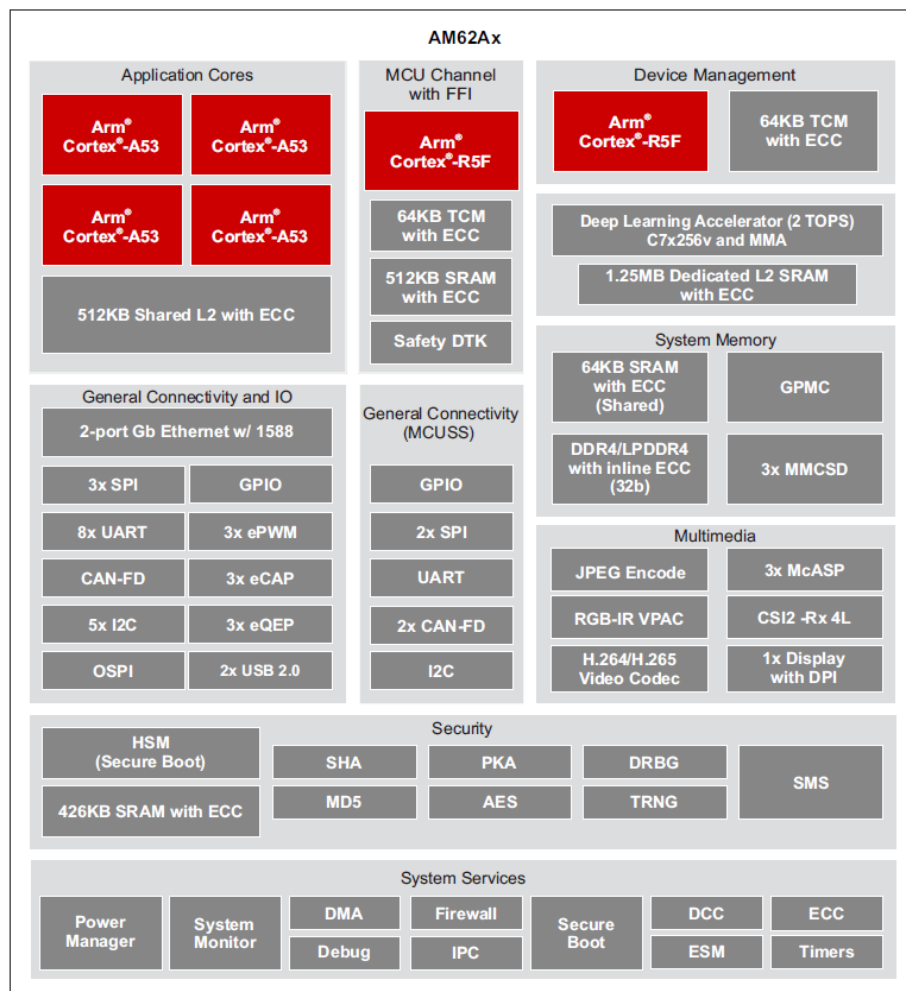


Figure 2: AM62Ax Block Diagram

Note: The AM62Ax processor offers numerous advanced features, please refer the latest AM62Ax Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC

The AM62Ax SBC uses one TPS6593-Q1 PMIC for the SoC power management. The TPS6593-Q1 features five high efficiency step-down regulators and four linear regulators. The TPS6593-Q1 includes a 32-KHz crystal oscillator, which generates an accurate 32-KHz clock for the integrated RTC module. A backup-battery management provides power to the crystal oscillator and the real-time clock (RTC) module from a coin cell battery or a super cap in the event of power loss from the main supply. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The TPS6593-Q1 PMIC comes in 56pin 8x8 VQFN package and is placed on the top side of the SBC.

2.5 Memory

2.5.1 LPDDR4 RAM

The AM62Ax based SBC supports 2GB LPDDR4 RAM memory by default using the 32bit DDR_CH0 channel of AM62Ax SoC to support LPDDR4 up to 3733MT/s. LPDDR4 part is placed on top side of the SBC. The RAM size can be expandable up to maximum of 8GB. To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The AM62Ax Compact SBC supports 16GB eMMC as default boot and storage device. This is directly connected to MMC0 controller of the AM62Ax SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory is physically located on top side of the SBC. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 QSPI Flash

The AM62Ax Compact SBC supports 16Mb QSPI using chip select 0 as optional boot and storage device. This is directly connected to OSPI controller of the AM62Ax SoC and operates at 1.8V (I/O supply).

The QSPI flash memory is physically located on top side of the SBC.

2.5.4 Micro SD Connector

The AM62Ax based SBC supports Micro SD slot which can be used to connect Micro SD card as a Mass storage device. Micro SD card connector is directly connected to the MMC1 controller of the AM62Ax SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The AM62Ax based SBC supports configurable I/O voltage levels for MMC1 lines through GPIO1_IO15. If GPIO1_IO15 is set to low, then 1.8V IO level is selected for MMC1 lines. If GPIO1_IO15 is set to high, then 3.3V IO level is selected for MMC1 lines. This feature is not implemented as of now and will be made available in future release. The micro-SD Connector is physically located on bottom side of the AM62Ax based SBC as shown below.

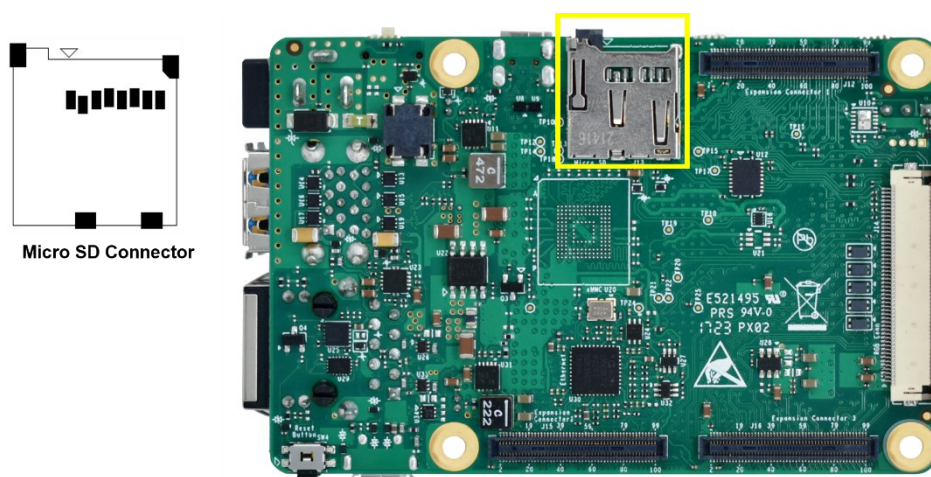


Figure 3: Micro SD Card Connector

2.6 Boot Media Setting

AM62Ax SoC boot process begins at Power on Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. AM62Ax SoC Boot ROM code uses the state of the internal register BOOTMODE [15:0] to determine the boot flow behaviour of the device. The SBC used logic circuit on the SBC to support the boot media making use of three bits as mentioned in below table.

Note: Contact iWave if different boot media support is required other than eMMC.

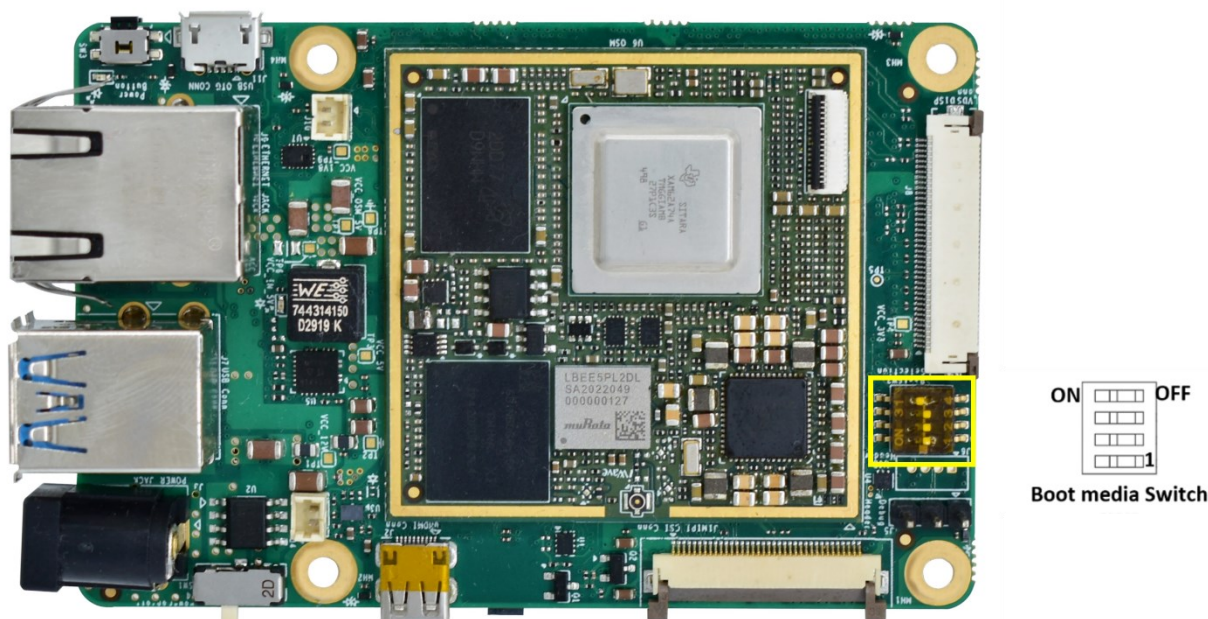


Figure 4: Boot Media Switch

Table 3: Boot Media Settings

Boot Media	SW2		
	POS1	POS2	POS3
QSPI	ON	ON	OFF
eMMC	OFF	OFF	OFF
USB Host	ON	OFF	OFF
USB DFU (Programming Mode)	ON	OFF	ON

2.7 Network & Communication

2.7.1 Wi-Fi and Bluetooth Interface

The AM62Ax based SBC is integrated with Murata's "LBES5PL2EL-SMP" based Wi-Fi+Bluetooth+IEEE802.15.4 module. LBES5PL2EL-SMP module is compliant with IEEE802.11a/b/g/n/ac/ax, SISO, Bluetooth specification v5.3 and IEEE802.15.4. It supports standard SDIO3.0 interface for WLAN, UART interfaces support for Bluetooth is Host Controller Interface (HCI) and SPI interface to optionally support IEEE802.15.4. Connection to a host processor is through SDIO, High-Speed UART interfaces and SPI. The SBC uses SoC UART6 interface for Bluetooth, MMC2 interface for Wi-Fi and MCU SPI With CS1 interface for IEEE802.15.4 in a default configuration. In the AM62Ax Compact SBC, antenna pin of LBES5PL2EL-SMP Wi-Fi/Bluetooth is connected to a µUFL connector.

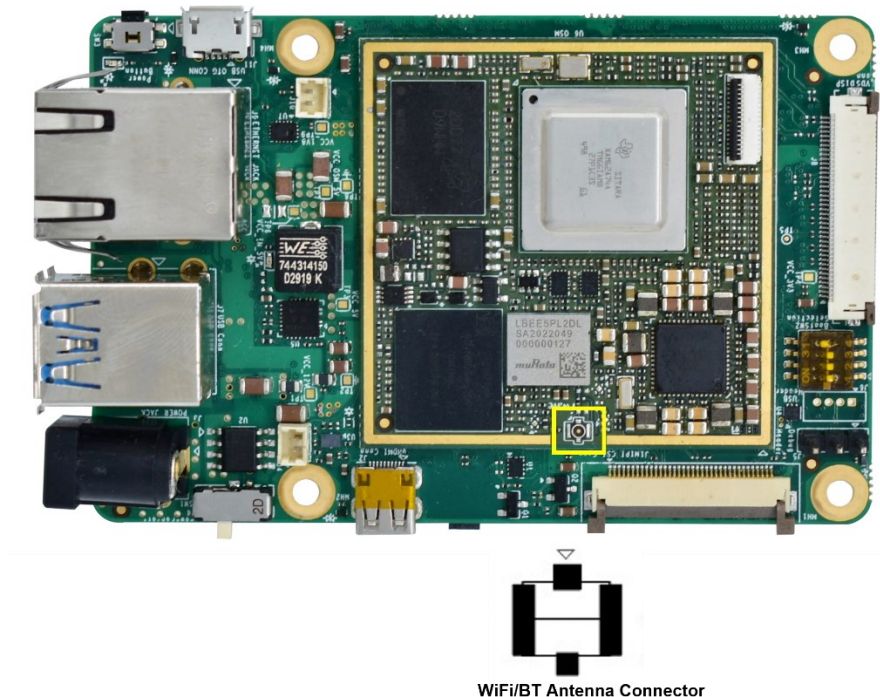


Figure 5: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata.

Antenna Part Number - : 2042811100 from Molex.

2.7.2 Gigabit Ethernet Interface

The AM62Ax SBC supports single Ethernet Port through external Ethernet PHYs from Analog devices which supports 10/100/1000Mbps Ethernet. The Ethernet PHY ADIN1300 is low power gigabit ethernet transceiver with low latency and Time sensitive networking. The interface is compatible with both the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures. The ADIN1300 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet). The ADIN1300 can support cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps. Brown-out protection is provided by monitoring the supplies to detect if one or more supply drops below a minimum falling threshold.

RJ45 Magjack connector is physically located at the top of the board as shown below.

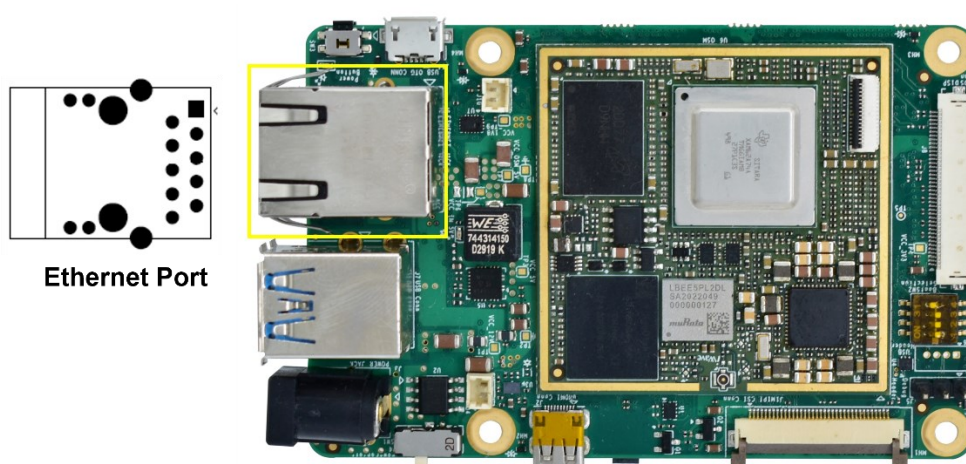


Figure 6: RJ45 Magjack

2.7.3 USB2.0 OTG Interface

The AM62Ax Compact SBC supports USB2.0 High Speed OTG interface. This USB2.0 signals is directly connected to 1:2 data switch and then one output is connected to USB2.0 Micro AB connector for OTG Host support & other one is connected to top port of USB 2.0 stack connector.

USB Interface at top port of USB 2.0 stack connector or OTG connector can be selected by changing the position of 4th bit of switch(SW2). To support USB2.0 OTG, the switch should be turned ON. This USB2.0 OTG connector is physically located at the top of the board as shown below.

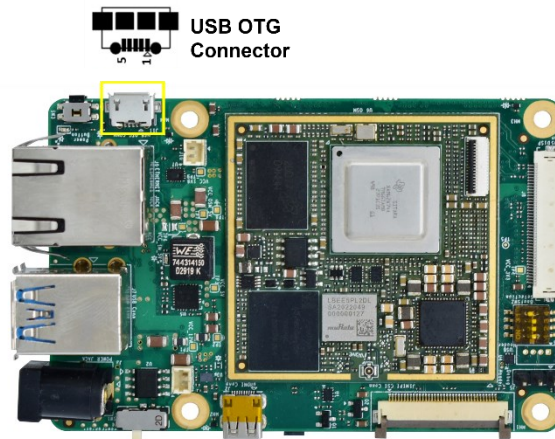


Figure 7: USB OTG Connector

2.8 Serial Interface Features

2.8.1 Debug UART Interface

The AM62Ax Compact SBC supports debug interface through SoC's UART0 interface. This UART0 signals from the SoC is connected to Debug UART header through 1.8V to 3.3V level Translator.

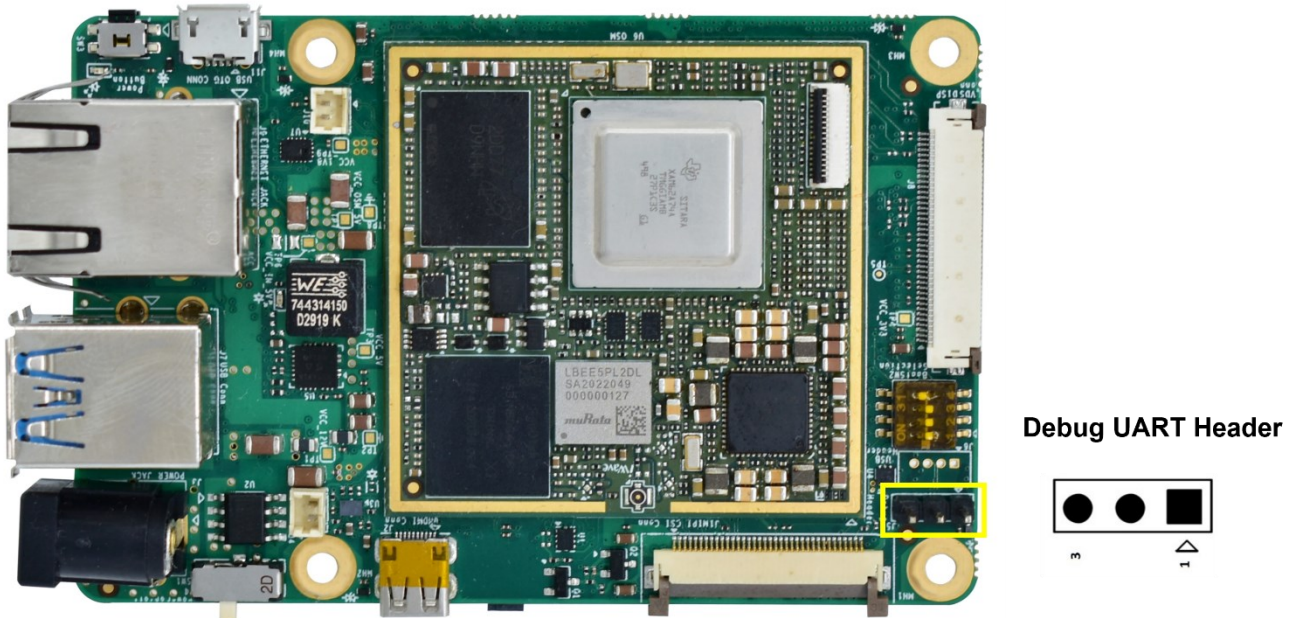


Figure 8: Debug UART Header

Table 4: Debug UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	TX	UART0_TXD	O, 3.3V CMOS	UART interface Transmit signal.
2	RX	UART0_RXD	I, 3.3V CMOS	UART interface Receive signal.
3	GND	GND	Power	Ground.

2.9 Video Features

2.9.1 MIPI CSI Connector

The AM62Ax SBC supports 4-lane camera connectors (36 Pin). the CSI-2 Rx Controller Core is compliant to MIPI CSI2 Specification v1.3 and implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The CSI-2 Rx Controller module supports up to 16 virtual channels per input (partial MIPI CSI v2.0 feature). The Programmable formats including YUV420, YUV422, RGB, Raw, and User Defined (over 25 different formats supported). The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus. The AM62Ax SoC also supports ISP for providing aggregate performance and HDR processing. This MIPI CSI camera connector is physically located on bottom of the board as shown below.

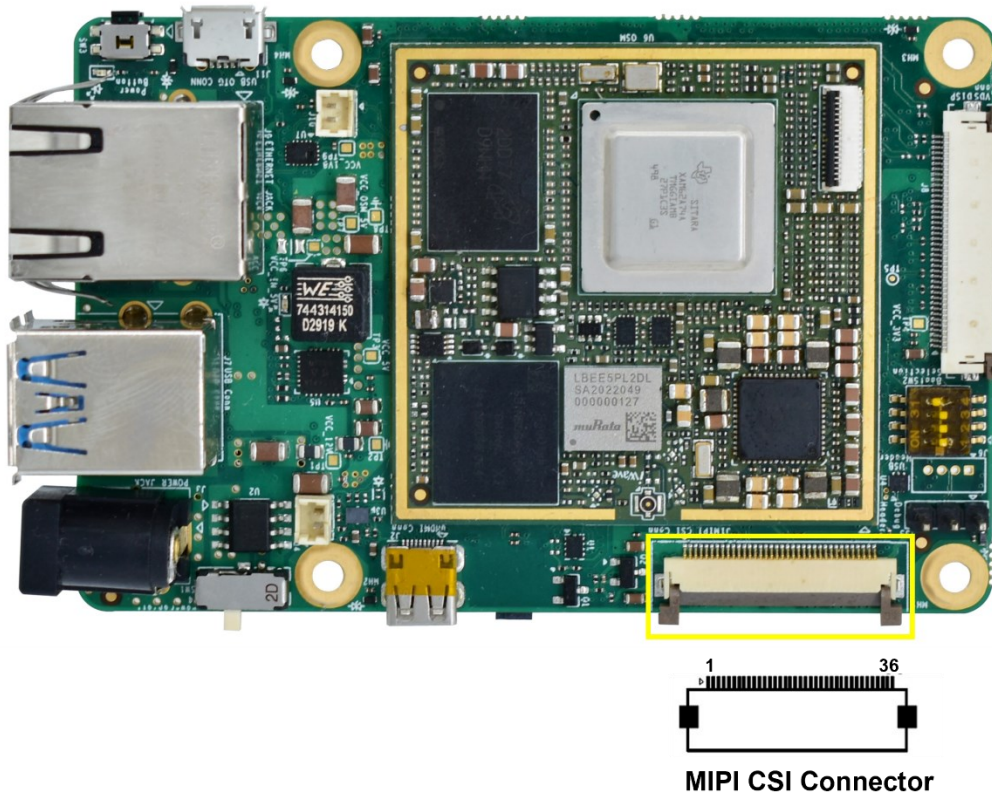


Figure 9: 36 pin MIPI CSI Connector

Number of Pins : 36

Connector Part : FH12A-36S-0.5SH(55) from Hirose Electric Co Ltd

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Table 5: MIPI CSI Connector Pinouts

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
2	CAM_PWR	VCC_3V3	Power	3V3 Camera Power
3	CAM0_CSI_D0+	MIPI_CSI0_DATA0_P	I, MIPI	MIPI CSI1 differential data lane 0 positive.
4	CAM0_CSI_D0-	MIPI_CSI0_DATA0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative.
5	GND	GND	Power	Ground.
6	CAM0_CSI_D1+	MIPI_CSI0_DATA1_P	I, MIPI	MIPI CSI1 differential data lane 1 positive.
7	CAM0_CSI_D1-	MIPI_CSI0_DATA1_N	I, MIPI	MIPI CSI1 differential data lane 1 negative.
8	GND	GND	Power	Ground.
9	CAM0_CSI_D2+	MIPI_CSI0_DATA2_P	I, MIPI	MIPI CSI1 differential data lane 2 positive.
10	CAM0_CSI_D2-	MIPI_CSI0_DATA2_N	I, MIPI	MIPI CSI1 differential data lane 2 negative.
11	CAM0_RST#	GPIO_CAM_RST#(GPIO0_35)	I, 1.8V CMOS/10K PU	MIPI Camera Reset signal
12	CAM0_CSI_D3+	MIPI_CSI0_DATA3_P	I, MIPI	MIPI CSI1 differential data lane 3 positive.
13	CAM0_CSI_D3-	MIPI_CSI0_DATA3_N	I, MIPI	MIPI CSI1 differential data lane 3 negative.
14	GND	GND	Power	Ground.
15	CAM0_CSI_CLK+	MIPI_CSI0_CLK_P	I, MIPI	MIPI CSI1 differential Clock positive.
16	CAM0_CSI_CLK-	MIPI_CSI0_CLK_N	I, MIPI	MIPI CSI1 differential Clock negative.
17	GND	GND	Power	Ground.
18	CAM0_I2C_CLK	I2C1_SCL	I, 1.8V OD/ 4.7K PU	I2C Clock for MIPI CSI1 Camera.
19	CAM0_I2C_DAT	I2C1_SDA	IO, 1.8V OD/ 4.7K PU	I2C Data for MIPI CSI1 Camera.
20	CAM0_ENA#	GPIO_CAM_PWR(GPIO0_32)	I, 1.8V CMOS	Camera 0 Enable (active low).
21	MCLK	NC	NA	NC.
22	CAM1_ENA#	NC	NA	NC.
23	CAM1_I2C_CLK	NC	NA	NC.
24	CAM1_I2C_DAT	NC	NA	NC.
25	GND	GND	Power	Ground.
26	CAM1_CSI_CLK+	NC	NA	NC.
27	CAM1_CSI_CLK-	NC	NA	NC.

Pin No.	Pin Name	Signal Name	Signal Type/ Termination	Description
28	GND	GND	Power	Ground.
29	CAM1_CSI_D0+	NC	NA	NC.
30	CAM1_CSI_D0-	NC	NA	NC.
31	CAM1_RST#	NC	NA	NC.
32	CAM1_CSI_D1+	NC	NA	NC.
33	CAM1_CSI_D1-	NC	NA	NC.
34	GND	GND	Power	Ground.
35	CAM0_GPIO	GPIO1_13	I, 1.8V CMOS	Camera 0 GPIO1_13
36	CAM1_GPIO	GPIO1_13	I, 1.8V CMOS	Camera 0 GPIO1_13

2.9.2 RGB Interface with Touch

The AM62Ax SoC SBC supports 18-Bit RGB display connector (50 pin). The 18-Bit RGB signals from SoC Display Subsystem (DSS) is connected to a 50 pin RGB display connector. The RGB Display Connector and Touch Header are located at bottom side of the board as shown in the below image.

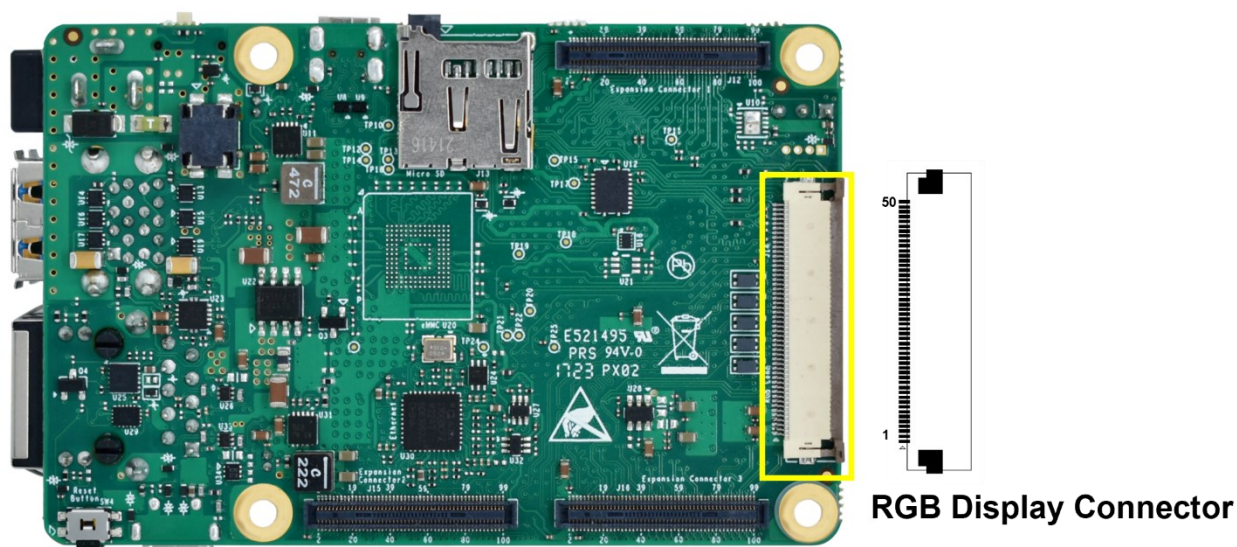


Figure 10: 50 pin RGB Display Connector

Number of Pins : 50

Connector Part : 0541045033 from Molex

Table 6: 50 Pin RGB Display Pinout

Pin No.	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VDD1	VCC_3V3	-	Power	3.3V Supply Voltage.
2	VDD2	VCC_3V3	-	Power	3.3V Supply Voltage.
3	VDD3	VCC_3V3	-	Power	3.3V Supply Voltage.
4	VCC1	VCC_5V	-	Power	5V Supply Voltage.
5	VCC2	VCC_5V	-	Power	5V Supply Voltage.
6	VCC3	VCC_5V	-	Power	5V Supply Voltage.
7	GND1	GND	-	Power	Ground.
8	R0	-	-	-	NC
9	R1	-	-	-	NC
10	R2	VOU0_DATA12(R GB_R0)	VOU0_DATA12/ W20	O, 3.3V CMOS	Red 0 signal.
11	R3	VOU0_DATA13(R GB_R1)	VOU0_DATA13/ W19	O, 3.3V CMOS	Red 1 signal.
12	GND2	GND	-	Power	Ground.
13	R4	VOU0_DATA14(R GB_R2)	VOU0_DATA14/ Y21	O, 3.3V CMOS	Red 2 signal.
14	R5	VOU0_DATA15(R GB_R3)	VOU0_DATA15/ Y22	O, 3.3V CMOS	Red 3 signal.
15	R6	GPMC0_AD8(RGB_ R4)	GPMC0_AD8/ P22	O, 3.3V CMOS	Red 4 signal.
16	R7	GPMC0_AD9(RGB_ R5)	GPMC0_AD9/ R19	O, 3.3V CMOS	Red 5 signal.
17	GND3	GND	-	Power	Ground.
18	G0	-	-	-	NC
19	G1	-	-	-	NC
20	G2	VOU0_DATA6(RG B_G0)	VOU0_DATA6/ V22	O, 3.3V CMOS	Green 0 signal.
21	G3	VOU0_DATA7(RG B_G1)	VOU0_DATA7/ V21	O, 3.3V CMOS	Green 1 signal.
22	GND4	GND	-	Power	Ground.
23	G4	VOU0_DATA8(RG B_G2)	VOU0_DATA8/ V19	O, 3.3V CMOS	Green 2 signal.
24	G5	VOU0_DATA9(RG B_G3)	VOU0_DATA9/ V18	O, 3.3V CMOS	Green 3 signal.
25	G6	VOU0_DATA10(R GB_G4)	VOU0_DATA10/ W22	O, 3.3V CMOS	Green 4 signal.
26	G7	VOU0_DATA11(R GB_G5)	VOU0_DATA11/ W21	O, 3.3V CMOS	Green 5 signal.
27	GND5	GND	-	Power	Ground.
28	B0	DISP_VDD_EN_3V3	GPMC0_CSN2/ M22	IO, 3.3V CMOS	GPIO for supporting VDD enable
29	B1	DISP_BL_EN_3V3	GPMC0_CSN3/ M20	IO, 3.3V CMOS	GPIO for supporting Backlight enable.

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Pin No.	Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
30	B2	VOUT0_DATA0(RG B_B0)	VOUT0_DATA0	O, 3.3V CMOS	Blue 0 signal.
31	B3	VOUT0_DATA1(RG B_B1)	VOUT0_DATA1/ U21	O, 3.3V CMOS	Blue 1 signal.
32	GND6	GND	-	Power	Ground.
33	B4	VOUT0_DATA2(RG B_B2)	VOUT0_DATA2/ U20	O, 3.3V CMOS	Blue 2 signal.
34	B5	VOUT0_DATA3(RG B_B3)	VOUT0_DATA3/ U19	O, 3.3V CMOS	Blue 3 signal.
35	B6	VOUT0_DATA4(RG B_B4)	VOUT0_DATA4/ T19	O, 3.3V CMOS	Blue 4 signal.
36	B7	VOUT0_DATA5(RG B_B5)	VOUT0_DATA5/ U18	O, 3.3V CMOS	Blue 5 signal.
37	GPIO	OSM_GPIO_A_2(M CU_GPIO0_3)	MCU_SPI0_D0/ A15	IO, 3.3V CMOS	General purpose GPIO.
38	DE	VOUT0_DE	VOUT0_DE/ U17	O, 3.3V CMOS	Data Enable.
39	HS	VOUT0_HSYNC	VOUT0_HSYNC/ T18	O, 3.3V CMOS	Horizontal sync.
40	VS	VOUT0_VSYNC	VOUT0_VSYNC/ V17	O, 3.3V CMOS	Vertical sync.
41	DCLK	VOUT0_PCLK	VOUT0_PCLK/ AA22	O, 3.3V CMOS	Dot clock.
42	GND7	GND	-	Power	Ground.
43	RGB_CS#	GPIO0_42(GPMC0_CSn1)	GPMC0_CSn1/ M21	O, 3.3V CMOS	Chip selects.
44	RGB_DISP	GPIO0_41(GPMC0_CSn0)	GPMC0_CSn0/ M19	O, 3.3V CMOS	Display ON/OFF GPIO.
45	GND8	GND	-	Power	Ground.
46	PWM	PWM_0(EXT_REFCLK1)	EXT_REFCLK1/ B16	O, 3.3V CMOS	PWM Signal.
47	RESET	SoC_RESET_OUT_3 V3	NA	O, 3.3V CMOS	Global reset.
48	I2C_SCL	MCU_I2C0_SCL	MCU_I2C0_SCL/ E12	O OD, 3.3V CMOS/4.7K PU	I2C Clock for touch.
49	I2C_SDA	MCU_I2C0_SDA	MCU_I2C0_SDA/ D9	IO OD, 3.3V CMOS/4.7K PU	I2C Data for touch.
50	INT	OSM_GPIO_A_3(M CU_GPIO0_4)	MCU_SPI0_D1/ B12	IO, 3.3V CMOS/ 10K PU	The interrupt signal for touch.

2.9.3 USB 2.0 Header

The AM62Ax Compact SBC supports a 4 Pin USB connector optionally. This connector can be used as general-purpose connector for USB interface.

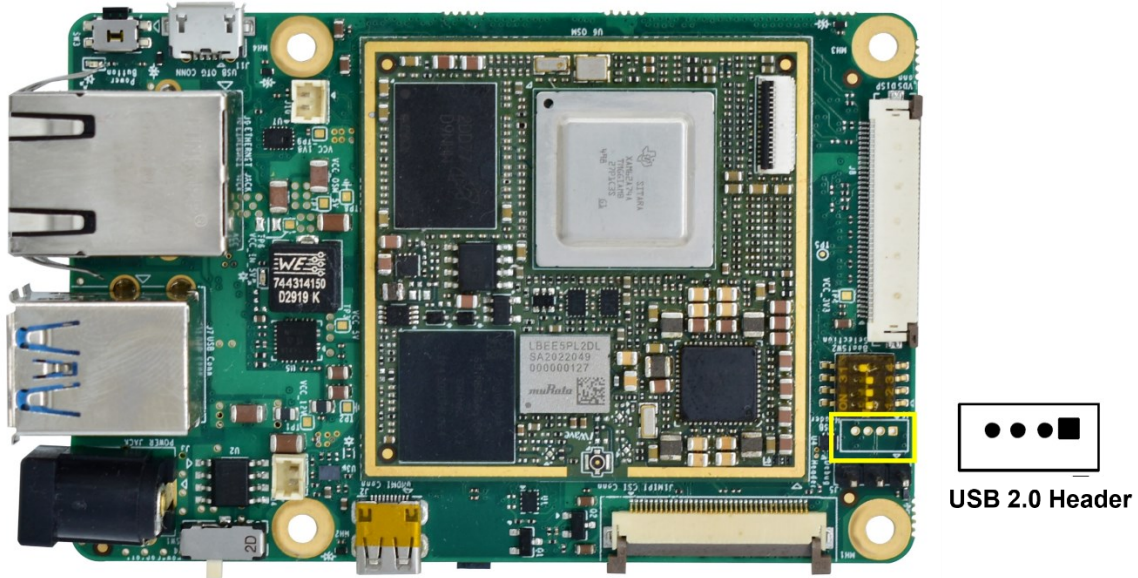


Figure 11: USB Touch Connector

Number of Pins : 4

Connector Part : 53047-0410 from Molex

Mating Connector Part : 0151340400 from Molex

Table 7: Display Touch Pinouts

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	1	VBUS_HOST_TP	5V, Power	Supply Voltage.
2	2	USB1_DM	IO, USB	Differential USB Negative.
3	3	USB1_DP	IO, USB	Differential USB Positive.
4	4	GND	Power	Ground.

2.10 Expansion Connectors

The AM62Ax Compact SBC supports three 100 Pin Expansion connectors.

The interfaces which are available at three 100 Pin Expansion connectors are explained in the following section. This Expansion Connector is physically located at the bottom of the SBC as shown below.

Number of Pins : 100

Connector Part : 10164227-1004A1RLF from Amphenol

Mating Connector Part : 10164228-1001A1RLF from Amphenol

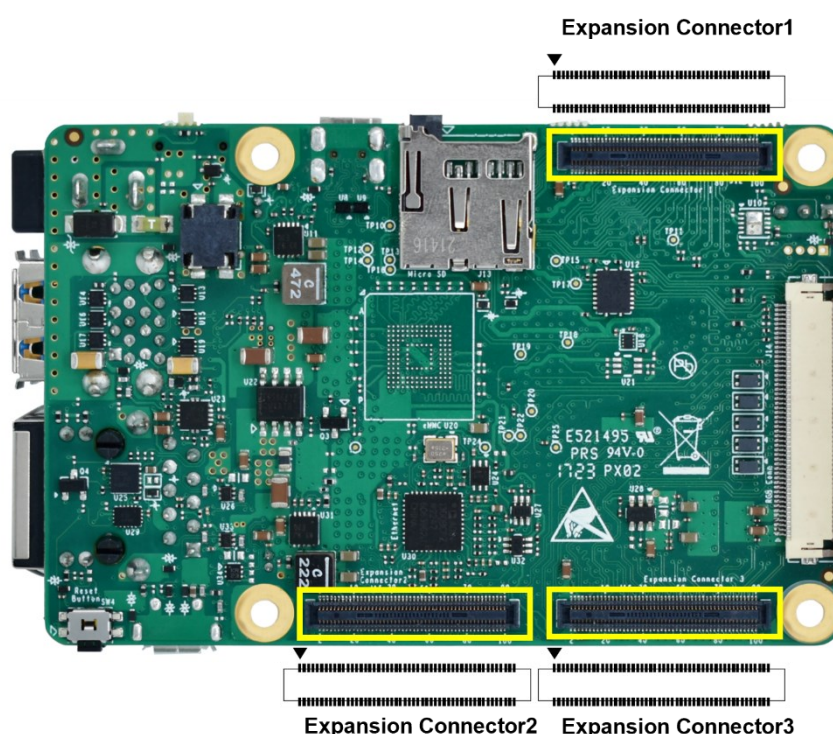


Figure 12: Expansion Connectors

Table 8: Expansion Connector1 Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_3V3	-	Power	3.3V Supply Voltage
2	VCC_5V	-	Power	5V Supply Voltage
3	VCC_3V3	-	Power	3.3V Supply Voltage
4	VCC_5V	-	Power	5V Supply Voltage
5	VCC_3V3	-	Power	3.3V Supply Voltage
6	VCC_5V	-	Power	5V Supply Voltage
7	GND	-	Power	Ground
8	VCC_5V	-	Power	5V Supply Voltage

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
9	UART4_TXD(MMC2_SDWP)	MMC2_SDWP / E21	O, 1.8V CMOS	UART4 Transmitter.
10	GND	-	Power	Ground
11	UART4_RXD(MMC2_SDCD)	MMC2_SDCD / F22	I, 1.8V CMOS	UART4 Receiver.
12	VCC_1V8	-	Power	1.8V Supply Voltage
13	NC	-	-	NC
14	VCC_1V8	-	Power	1.8V Supply Voltage
15	NC	-	-	NC
16	PMIC_ON_OFF	NA	I, 5V CMOS 10K PU	PMIC ON /OFF Input.
17	NC	-	-	NC
18	UART_C_TX	WKUP_UART0_TXD	WKUP_UART0_TX D/E9	O, 1.8V CMOS
19	NC	-	-	NC
20	UART_C_RX	WKUP_UART0_RXD	WKUP_UART0_RX D/C9	I, 1.8V CMOS
21	NC	-	-	NC
22	NC	-	-	NC
23	NC	-	-	NC
24	NC	-	-	NC
25	NC	-	-	NC
26	NC	-	-	NC
27	NC	-	-	NC
28	NC	-	-	NC
29	NC	-	-	NC
30	NC	-	-	NC
31	NC	-	-	NC
32	NC	-	-	NC
33	NC	-	-	NC
34	PWM_1(SPI0_CS1)	SPI0_CS1/C16	O CMOS	PWM.
35	NC	-	-	NC
36	SoC_RESET_OUT	RESETSTATZ/ F19	O, 1.8V CMOS 10K PD	Main domain Hard RESET Out to Carrier.
37	GND	-	Power	Ground
38	NC	-	-	NC
39	NC	-	-	NC
40	NC	-	-	NC
41	GPIO_A_4(MCU_GPIO0_20)	WKUP_I2C0_SDA/ E13	IO, 1.8V CMOS	General Purpose Input/output.
42	GND	-	Power	Ground
43	NC	-	-	NC

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
44	UART5_TXD(OSPI0_C S3)	OSPI0_CSN3/ G20	O, 1.8V CMOS	UART5 Transmitter.
45	GPIO_A_5(MCU_GPIO0_23)	WKUP_CLKOUT0/ B10	IO, 1.8V CMOS	General Purpose Input/output.
46	UART5_RXD(OSPI0_C S2)	OSPI0_CSN2/K20	I, 1.8V CMOS	UART5 Receiver.
47	NC	-	-	NC
48	UART5_CTSn(OSPI0_DQS)	OSPI0_DQS/L21	I, 1.8V CMOS	UART5 Request to Send.
49	GPIO_A_6(MCU_GPIO0_1)	MCU_SPI0_CS1/ C11	IO, 1.8V CMOS	General Purpose Input/output.
50	UART5_RTSn(OSPI0_LBCLK)	OSPI0_LBCLKO/K22	O, 1.8V CMOS	UART2 Clear to Send.
51	NC	-	-	NC
52	MCU_UART0_RXD	MCU_UART0_RXD/D8	I, 1.8V CMOS	MCU UART0 Receiver.
53	NC	NA	IO, 1.8V CMOS	NC. <i>By default, connected to low rate Wifi SPI interface and optionally connected to this pin.</i>
54	MCU_UART0_TXD	MCU_UART0_TXD/F8	O, 1.8V CMOS	MCU UART0 Transmitter.
55	NC	-	-	NC
56	NC	-	-	NC
57	GPIO_B_2(GPIO1_31)	EXTINTn/ F17	IO, 1.8V CMOS	General Purpose Input/output.
58	POR_RESET_OUT	PORZ_OUT/ F18	O, 1.8V CMOS 10K PD	Power on reset out.
59	GND	-	Power	Ground
60	MCU_RESET_IN	MCU_RESETZ/ C12	I, 1.8V CMOS 10K PU	MCU domain Hard RESET Input.
61	NC	-	-	NC
62	ENET_MDIO	MDIO0_MDIO / V13	I/O, 1.8V CMOS	Management data
63	NC	-	-	NC
64	ENET_MDC	MDIO0_MDC / V12	O, 1.8V CMOS	Management data clock
65	GND	-	Power	Ground
66	GND	-	Power	Ground
67	NC	-	-	NC
68	NC	-	-	NC
69	NC	-	-	NC
70	NC	-	-	NC
71	GND	-	Power	Ground

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
72	NC	-	-	NC
73	NC	-	-	NC
74	NC	-	-	NC
75	NC	-	-	NC
76	NC	-	-	NC
77	GND	-	Power	Ground
78	NC	-	-	NC
79	NC	-	-	NC
80	NC	-	-	NC
81	NC	-	-	NC
82	NC	-	-	NC
83	GND	-	Power	Ground
84	NC	-	-	NC
85	NC	-	-	NC
86	GND	-	Power	Ground
87	NC	-	-	NC
88	ENET_RGMII1_TD3	RGMII2_TD3/ W17	O, 1.8V CMOS	Transmit data bit 3
89	GND	-	Power	Ground
90	ENET_RGMII1_TD1	RGMII2_TD1/ Y18	O, 1.8V CMOS	Transmit data bit1
91	NC	-	-	NC
92	ENET_RGMII1_TD2	RGMII2_TD2/ AA18	O, 1.8V CMOS	Transmit data bit 2
93	NC	-	-	NC
94	ENET_RGMII1_TD0	RGMII2_TD0/ AA19	O, 1.8V CMOS	Transmit data bit0
95	GND	-	Power	Ground
96	ENET_RGMII1_TX_CTL	RGMII2_TX_CTL/ Y19	O, 1.8V CMOS	Transmit enable (Error)
97	NC	-	-	NC
98	ENET_RGMII1_TXC	RGMII2_TXC / AB19	I/O, 1.8V CMOS	Transmit clock
99	NC	-	-	NC
100	GND	-	Power	Ground

Table 9: Expansion Connector2 Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_12V	-	Power	12V Supply Voltage
2	VCC_12V	-	Power	12V Supply Voltage
3	VCC_12V	-	Power	12V Supply Voltage
4	VCC_12V	-	Power	12V Supply Voltage

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
5	VCC_12V	-	Power	12V Supply Voltage
6	VCC_12V	-	Power	12V Supply Voltage
7	GND	-	Power	Ground
8	GND	-	Power	Ground
9	NC	-	-	NC
10	NC	-	-	NC
11	NC	-	-	NC
12	NC	-	-	NC
13	GND	-	Power	Ground
14	GND	-	Power	Ground
15	NC	-	-	NC
16	NC	-	-	NC
17	NC	-	-	NC
18	NC	-	-	NC
19	GND	-	Power	Ground
20	GND	-	Power	Ground
21	NC	-	-	NC
22	NC	-	-	NC
23	NC	-	-	NC
24	NC	-	-	NC
25	GND	-	Power	Ground
26	GND	-	Power	Ground
27	NC	-	-	NC
28	NC	-	-	NC
29	NC	-	-	NC
30	NC	-	-	NC
31	NC	-	-	NC
32	GND	-	Power	Ground
33	NC	-	-	NC
34	NC	-	-	NC
35	NC	-	-	NC
36	NC	-	-	NC
37	SOC_BOOT_MODE0	GPMC0_AD0/ N21	I/O 3.3V CMOS 10K PU	Boot mode0.
38	GND	-	Power	Ground
39	SOC_BOOT_MODE1	GPMC0_AD1/ N20	I/O 3.3V CMOS 10K PU	Boot mode1.
40	NC	-	-	NC
41	SOC_BOOT_MODE12	GPMC0_AD12/ T22	I/O 3.3V CMOS 10K PU	Boot mode12.
42	NC	-	-	NC
43	SOC_BOOT_MODE13	GPMC0_AD13/ R21	I/O 3.3V CMOS 10K PU	Boot mode13.

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
44	GND	-	Power	Ground
45	SOC_BOOT_MODE15	GPMC0_AD15/ T21	I/O 3.3V CMOS 100K PD	Boot mode15.
46	NC	-	-	NC
47	SOC_BOOT_MODE14	GPMC0_AD14/ T20	I/O 3.3V CMOS 100K PD	Boot mode14.
48	NC	-	-	NC
49	NC	-	-	NC
50	GND	-	Power	Ground
51	NC	-	-	NC
52	NC	-	-	NC
53	NC	-	-	NC
54	NC	-	-	NC
55	GND	-	Power	Ground
56	GND	-	Power	Ground
57	NC	-	-	NC
58	NC	-	-	NC
59	NC	-	-	NC
60	NC	-	-	NC
61	NC	-	-	NC
62	GND	-	Power	Ground
63	NC	-	-	NC
64	NC	-	-	NC
65	NC	-	-	NC
66	NC	-	-	NC
67	NC	-	-	NC
68	GND	-	Power	Ground
69	NC	-	-	NC
70	NC	-	-	NC
71	NC	-	-	NC
72	NC	-	-	NC
73	NC	-	-	NC
74	NC	-	-	NC
75	GPIO0_40(GPMC0_D IR)	GPMC0_DIR/ K18	I/O 3.3V CMOS	GPIO0_40
76	NC	-	-	NC
77	NC	-	-	NC
78	NC	-	-	NC
79	NC	-	-	NC
80	NC	-	-	NC
81	PMIC_GPIO6	NA	I/O 1.8V CMOS	PMIC GPIO16
82	NC	-	-	NC

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
83	EMU1	EMU1/E10	I/O 1.8V CMOS 10K PU	Emulator1
84	NC	-	-	NC
85	EMU0	EMU0/C13	I/O 1.8V CMOS 10K PU	Emulator0
86	MCU_SPI1_CS0(WKU P_UART0_CTSn)	WKUP_UART0_CTSN /C10	O, 1.8V CMOS	MCU SPI1 Chip Select 0
87	NC	-	-	NC
88	NC	-	-	NC
89	NC	-	-	NC
90	MCU_SPI1_MOSI(MC U_UART0_CTSn)	MCU_UART0_CTSN/ B11	O, 1.8V CMOS	MCU SPI1 Master Out Slave In
91	NC	-	-	NC
92	MCU_SPI1_MISO(MC U_UART0_RTSn)	MCU_UART0_RTSN/ D10	I, 1.8V CMOS	MCU SPI1 Master IN Slave Out
93	NC	-	-	NC
94	MCU_SPI1_CLK(MCU _MCAN1_RX)	MCU_SPI1_CLK(MCU _MCAN1_RX)/B9	O, 1.8V CMOS/0E	MCU SPI1 Clock
95	NC	-	-	NC
96	NC	-	-	NC
97	NC	-	-	NC
98	MCU_MCAN0_TXD	MCU_MCAN0_TXD/ C7	O, 1.8V CMOS	MCU CAN0 Transmitter.
99	NC	-	-	NC
100	MCU_MCAN0_RXD	MCU_MCAN0_RXD/ E8	I, 1.8V CMOS	MCU CAN0 Receiver.

Table 10: Expansion Connector3 Pinouts

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_3V3	-	Power	3V3 Supply Voltage
2	VCC_128	-	Power	1V8 Supply Voltage
3	VCC_3V3	-	Power	3V3 Supply Voltage
4	VCC_128	-	Power	1V8 Supply Voltage
5	VCC_3V3	-	Power	3V3 Supply Voltage
6	GND	-	Power	Ground
7	VCC_3V3	-	Power	3V3 Supply Voltage
8	NC	-	-	NC
9	GND	-	Power	Ground
10	QSPIO_CS1	OSPIO_CSN1/ G19	O, 1.8V CMOS	QSPIO Chip Select 0
11	MCAN0_RX	MCAN0_RX/ C18	I, 1.8V CMOS	CAN 1 Receiver.

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
12	MCASP0_AXR3	MCASP0_AXR3/ C19	O, 1.8V CMOS	Serial Audio Interface Channel A Data Output
13	MCAN0_TX	MCAN0_TX/ B17	O, 1.8V CMOS	CAN 1 Transmitter.
14	I2C3_SDA(UART0_RS TN)	UART0_RTSN/ C15	IO OD, 1.8V CMOS/4.7K PU	General Purpose I2C Data.
15	NC	-	-	NC
16	I2C3_SCL(UART0_CS TN)	UART0_CTSN/ F14	IO OD, 1.8V CMOS/4.7K PU	General Purpose I2C Clock.
17	NC	-	-	NC
18	NC	-	-	NC
19	NC	-	-	NC
20	NC	-	-	NC
21	NC	-	-	NC
22	NC	-	-	NC
23	GND	-	Power	Ground
24	MCASP0_AXR1	MCASP0_AXR1/ B18	O, 1.8V CMOS	Serial Audio Interface Channel B Data Output
25	NC	-	-	NC
26	MCASP0_AFSX	MCASP0_AFSX/ A20	O, 1.8V CMOS	Serial Audio Interface Channel Left/Right Clock
27	NC	-	-	NC
28	GND	-	Power	Ground
29	GND	-	Power	Ground
30	QSPIO_D3	OSPIO_D3/ H18	IO, 1.8V CMOS	QSPIO Data3
31	NC	-	-	NC
32	QSPIO_D2	OSPIO_D2/ J19	IO, 1.8V CMOS	QSPIO Data2
33	NC	-	-	NC
34	MCASP0_ACLKX	MCASP0_ACLKX/A19	O, 1.8V CMOS	Serial Audio Interface Channel Bit Clock
35	GND	-	Power	Ground
36	MCASP0_AXR2	MCASP0_AXR2/ B19	I, 1.8V CMOS	Serial Audio Interface Channel A Data Input
37	NC	-	-	NC
38	QSPIO_D1	OSPIO_D1/ J18	IO, 1.8V CMOS	QSPIO Data1
39	NC	-	-	NC
40	NC	-	-	NC
41	GND	-	Power	Ground
42	MCASP0_AXR0	MCASP0_AXR0/ B20	I, 1.8V CMOS	Serial Audio Interface Channel B Data Input

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
43	NC	-	-	NC
44	QSPIO_D0	OSPIO_D0/ J21	IO, 1.8V CMOS	QSPIO Data0
45	NC	-	-	NC
46	QSPIO_CLK	OSPIO_CLK/ L22	O, 1.8V CMOS	QSPIO Clock
47	GND	-	Power	Ground
48	NC	-	-	NC
49	NC	-	-	NC
50	NC	-	-	NC
51	NC	-	-	NC
52	JTAG_TDO	JTAG_TDO/ C14	O, CMOS 1V8	JTAG test data output.
53	GND	-	Power	Ground
54	JTAG_TRSTN	TRSTN/ F15	I, 1V8 CMOS 10K PD	JTAG test RESET output.
55	NC	-	-	NC
56	NC	-	-	NC
57	NC	-	-	NC
58	MCU_RESET_OUT	MCU_RESETSTATZ/ D14	O, 1.8V CMOS 10K PD	MCU domain (SoC) Hard RESET Out.
59	GND	-	Power	Ground
60	JTAG_TDI	TDI/ A16	I, 1V8 CMOS 10K PU	JTAG test data input.
61	NC	-	-	NC
62	JTAG_TCK	TCK/ A14	I, 1V8 CMOS 10K PU	JTAG test Clock.
63	NC	-	-	NC
64	JTAG_TMS	TMS/ B14	I, 1V8 CMOS 10K PU	JTAG test mode select.
65	GND	-	Power	Ground
66	NC	-	-	NC
67	NC	-	-	NC
68	NC	-	-	NC
69	NC	-	-	NC
70	NC	-	-	NC
71	GND	-	Power	Ground
72	NC	-	-	NC
73	NC	-	-	NC
74	NC	-	-	NC
75	NC	-	-	NC
76	NC	-	-	NC
77	GND	-	Power	Ground
78	NC	-	-	NC

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Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
79	NC	-	-	NC
80	NC	-	-	NC
81	NC	-	-	NC
82	NC	-	-	NC
83	GND	-	Power	Ground
84	NC	-	-	NC
85	NC	-	-	NC
86	NC	-	-	NC
87	NC	-	-	NC
88	ENET_RGMII1_RXC	RGMII2_RXC/ AA20	I, 1.8V CMOS	Receive clock.
89	GND	-	Power	Ground
90	NC	-	-	NC
91	NC	-	-	NC
92	ENET_RGMII1_RD3	RGMII2_RD3/ AB20	I, 1.8V CMOS	Receive data bit 3.
93	NC	-	-	NC
94	ENET_RGMII1_RD2	RGMII2_RD2/ AB21	I, 1.8V CMOS	Receive data bit 2.
95	GND	-	Power	Ground
96	ENET_RGMII1_RX_CTL	RGMII2_RX_CTL/W18	I, 1.8V CMOS	Receive control bit.
97	NC	-	-	NC
98	ENET_RGMII1_RD1	RGMII2_RD1/ Y20	I, 1.8V CMOS	Receive data bit 1.
99	NC	-	-	NC
100	ENET_RGMII1_RD0	RGMII2_RD0/ AA21	I, 1.8V CMOS	Receive data bit 0.

Note: Refer GPIO Column under “AM62Ax Pin Multiplexing on Expansion Connector for details on GPIO options available from Expansion connector.

2.11 Other Features

2.12 Fan Header

The AM62Ax Compact SBC supports a Fan Header to connect a cooling Fan if required. This Fan Header is physically located at the top of the board as shown below.

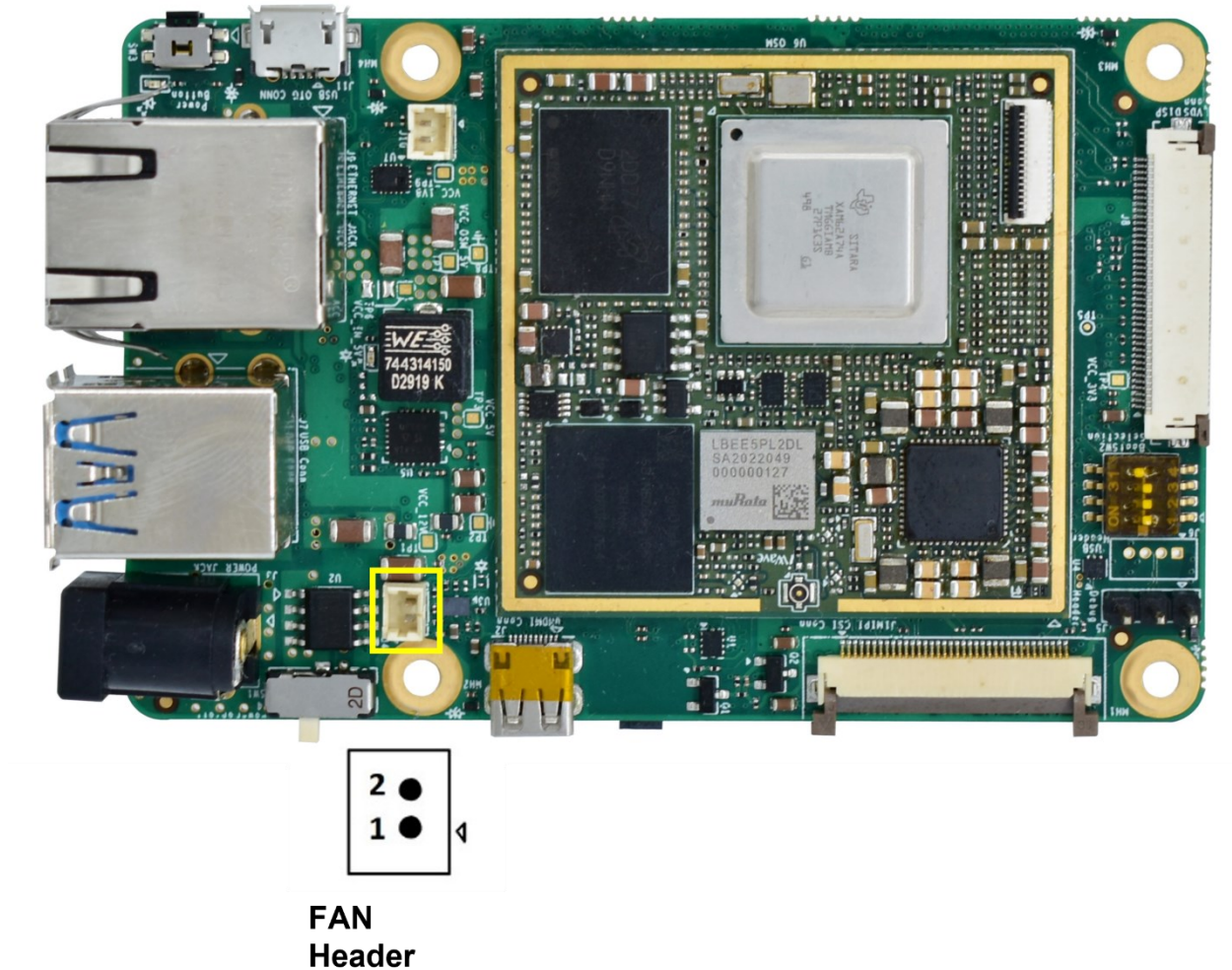


Figure 13: Fan Connector

Number of Pins : 2

Connector Part :10114829-10102LF from Amphenol ICC (FCI)

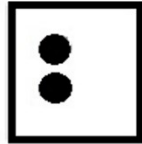
Table 11: Fan Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN. <i>Note: Optionally connected to 12V Power.</i>
2	GND	Power	Ground.

Note: Contact iWave support team if 12V Power Support is required for FAN Header.

2.12.1 RTC Battery Header

The AM62Ax Compact SBC supports external RTC cell. The SBC supports 2pin connector for backup battery or coin cell connection. The 2pin RTC battery connector is physically located on bottom side of the SBC as shown below.



RTC Header

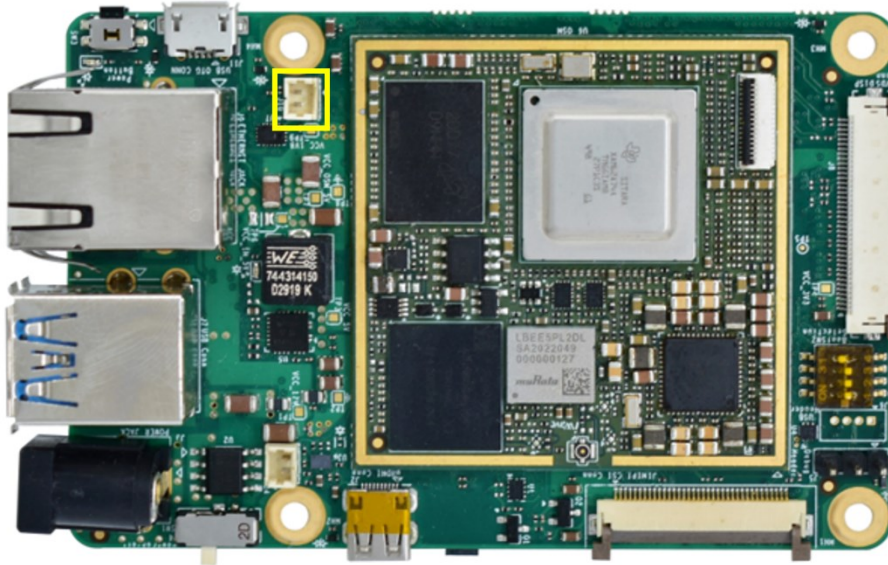


Figure 14: RTC Battery Connector

Number of Pins : 2

Connector Part : 10114829-10102LF from Amphenol ICC (FCI)

Table 12: RTC Battery Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VRTC_3V0	I, Power	+3V Power Input to RTC Controller
2	GND	Power	Ground.

2.12.2 Power ON/OFF Switch

The AM62Ax Compact SBC has power ON/OFF switch to control the Main power Input ON/OFF functionality. The Power ON/OFF switch is physically located at the top of the board as shown below.

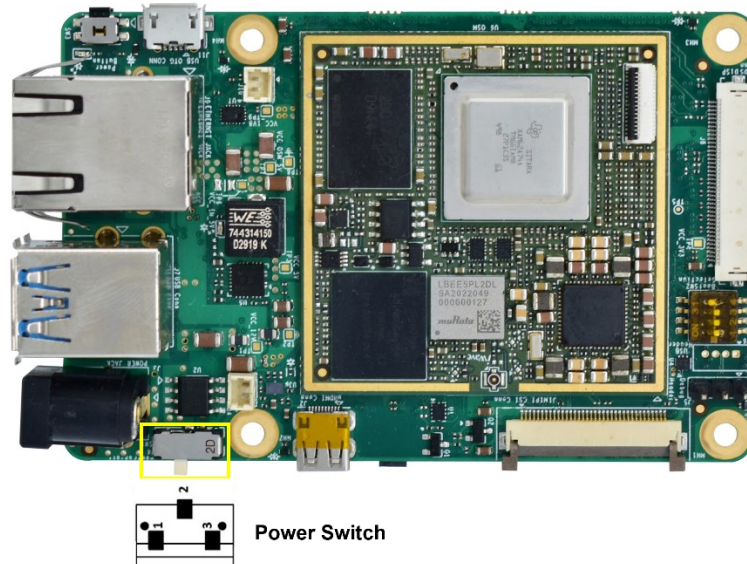


Figure 15: Power ON/OFF Switch

2.12.3 Reset Switch

The AM62Ax Compact SBC Support Push Button Switch to reset the AM62Ax CPU. Reset signal is directly connected from reset push button switch. This Reset push button Switch is physically located at the bottom of the board as shown below.

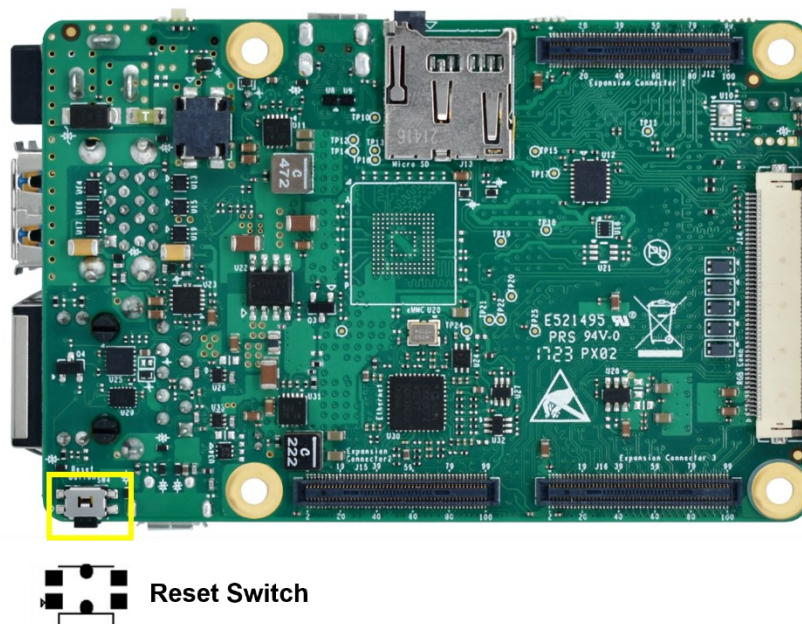


Figure 16: Reset Switch

2.13 AM62Ax Pin Multiplexing on Expansion Connector

The AM62Ax SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the AM62Ax SOC's IO pins can be configured as GPIO if required. The below table provides the details of AM62Ax SoC pin connections to the Expansion Connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring TI's AM62Ax Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in SBC for iWave's BSP reusability.

Table 13: AM62Ax CPU IOMUX for Expansion Connector interfaces

Interface/ Function	Exp. Conn. Pin Number	AM62Ax CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 14	Default
Expansion Connector1														
RGMII	88	W17	RGMII2_TD3	CLKOUT0	MCASP2_ACLKX					GPIO1_0	EQEP2_S			RGMII2_TD3
	90	Y18	RGMII2_TD1	RMII2_TXD1	MCASP2_ACLKR			MCASP2_AXR8		GPIO0_90				RGMII2_TD1
	92	AA18	RGMII2_TD2		MCASP2_AFSX					GPIO0_91	EQEP2_I			RGMII2_TD2
	94	AA19	RGMII2_TD0	RMII2_TXD0	MCASP2_AXR6					GPIO0_89				RGMII2_TD0
	96	Y19	RGMII2_TX_CTL	RMII2_TX_EN	MCASP2_AXR4					GPIO0_87				RGMII2_TX_CTL
	98	AB19	RGMII2_TXC	RMII2_CRS_DV	MCASP2_AXR5					GPIO0_88				RGMII2_TXC
MDIO	62	V13	MDIO0_MDIO							GPIO0_85				MDIO0_MDIO
	64	V12	MDIO0_MDC							GPIO0_86				MDIO0_MDC
UART4	9	E21	MMC2_SDWP	MCASP1_AFSX			UART4_TXD			GPIO0_72				UART4_TXD
	11	F22	MMC2_SDCD	MCASP1_ACLKX			UART4_RXD			GPIO0_71				UART4_RXD
WKUP_UART0	18	E9	WKUP_UART0_TXD		MCU_SPI1_CS2					MCU_GPIO0_10				WKUP_UART0_TXD
	19	C9	WKUP_UART0_RXD		MCU_SPI0_CS2					MCU_GPIO0_9				WKUP_UART0_RXD
UART5	44	G20	OSPI0_CSn3	OSPI0_RESET_OUT0	OSPI0_ECC_FAIL	MCASP1_ACLKR	MCASP1_AXR3	UART5_TXD		GPIO0_14				UART5_TXD
	46	K20	OSPI0_CSn2	SPI1_CS1	OSPI0_RESET_OUT1	MCASP1_AFSR	MCASP1_AXR2	UART5_RXD		GPIO0_13				UART5_RXD
	48	L21	OSPI0_DQS					UART5_CTSn		GPIO0_2				UART5_CTSn
	50	K22	OSPI0_LBCLK0					UART5_RTSn		GPIO0_1				UART5_RTSn
MCU_UART0	52	D8	MCU_UART0_RXD							MCU_GPIO0_5				MCU_UART0_RXD
	54	F8	MCU_UART0_TXD							MCU_GPIO0_6				MCU_UART0_TXD
PWM	34	C16	SPI0_CS1	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APWM_OUT				GPIO1_16		EHRPWM_TZn_IN5		EHRPWM0_B
GPIOs	41	E13	WKUP_I2C0_SDA							MCU_GPIO0_20				MCU_GPIO0_20
	45	B10	WKUP_CLKOUT0							MCU_GPIO0_23				MCU_GPIO0_23
	49	C11	MCU_SPI0_CS1	MCU_OBSCLK0	MCU_SYSCLOCK0	MCU_EXT_REFCLK0	MCU_TIMER_I01			MCU_GPIO0_1				MCU_GPIO0_1
	57	F17	EXTINTn							GPIO1_31				GPIO1_31
Expansion Connector2														
MCU_SPI	86	C10	WKUP_UART0_CTSn	WKUP_TIMER_IO0		MCU_SPI1_CS0				MCU_GPIO0_11				MCU_SPI1_CS0
	90	B11	MCU_UART0_CTSn	MCU_TIMER_IO0		MCU_SPI1_D0				MCU_GPIO0_7				MCU_SPI1_D0
	92	D10	MCU_UART0_RTSn	MCU_TIMER_IO1		MCU_SPI1_D1				MCU_GPIO0_8				MCU_SPI1_D1
	94	B9	MCU_MCAN1_RX	MCU_TIMER_IO3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK			MCU_GPIO0_16				MCU_SPI1_CLK

Interface/ Function	Exp. Conn. Pin Number	AM62Ax CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 14	Default
MCU_CAN	98	C7	MCU_MCAN0_TX	WKUP_TIMER_IO0	MCU_SPI0_CS3					MCU_GPIO0_13				MCU_MCAN0_TX
	100	E8	MCU_MCAN0_RX	MCU_TIMER_IO0	MCU_SPI1_CS3					MCU_GPIO0_14				MCU_MCAN0_RX
I2S	43	R21	GPMC0_AD13	VOUT0_DATA21	UART4_TXD	MCASP2_ACLKX			TRC_DATA2_1	GPIO0_28			GPIO1_124	MCASP2_ACLKX
	41	T22	GPMC0_AD12	VOUT0_DATA20	UART4_RXD	MCASP2_AFSX			TRC_DATA2_2	GPIO0_27			GPIO1_123	MCASP2_AFSX
	39	N20	GPMC0_AD1			MCASP2_AXR5			TRC_CTL	GPIO0_16			GPIO1_113	MCASP2_AXR5
	37	N21	GPMC0_AD0			MCASP2_AXR4			TRC_CLK	GPIO0_15			GPIO1_112	MCASP2_AXR4
GPIOs	45	T21	GPMC0_AD15	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR			TRC_DATA1_9	GPIO0_30	UART2_RTSn		GPIO1_126	GPIO1_126
	47	T20	GPMC0_AD14	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR			TRC_DATA2_0	GPIO0_29	UART2_CTSn		GPIO1_125	GPIO1_125
	75	K18	GPMC0_DIR			MCASP2_AXR13			TRC_DATA1_4	GPIO0_40	EQEP2_S			GPIO0_40
Expansion Connector3														
RGMII	88	AA20	RGMII2_RXC	RMII2_REF_CLK	MCASP2_AXR1					GPIO1_2				RGMII2_RXC
	92	AB20	RGMII2_RD3		AUDIO_EXT_RE_FCLK0					GPIO1_6				RGMII2_RD3
	94	AB21	RGMII2_RD2		MCASP2_AXR0					GPIO1_5				RGMII2_RD2
	96	W18	RGMII2_RX_CTL	RMII2_RX_ER	MCASP2_AXR3					GPIO1_1				RGMII2_RX_CTL
	98	Y20	RGMII2_RD1	RMII2_RXD1	MCASP2_AFSR			MCASP2_AXR7		GPIO1_4				RGMII2_RD1
	100	AA21	RGMII2_RD0	RMII2_RXD0	MCASP2_AXR2					GPIO1_3				RGMII2_RD0
QSPI	30	H18	OSPI0_D3							GPIO0_6				OSPI0_D3
	32	J19	OSPI0_D2							GPIO0_5				OSPI0_D2
	38	J18	OSPI0_D1							GPIO0_4				OSPI0_D1
	44	J21	OSPI0_D0							GPIO0_3				OSPI0_D0
	46	L22	OSPI0_CLK							GPIO0_0				OSPI0_CLK
	10	G19	OSPI0_CSn1							GPIO0_12				OSPI0_CSn1
I2S	12	C19	MCASP0_AXR3	SPI2_D0	UART1_CTSn	UART6_RXD		ECAP1_IN_APWM_OUT		GPIO1_7	EQEP0_A			MCASP0_AXR3
	24	B18	MCASP0_AXR1	SPI2_CS2	ECAP1_IN_APWM_OUT				EHRPWM1_A	GPIO1_9	EQEP0_S			MCASP0_AXR1
	26	A20	MCASP0_AFSX	SPI2_CS3	AUDIO_EXT_RE_FCLK1					GPIO1_12	EQEP1_B			MCASP0_AFSX
	34	A19	MCASP0_ACLKX	SPI2_CS1	ECAP2_IN_APWM_OUT					GPIO1_11	EQEP1_A			MCASP0_ACLKX
	36	B19	MCASP0_AXR2	SPI2_D1	UART1_RTSn	UART6_TXD		ECAP2_IN_APWM_OUT		GPIO1_8	EQEP0_B			MCASP0_AXR2
	42	B20	MCASP0_AXR0		AUDIO_EXT_RE_FCLK0				EHRPWM1_B	GPIO1_10	EQEP0_I			MCASP0_AXR0
CAN	11	C18	MCAN0_RX	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S		GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4		MCAN0_RX
	13	B17	MCAN0_TX	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I		GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3		MCAN0_TX
I2C	14	C15	UART0_RTSn	UART0_RTSn	SPI0_CS3	I2C3_SDA	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1		GPIO1_23	MCASP2_ACLKX		I2C3_SDA
	16	F14	UART0_CTSn	UART0_CTSn	SPI0_CS2	I2C3_SCL	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0		GPIO1_22	MCASP2_AFSX		I2C3_SCL

3. TECHNICAL SPECIFICATION

This section provides detailed information about the AM62Ax Compact SBC technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The AM62Ax Compact SBC supports 7V to 24V external power and uses on board voltage regulators for internal power management. By default, it supports to work with 12V power input. 12V power input from an external power supply is connected to the AM62Ax Compact SBC. This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. The Power Jack is physically placed at the top of the board as shown below.

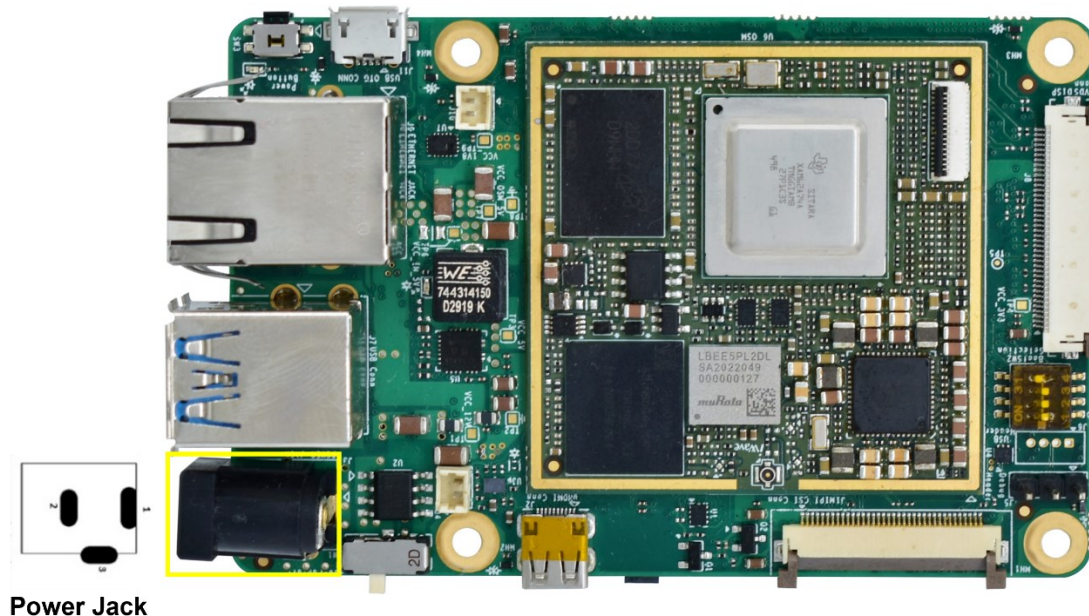


Figure 17: Power Input Jack

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V01	2.8V	3V	3.3V	±20mV

¹ The AM62Ax Compact SBC uses this voltage as backup power source to RTC controller when VCC_12V is OFF.

3.2 Power Consumption

Table15: AM62Ax Compact SBC Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption¹		
Ping Bluetooth	VCC_ 12V	TBD
Ping Wi-Fi	VCC_ 12V	TBD
Ping Ethernet (Eth0) at 1000Mbps	VCC_ 12V	TBD
eMMC to Micro SD file transfer	VCC_ 12V	TBD
eMMC to USB2.0 file transfer	VCC_ 12V	TBD
Dhrystone	VCC_ 12V	TBD
Maximum Power Test: - Run the below during Maximum Power Test, - Play Video run in RGB display - Camera Streaming - Ethernet (eth0) Run the ping (65500 packet size) - Wi-Fi- Run the ping testing in background - File Transfer - Transfer the 1GB files in storage devices - Run the dry2 application on background	VCC_ 12V	TBD
- Run the below during Maximum Power Test, Play the video on RGB display Connected. - Camera Streaming - Ethernet (eth0) Run the ping (65500 packet size) - Wi-Fi- Run the ping testing in background - File Transfer - Transfer the 1GB files in storage devices - Run the dry2 application on background	VCC_ 12V	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VCC_ 12V	TBD
Deep Sleep Mode.	VCC_ 12V	TBD

¹ Power consumption measurements have been done in iWave's AM62Ax based Compact SBC with iWave's TBD

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of AM62Ax Compact SBC.

Table 16: Environmental Specification

Parameters	Min	Max
Operating temperature range ¹	-40°C	85°C

¹ iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3 For more information on Thermal solution & Heat sink refer the following section.

3.3.2 Heat Sink

For any highly integrated SBC, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink must be used. Always need to remember that more effective thermal solution will give more performance out of the CPU.

Note: iWave supports Heat Sink Solution for AM62Ax Compact SBC. For more information on Heat Sink contact iWave support team. Do not Power On the AM62Ax Compact SBC without a proper thermal solution.

Ordering Part Number: iW-AFHK-BKAT-SSA0

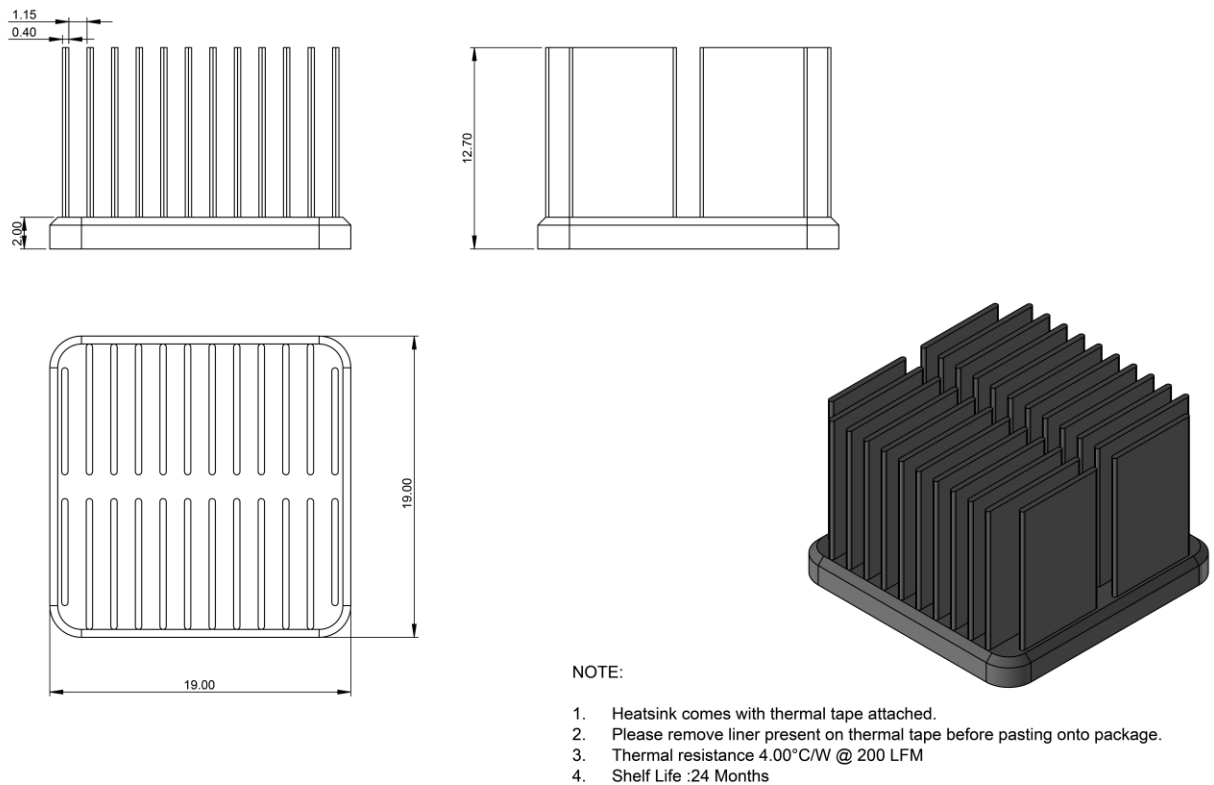


Figure 18 Mechanical Dimension of Heat sink

3.3.3 RoHS Compliance

iWave's AM62Ax Compact SBC is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.4 Electrostatic Discharge

iWave's AM62Ax Compact SBC is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SBC except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 AM62Ax Compact SBC Mechanical Dimensions

i.MX 8M Compact SBC PCB size is 100mm x 72mm x 1.2mm. Compact SBC mechanical dimension is shown below. (All dimensions are shown in mm)

The AM62Ax Compact SBC PCB thickness is 1.2mm±0.15mm, top side maximum height component is 16.40mm (HDMI Connector), followed by Dual Ethernet Connector (16.40mm). In bottom side maximum height component is JTAG connector (5.91mm) followed by M.2 SMT spacer (3.99mm).

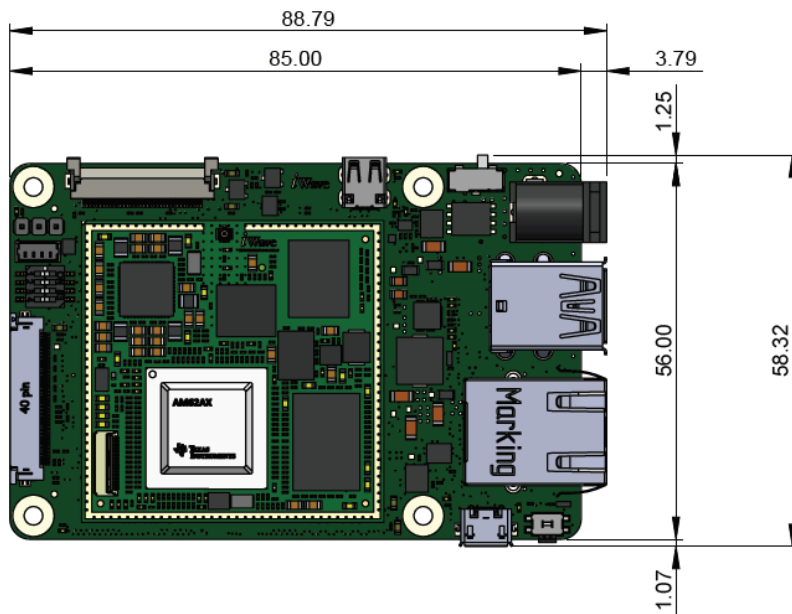


Figure 19 AM62Ax Compact SBC Mechanical Dimensions Top View

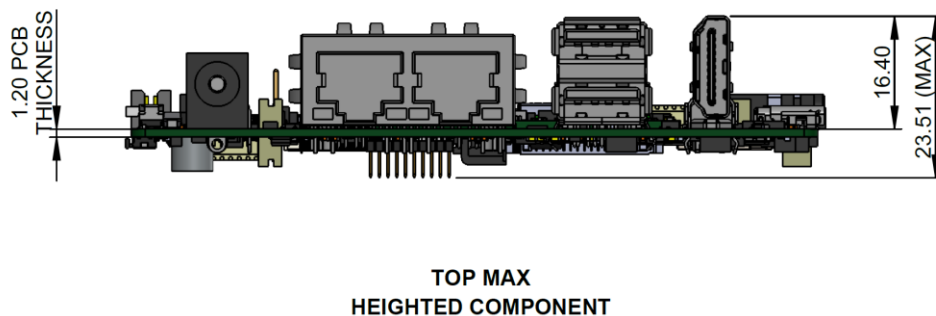


Figure 20 AM62Ax Compact SBC Mechanical Dimensions - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different AM62Ax Compact SBC variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SBC configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 17: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G55S - AM62Ax Compact SBC (industrial grade)		
iW-G55M-OL74-4L002G-E016G-BIA	AM62A74 CPU, 2GB LPDDR4, 16GB eMMC, Wi-Fi/BT SBC	-40°C to 85°C

For SBC identification purpose, Product Part Number and SBC Unique Serial Number are pasted as Label with Barcode readable format on SBC.

