1. DESCRIPTION

The XL1044T/3 is a high-speed CAN transceivers. It provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The XL1044T/3 transceiver supports both classical CAN（1Mbit/s) and CAN FD networks (up to 5Mbit/s) ,It includes internal logic level translation via the VIO terminal to allow for interfacing the transceiver I/Os directly to 3.0V or 5V logic can bus controllers (such as XL2515 and XL2518). Additionally, it supports a low-power standby mode and wake over CAN compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP). The XL1044T/3 transceiver also includes protection and diagnostic features supporting thermal-shutdown (TSD), TXD dominant time-out (DTO), supply undervoltage detection, and bus fault protection up to ±58V etc.

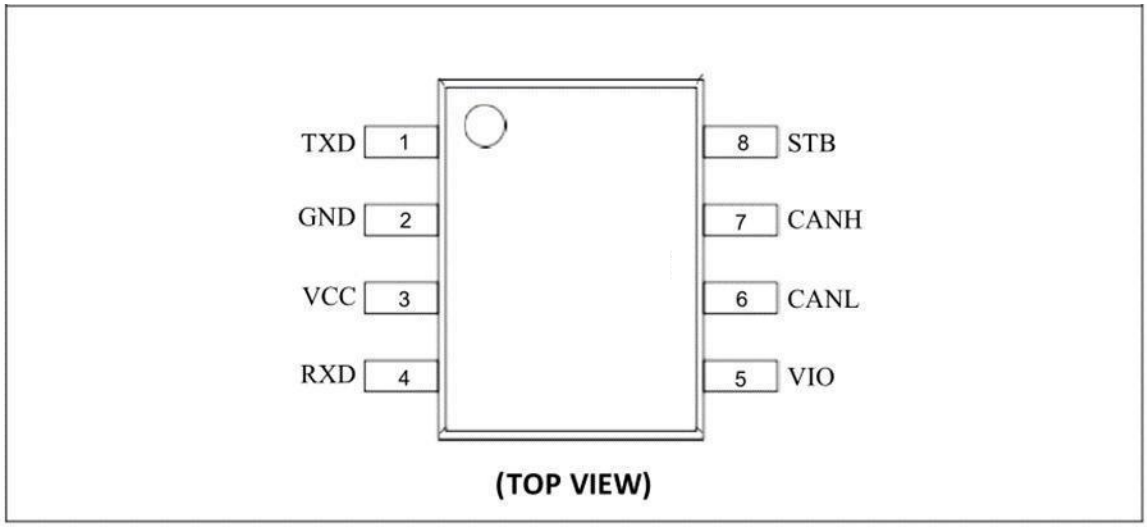
2. FEATURES

- Compliance with Physical Layer Standards: ISO 11898-2:2016 and ISO 11898-5:2007
- Support of classical CAN and optimized CAN FD communication (data rates up to 5 Mbit/s)
- Supports SAE J2962-2 and IEC 62228-3 (up to 500kbps) without the need for common-mode chokes
- Low power standby mode (10uA typical) supporting can bus wake-up
- Ideal Passive Behavior when Unpowered: High-impedance state on bus and logic pins (no load), enabling seamless power-up/power-down operation on the bus and RXD output
- With a VIO pin allow for direct interfacing with 3.0 V to 5 V microcontrollers.
- Undervoltage Protection on VCC and VIO power supplies
- Transmitter Dominant Timeout (TXD DTO) for data rates as low as 10kbps
- Thermal Shutdown Protection (TSD)
- Receiver common mode input voltage: ±27V
- Bus fault protection: ±40 V
- Operating Junction Temperature Range: **–40°C to 125°C**
- Package: Available in SOP-8 package

3. APPLICATIONS

- Telecommunication base station
- Energy storage, battery applications
- Two-wheeled vehicle

4. PIN CONFIGURATIONS AND FUNCTIONS



Pin Functions			
NAME	**TYPE**	**DESCRIPTION**	
1	TXD	Digital Input	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	GND	Ground connection
3	VCC	Power	Transceiver 5V supply voltage
4	RXD	Digital Output	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Power	Transceiver I/O level shifting supply voltage (3.0V to 5.5V)
6	CANL	Bus I/O	Low-level CAN bus input/output line
7	CANH	Bus I/O	High-level CAN bus input/output line
8	STB	Digital Input	Standby Mode control input (active high)

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	5V bus supply voltage range (VCC)	−0.3	6	V
	I/O level-shifting voltage range (VIO)	−0.3	6	V
	CAN bus I/O voltage range (CANH, CANL), VBUS	−40	40	V
	Max differential voltage between CANH and CANL,V(Diff)	−27	27	V
	Logic input terminal voltage range (TXD,STB)	−0.3	6	V
	Logic output terminal voltage range (RXD)	−0.3	+6 and VI ≤ VIO	V
Current	RXD (receiver) output, IO(RXD)	−7	7	mA
Temperature	Junction, TJ	−40	125	℃
	Storage, Tstg	−65	150	℃

NOTES:
Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD RATINGS

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge		Human-body model (HBM) CANH/CANL, per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Human-body model (HBM) Other PINs, per ANSI/ESDA/JEDEC JS- 001(1)	±4000	
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

NOTES
Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
5V Bus Supply Voltage Range	VCC	4.5	5.0	5.5	V
I/O Level-Shifting Voltage Range	VIO	3.0		5.5	V
RXD Terminal HIGH Level Output Current	IOH(RXD)	−2			mA
RXD Terminal LOW Level Output Current	IOL(RXD)			2	mA

5.4 THERMAL INFORMATION

PARAMETER	SYMBOL	TYP	UNITS
Junction-to-Ambient Thermal Resistance	RθJA	170	℃/W
Junction-to-Board Thermal Resistance	RθJB	85	℃/W

5.5 ELECTRICAL CHARACTERISTICS

TA = –40°C to 125°C, VCC = 4.5V to 5.5V, VIO = 3.0V to 5.5V, RL = 60Ω, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CHARACTERISTICS						
5V Supply Current	ICC	Normal mode (dominant), TXD = 0V, RL = 60Ω , CL =open, RCM = open, STB= 0V, typical bus load		45		mA
		Normal mode (dominant), TXD = 0V, RL = 50Ω , CL =open, RCM = open, STB = 0V, high bus load		48		mA
		Normal mode (dominant – with bus fault), TXD = 0V, STB= 0V, CANH = – 12V, RL =open, CL = open, RCM = open		55		mA
		Normal mode (recessive), TXD = VCC or VIO, RL = 50Ω , CL = open, RCM = open, STB = 0V		1.5	5	mA
		STB mode, d VCC not needed in Standby mode, TXD = VIO, RL = 50Ω , CL = open, RCM = open, STB = VIO		0.5	3	mA
I/O Supply Current	IIO	Normal mode, recessive, RXD floating, TXD = STB = 0V		60		µA
		Normal mode, Dominant, RXD floating, TXD = STB = 0V		150		µA
		Standby mode: RXD floating, TXD = STB = VIO, VCC = 0 or 5.5 V		11	20	µA
Rising Undervoltage Detection on VCC for Protected Mode	UVVCC			4.2	4.4	V
Falling Undervoltage Detection on VCC for Protected Mode			3.5	4.0	4.25	V
Hysteresis Voltage on UVVCC	VHYS(UVVCC)			200		mV
Undervoltage Detection on VIO for Protected Mode	UVVIO	rising under voltage detection on VIO		2.0	2.5	V
		falling under voltage detection on VIO	1.7	1.8	2.0	V
Hysteresis Voltage on UVVIO for Protected Mode	VHYS(UVVIO)			300		mV
STB TERMINAL (MODE SELECT INPUT)						
High-Level Input Voltage	VIH		0.7× VIO			V
Low-Level Input Voltage	VIL				0.3× VIO	V
High-Level Input Leakage Current	IIH	S = VCC = VIO = 5.5V	–3		3	µA
Low-Level Input Leakage Current	IIL	S = 0V, VCC = VIO = 5.5V	–15	0	–2	µA
Unpowered Leakage Current	Ilkg(OFF)	S = 5.5V, VCC = VIO = 0V	–2	0	2	µA
TXD TERMINAL (CAN TRANSMIT DATA INPUT)						
High-Level Input Voltage	VIH		0.7× VIO			V
Low-Level Input Voltage	VIL				0.3× VIO	V
High-Level Input Leakage Current	IIH	TXD = VCC = VIO = 5.5V	–3	0	2	µA
Low-Level Input Leakage	IIL	TXD = 0V, VCC = VIO = 5.5V	–200	–150	–100	µA

Current						
Unpowered Leakage Current	Ilkg(OFF)	TXD = 5.5V, VCC = VIO = 0V	–2	0	2	µA
Input Capacitance	CI	VIN =0.4 × sin(2 × π × 2 × 106 × t) + 2.5V		8		pF
RXD TERMINAL (CAN RECEIVE DATA OUTPUT)						
High-Level Output Current	IOH	VRXD = VIO - 0.4V	-8	-3	-1	mA
						mA
Low-Level Output Current	IOL	VRXD = 0.4V, bus dominant	1		8	mA
DRIVER ELECTRICAL CHARACTERISTICS						
Bus Output Voltage (Dominant), CANH	VO(DOM)	TXD = 0V, STB = 0V, 50Ω ≤ RL ≤ 65Ω, CL = open, RCM = open	2.75		4.5	V
Bus Output Voltage (Dominant), CANL			0.5		2.25	V
Bus Output Voltage (Recessive), CANH and CANL	VO(REC)	TXD = VCC or VIO, VIO = VCC, STB = 0V, RL = open (noload), RCM = open	2	0.5× VCC	3	V
Differential Output Voltage (Dominant), CANH - CANL	VOD(DOM)	TXD = 0V, STB = 0V, 50Ω ≤ RL < 65Ω, CL = open, RCM = open	1.2		3	V
		TXD = 0V, STB = 0V, 45Ω ≤ RL ≤ 70Ω, CL = open, RCM = open	1.0		3	V
		TXD = 0V, STB = 0V, RL = 2240Ω, CL = open, RCM = open	1.3		5	V
Differential Output Voltage (Recessive), CANH - CANL	VOD(REC)	TXD = VCC, STB = 0V, RL = 60Ω, CL = open, RCM = open	–100		20	mV
		TXD = VCC, STB = 0V, RL = open (no load), CL =open, RCM = open	–50		50	mV
Output Symmetry (Dominant or Recessive) (VO(CANH) + VO(CANL)) / VCC	VSYM	STB at 0V, Rterm = 60Ω , Csplit = 4.7nF, CL = open, RCM = open, TXD = 1MHz	0.9		1.1	V/V
DC Output Symmetry (Dominant or Recessive) (VCC – VO(CANH) –	VSYM_DC	STB = 0V, RL = 60Ω, CL = open, RCM = open	–0.6		0.6	V
Short-Circuit Steady-State Output Current, Dominant, Normal Mode	IOS(SS_DOM)	STB at 0V, VCANH = -5V to 40V, CANL = open, TXD = 0V	–100			mA
		STB at 0V, VCANL = –5V to 40V, CANH = open, TXD = 0V			100	mA
Short-Circuit Steady-State Output Current, Recessive, Normal Mode	IOS(SS_REC)	STB at 0V, –27V ≤ VBUS ≤ 32V, where VBUS = CANH = CANL, TXD = VCC	–10		10	mA

5.6 SWITCHING CHARACTERISTICS

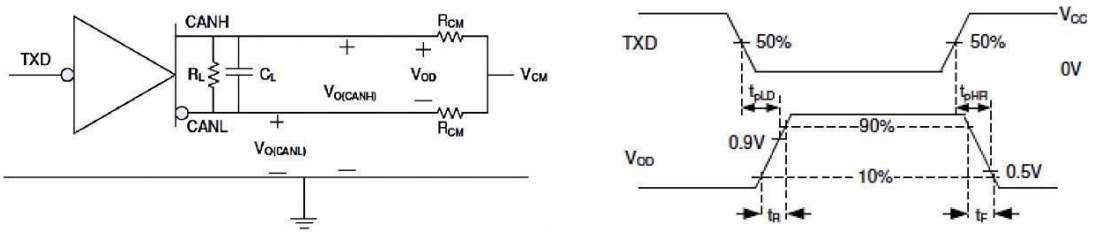
TA = –40°C to 125°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER ELECTRICAL CHARACTERISTICS						
Common-Mode Range, Normal Mode	VCM	STB = 0V	–30		30	V
Positive-Going Input Threshold Voltage, Normal Mode	VIT+	STB = 0V, –20V ≤ VCM ≤ +20V			1100	mV
Negative-Going Input Threshold Voltage, Normal Mode	VIT–		500			mV
Positive-Going Input Threshold Voltage, Normal Mode	VIT+	STB = 0V, –30V ≤ VCM ≤ +30V			1200	mV
Negative-Going Input Threshold Voltage, Normal Mode	VIT–		400			mV

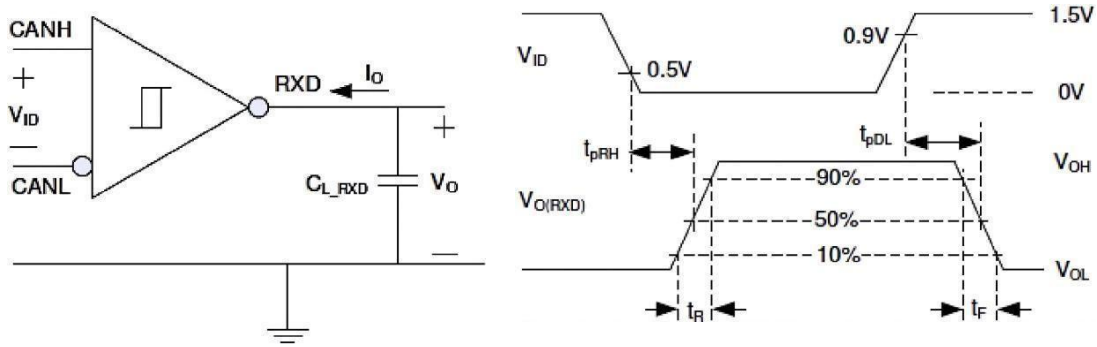
Hysteresis Voltage (VIT+ – VIT –), Normal Mode	VHYS	STB = 0V			135	mV
Common-Mode Range, Standby Mode	VCM	Devices with the "V" suffix (I/O level-shifting), STB = VIO, 4.5V≤ VIO ≤ 5.5V	– 12		12	V
		Devices with the "V" suffix (I/O level-shifting), STB = VIO, 3.0V ≤ VIO ≤ 4.5V	–2		7	V
Input Threshold Voltage, Standby Mode	VIT(STANDBY)	STB = VCC or VIO	500		1200	mV
Input Capacitance to Ground (CANH or CANL)	CI	TXD = VCC, VIO = VCC		24	30	pF
Differential Input Capacitance (CANH to CANL)	CID	TXD = VCC, VIO = VCC		12	15	pF
Differential Input Resistance	RID	TXD = VCC = VIO = 5V, S = 0V, −30V ≤ VCM ≤+30V	40	49	90	kΩ
Input Resistance (CANH or CANL)	RIN		20	25	45	kΩ
Input Resistance Matching: [1 – RIN(CANH) / RIN(CANL)] × 100%	RIN(M)	VCANH = VCANL = 5V	−5%		5%	kΩ
DEVICE SWITCHING CHARACTERISTICS						
Total Loop Delay, Driver Input (TXD) to Receiver Output (RXD), Recessive to Dominant	tPROP(LOOP1)	STB = 0V, RL = 60Ω , CL = 100pF, CL(RXD) = 15pF		60	100	ns
Total Loop Delay, Driver Input (TXD) to Receiver Output (RXD), Dominant to Recessive	tPROP(LOOP2)			62	100	ns
Mode Change Time, From Normal to STB or From STB to Normal	tMODE			17	30	µs
Long Filter Time for Valid Wake-Up Pattern	tWK_FILTER		0.5		3.0	µs
Short Filter Time for Valid Wake-Up Pattern	tWK_FILTER		0.5		5	µs
DRIVER SWITCHING CHARACTERISTICS						
Propagation Delay Time, High TXD to Driver Recessive (Dominant to Recessive)	tpHR	STB = 0V, RL = 60Ω , CL = 100pF, RCM = open		80		ns
Propagation Delay Time, Low TXD to Driver Dominant (Recessive to Dominant)	tpLD			70		ns
Pulse Skew (|tpHR – tpLD |)	tsk(p)			20		ns
Differential Output Signal Rise Time	tR			30		ns
Differential Output Signal Fall Time	tF			50		ns
Dominant Timeout	tTXD_DTO	STB = 0V, RL = 60Ω , CL = open	2		10	ms
RECEIVER SWITCHING CHARACTERISTICS						
Propagation Delay Time, Bus Recessive Input to High Output (Dominant to Recessive)	tpRH	STB = 0V, CL(RXD) = 15pF		60		ns
Propagation Delay Time, Bus Dominant Input to Low Output (Recessive to Dominant)	tpDL			65		ns
RXD Output Signal Rise Time	tR			10		ns
RXD Output Signal Fall Time	tF			10		ns
FD TIMING PARAMETERS						
Bit Time on CAN Bus Output Pins with tBIT(TXD) = 500ns, All Devices	tBIT(BUS)		400		600	ns
Bit Time on CAN Bus Output Pins with tbit(TXD) = 200ns, G Device			125		250	ns
Power-Off (Unpowered) Bus Input Leakage Current	ILKG(IOFF)	CANH = CANL = 5V, VCC = VIO = 0V			10	µA

Bit Time on RXD Output Pins with tbit(TXD) = 500ns, All Devices	tBIT(RXD)	STB = 0V, RL = 60Ω, CL = 100pF, CL(RXD) = 15pF, ΔtREC = tBIT(RXD) – tBIT(BUS)	400		650	ns
Bit Time on RXD Output Pins with tbit(TXD) = 200ns, G Device Variants Only			120		260	ns
Receiver Timing Symmetry with tbit(TXD) = 500ns, All Devices	ΔtREC		−65		60	ns
Receiver Timing Symmetry with tbit(TXD) = 200ns, G Device Variants Only			−45		20	ns

6. PARAMETER MEASUREMENT INFORMATION

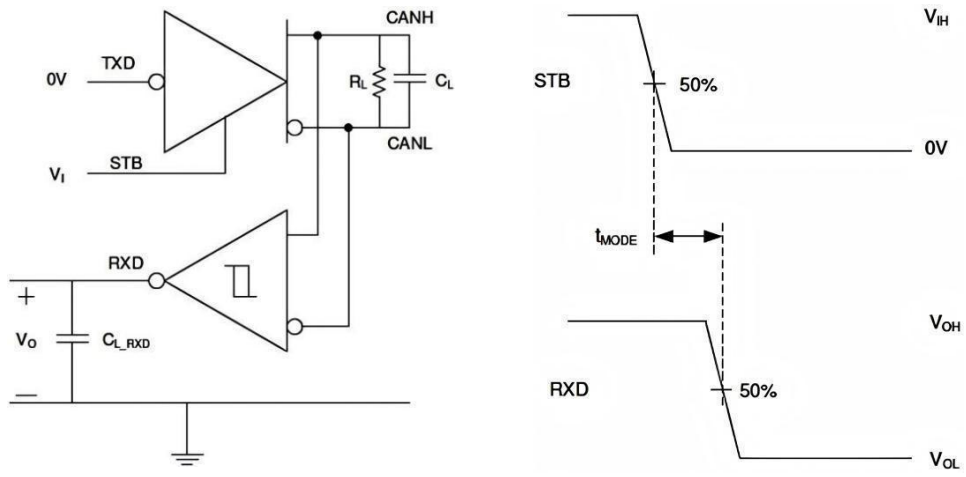


Driver Test Circuit and Measurement

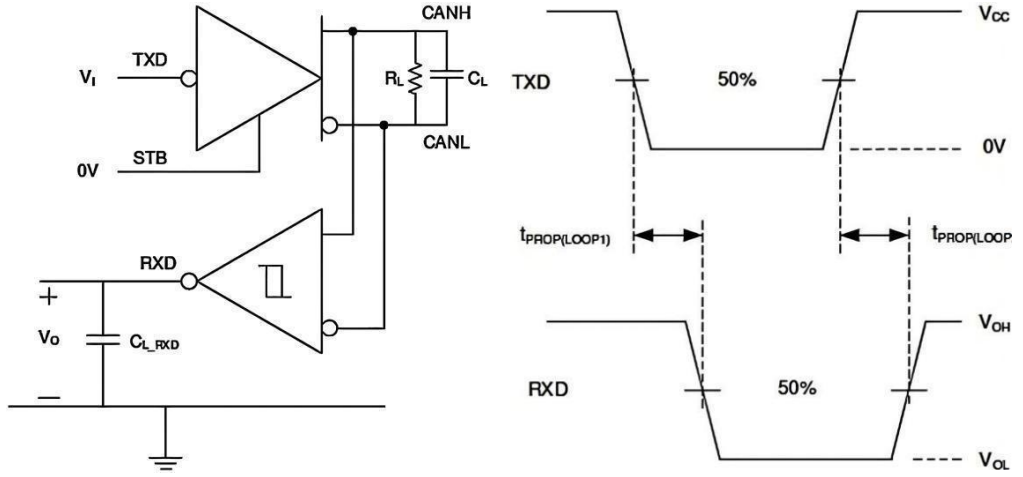


Receiver Test Circuit and Measuremen

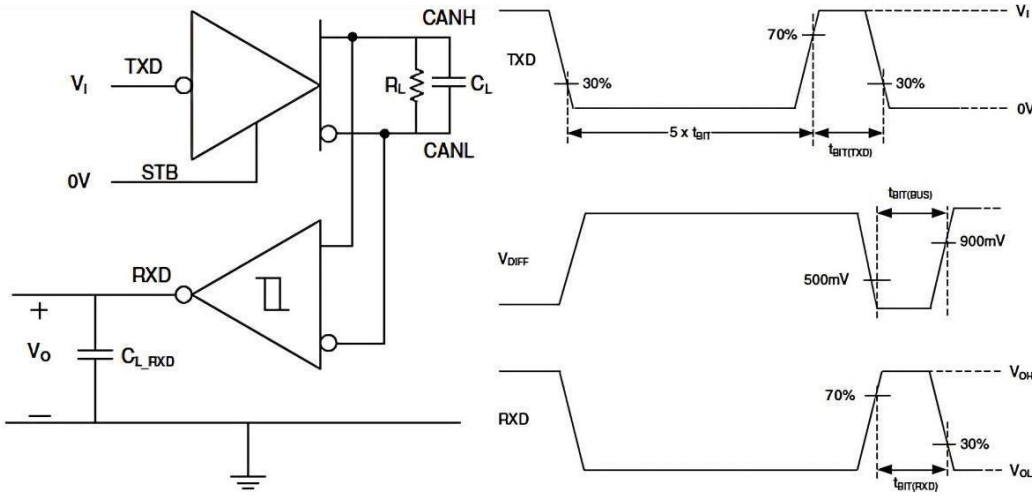
Receiver Differential Input Voltage Threshold Test				
INPUT			**OUTPUT**	
VCANH	**VCANL**	**|VID |**	**RXD**	
−29.5V	−30.5V	1000mV	L	VOL
30.5V	29.5V	1000mV	L	
− 19.55V	−20.45V	900mV	L	
20.45V	19.55V	900mV	L	
− 19.75V	−20.25V	500mV	H	VOH
20.25V	19.75V	500mV	H	
−29.8V	−30.2V	400mV	H	
30.2V	29.8V	400mV	H	
Open	Open	X	H	



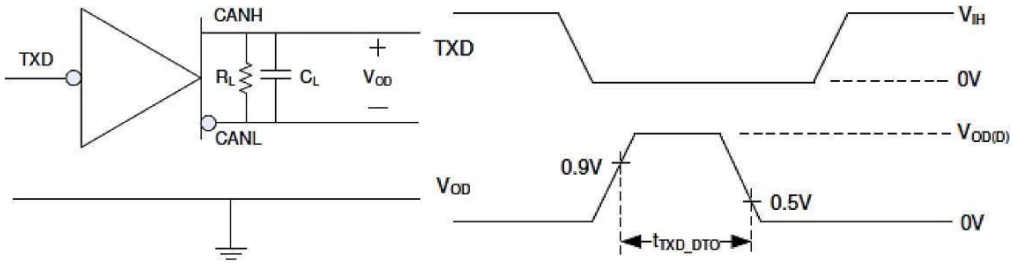
t_{MODE} Test Circuit and Measurement



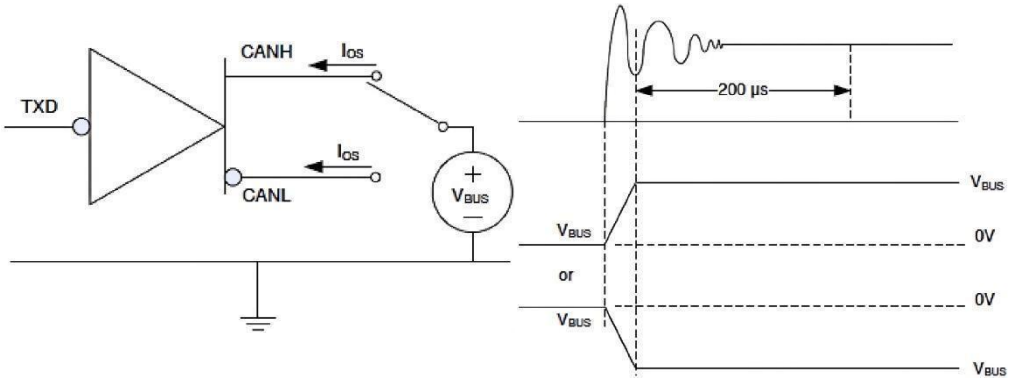
$T_{PROP(LOOP)}$ Test Circuit and Measurement



CAN FD Timing Parameter Measurement



TXD Dominant Timeout Test Circuit and Measurement



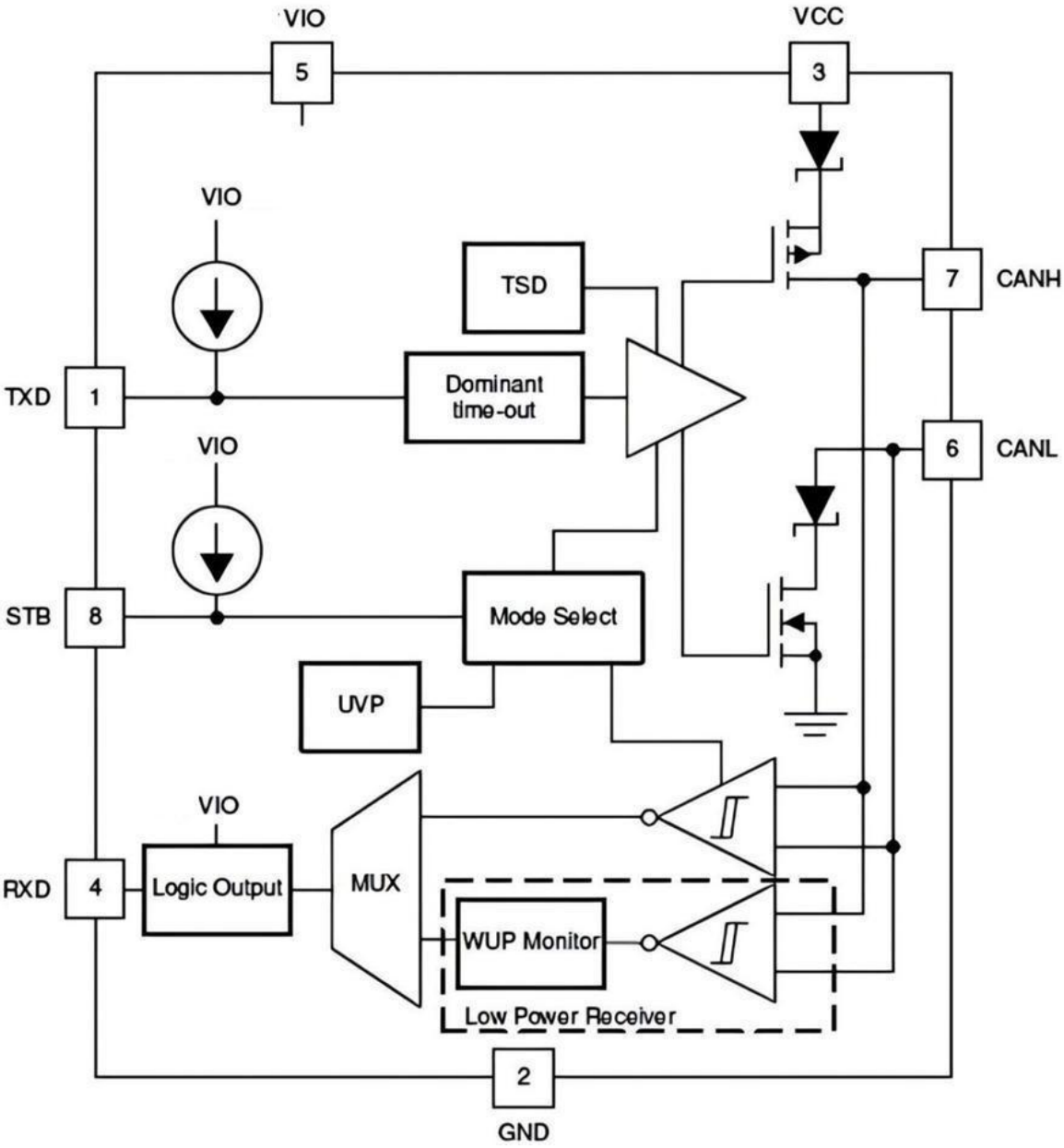
Driver Short Circuit Current Test and Measurement

7. DETAILED DESCRIPTION

7.1 Overview

The CAN transceiver XL1044/T3 adhere to the ISO 11898-2 (2016) standard for the high-speed CAN (Controller Area Network) physical layer. They are specifically engineered for CAN FD networks that exceed 1 Mbps data rates, offering enhanced timing margins for higher data transfer rates in long-distance and high-load scenarios. These devices incorporate numerous protection features that bolster the robustness of both the transceivers themselves and the CAN network as a whole.

7.2 Functional Module Block Diagram

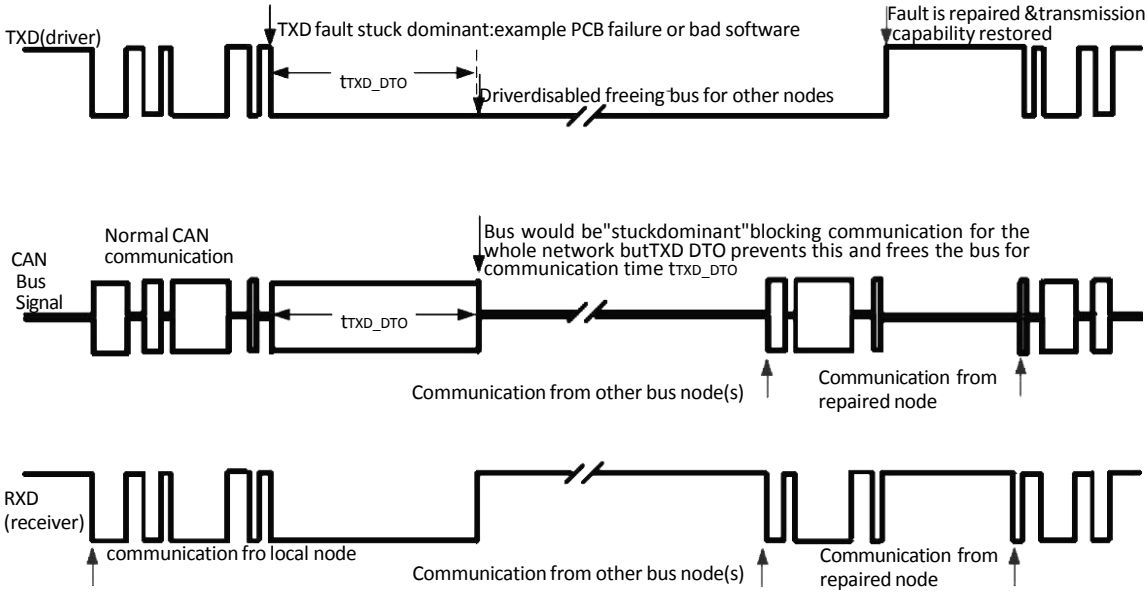


Functional Block Diagram

7.3 Feature Description

7.3.1 TXD Dominant Timeout (DTO)

During normal mode, which is the sole mode where the CAN driver is active, the TXD DTO (Dominant Timeout) circuitry prevents the transceiver from blocking network communication in the event of a hardware or software fault, where TXD remains in the dominant state for longer than the timeout period, tTXD_DTO. The DTO circuit timer initiates upon the falling edge of TXD. If a rising edge is not observed before the timeout expires, the DTO circuitry disables the CAN bus driver, thereby releasing the bus for communication among other nodes on the network. When a recessive signal is detected on the TXD terminal, the CAN driver is reactivated, clearing the TXD DTO condition. The receiver and RXD terminal continue to reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during the TXD dominant timeout period.



Example Timing Diagram for TXD DTO

The minimum dominant TXD time allowed by the TXD DTO (Dominant Timeout) circuitry imposes a limit on the minimum possible transmission data rate of the device. In the worst-case scenario, the CAN protocol permits up to 11 consecutive dominant bits (on TXD), with 5 consecutive dominant bits immediately following an error frame. This, in conjunction with the minimum value of tTXD_DTO, restricts the minimum achievable data rate. The minimum data rate can be calculated using the following formula: Minimum Data Rate = 11 / tTXD_DTO.

7.3.2 Thermal Shutdown (TSD)

If the device's junction temperature exceeds the thermal shutdown threshold (TTSD), the CAN driver circuitry is shut down by the device, effectively blocking the transmission path from TXD to the bus. During this thermal shutdown, the CAN bus terminals are biased to the recessive level, while the receiver to RXD path remains operational. The shutdown condition is cleared when the junction temperature falls below the thermal shutdown hysteresis temperature (TTSD_HYS), which is a temperature threshold lower than the device's thermal shutdown temperature (TTSD).

7.3.3 Under-Voltage Lockout (UVLO)

The power supply terminals are equipped with under-voltage detection functionality, which can put the device into a protection mode. This can safeguard the bus during under-voltage events occurring on the VIO power terminals.

Undervoltage Lockout I/O Level Shifting Devices (Devices with the "V" Suffix)				
VCC	**VIO**	**DEVICE STATE**	**BUS OUTPUT**	**RXD**
> UVVCC	> UVVIO	Normal	Per TXD	Mirrors Bus(1)
< UVVCC	> UVVIO	Protected	High Impedance	High (Recessive)
> UVVCC	< UVVIO	Protected	High Impedance	High Impedance
< UVVCC	< UVVIO	Protected	High Impedance	High Impedance

Notes

(1) Mirror bus status: It is low if the CAN bus is dominant; it is high if the CAN bus is recessive.

(2) After the under-voltage condition is cleared and the power supply returns to a valid level, the device will usually resume normal operation within 50μs.

7.3.4 Passive device

This device is designed to be "ideally passive" or "unloaded" on the CAN bus when unpowered. When the device is not energized, the bus terminals (CANH, CANL) exhibit extremely low leakage currents to prevent any degradation of the bus load. This is crucial in scenarios where some nodes of the network are powered down while the rest of the network remains operational. Additionally, when the device is unpowered, the logic terminals also maintain extremely low leakage currents to avoid loading other circuits that may remain energized.

7.3.5 Floating terminal

These devices incorporate internal pull-up resistors on critical terminals to place the device in a known state when the terminals are floating. The TXD terminal is pulled up to VIO, enforcing a recessive input level when the terminal is floating. Similarly, if left unconnected, the STB terminal is also pulled low to force the device into normal mode.

7.3.6 CAN bus short circuit current limiting

The device incorporates two protection mechanisms to limit short-circuit current during CAN bus line faults: driver current limitation (in both dominant and recessive states) and TXD dominant state timeout, preventing persistent high short-circuit current in the dominant state during system faults. During CAN communication, the bus alternates between dominant and recessive states, hence the short-circuit current can be viewed as either an instantaneous current during each bus state or an average current over both states. For system current (power) and power considerations in terminal resistance and common-mode choke ratings, the average short-circuit current is used. The ratio of dominant to recessive bits is determined by the CAN frame data, alongside protocol and PHY factors that enforce either recessive or dominant states at specific times, including:

- Control fields with set bits
- Bit stuffing
- Interframe spacing
- TXD dominant timeout (for fault condition mitigation)

These factors ensure minimal recessive time on the bus, even when the data field contains a high proportion of dominant bits. The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current can be calculated using the formula:

$$IOS(AVG) = \%Transmit \times [(\%REC\_Bits \times IOS(SS)\_REC) + (\%DOM\_Bits \times IOS(SS)\_DOM)] + [\%Receive \times IOS(SS)\_REC]$$

Where:

- IOS(AVG) represents the average short-circuit current.
- %Transmit is the percentage of CAN messages transmitted by the node.
- %Receive is the percentage of CAN messages received by the node.
- %REC_Bits is the percentage of recessive bits in transmitted CAN messages.
- %DOM_Bits is the percentage of dominant bits in transmitted CAN messages.
- IOS(SS)_REC denotes the recessive steady-state short-circuit current.
- IOS(SS)_DOM denotes the dominant steady-state short-circuit current.

Note: When determining the power ratings for terminal resistors and other network components, consider the short-circuit current of the network and potential fault scenarios.

7.3.7 Digital input and output

7.3.7.1 5V VCC with VIO I/O level conversion

These devices employ a 5V VCC power supply for CAN drivers and high-speed receiver modules. These transceivers feature a secondary power supply for I/O level shifting (VIO), which is utilized to set the CMOS input thresholds for the TXD and STB pins, as well as the RXD high- level output voltage. Notably, the TXD pin is internally pulled up to VIO, whereas the STB pin is pulled down to GND.

7.4 Device functional mode

The device operates in two primary modes: Normal Mode and Silent Mode. The selection of the operating mode is made through the S input terminal.

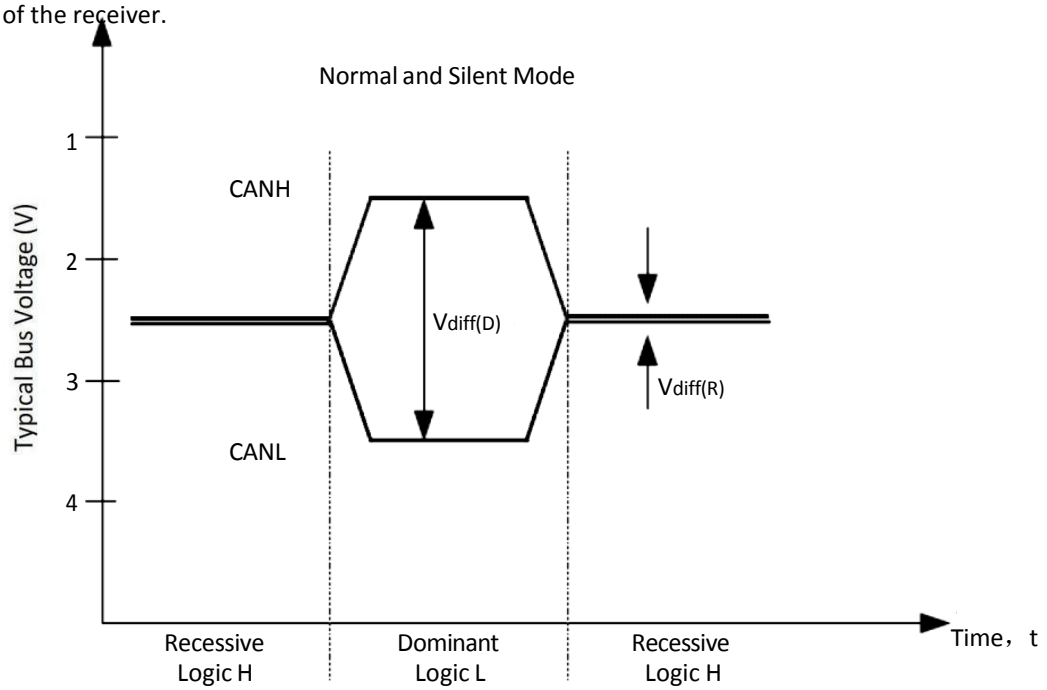
Operating Modes				
S TERMINAL	**MODE**	**DRIVER**	**RECEIVER**	**RXD TERMINAL**
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	STB Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State(1)

Note:

(1)Mirror bus state: If the CAN bus is dominant, it is low; if the CAN bus is recessive, it is high.

7.4.1 CAN Bus State

The CAN bus exhibits two states during the powered operation of devices: dominant and recessive. The dominant bus state corresponds to a logical low level on the TXD and RXD terminals when the bus is differentially driven. In contrast, the recessive bus state corresponds to a logical high level on the TXD and RXD terminals when the bus is biased to VCC/2 through the high-impedance internal input resistance (RIN) of the receiver.



Bus States (Physical Bit Representation)

The normal operating mode of the device is selected by setting the STB terminal to a low level, allowing the CAN driver and receiver to be fully operational and enabling bidirectional CAN communication. The driver converts digital inputs on the TXD into differential outputs on CANH and CANL, while the receiver translates differential signals from CANH and CANL into digital outputs on RXD.

7.4.2 Standby Mode

The Standby mode is activated by setting the STB terminal to a high level. In standby mode, the BUS end has very low leakage and power consumption. The chip is in the standby state.

7.4.3 Driver and Receiver Function Table

DriverFunction Table					
DEVICE	INPUTS		OUTPUTS		DRIVEN BUSSTATE
	STB(1)	TXD(1)(2)	CANH(1)	CANL(1)	
All Devices	L or open	L	H	L	Dominant
		H or open	Z	Z	Recessive
	H	X	Z	Z	Recessive

Notes

(1) H = high level, L = low level, X = irrelevant, Z = VCC / 2. For information about bus status and common mode bias, see CAN BUS STATES.

(2) The device has an internal pull-up to the VCC on the TXD terminal. If the TXD terminal is open, the terminal is pulled up and the transmitter remains hidden (non-driven).

Receiver Function Table			
DEVICE MODE	CAN DIFFERENTIAL INPUTS VID = VCANH – VCANL	BUS STATE	RXD TERMINAL(1)
Normal or STB	VID ≥ VIT+(MAX)	Dominant	L(2)
	VIT-(MIN) < VID < VIT+(MAX)	?	?(2)
	VID ≤ VIT-(MIN)	Recessive	H(2)
	Open (VID ≈ 0V)	Open	H

Notes

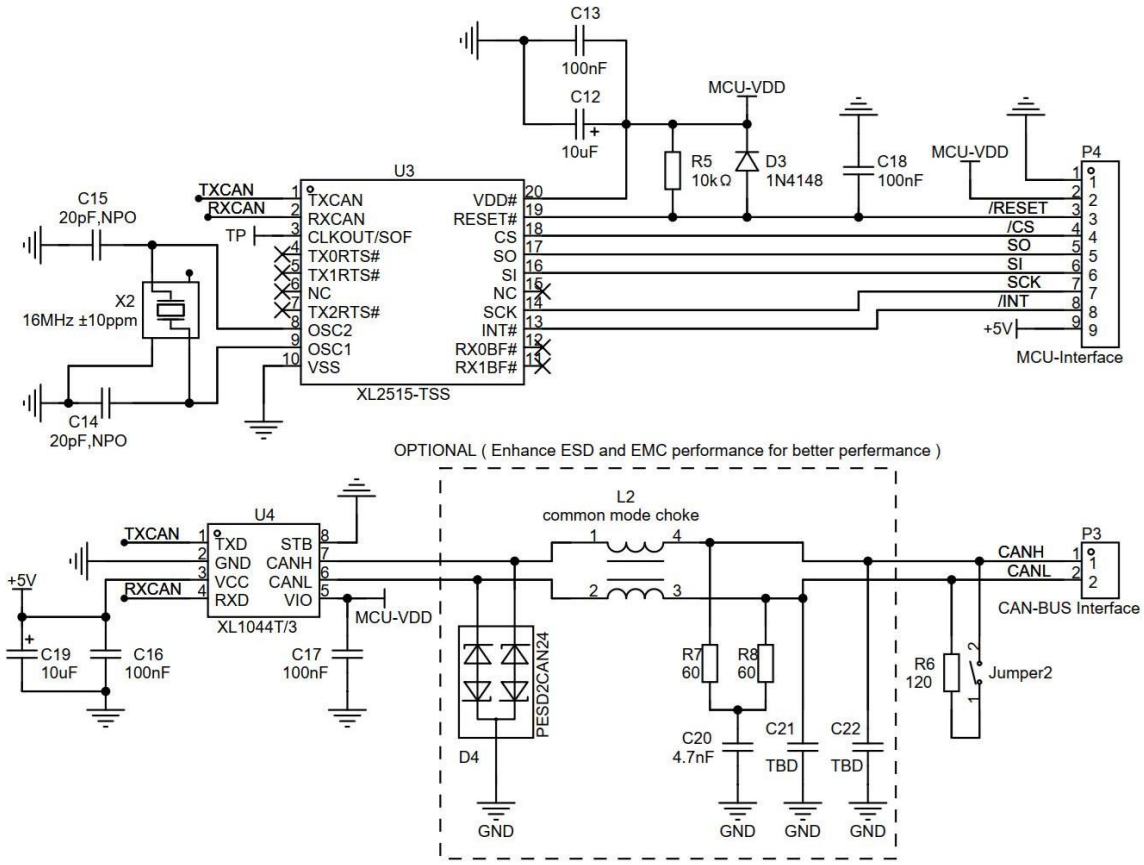
(1) H = high level, L = low level,?= indeterminacy.

(2) For information on the input thresholds, see the ELECTRICAL CHARACTERISTICS section.

8. Application and implementation

8.1 Application message

As shown in the figure below , U1 and U2 form a minimal application system for a CAN-BUS bus. In this circuit, U1 (XL2515) is an independent CAN bus controller with SPI interface, while U2 (XL1044T/3) is a CAN-BUS interface transceiver chip. Any MCU (DSP or FPGA) with a SPI interface can connected to P1 will be able to transmit and receive CAN-BUS bus frame data. The normal operating voltage range of MCU-VDD is +3.0V ~ 5.0V.



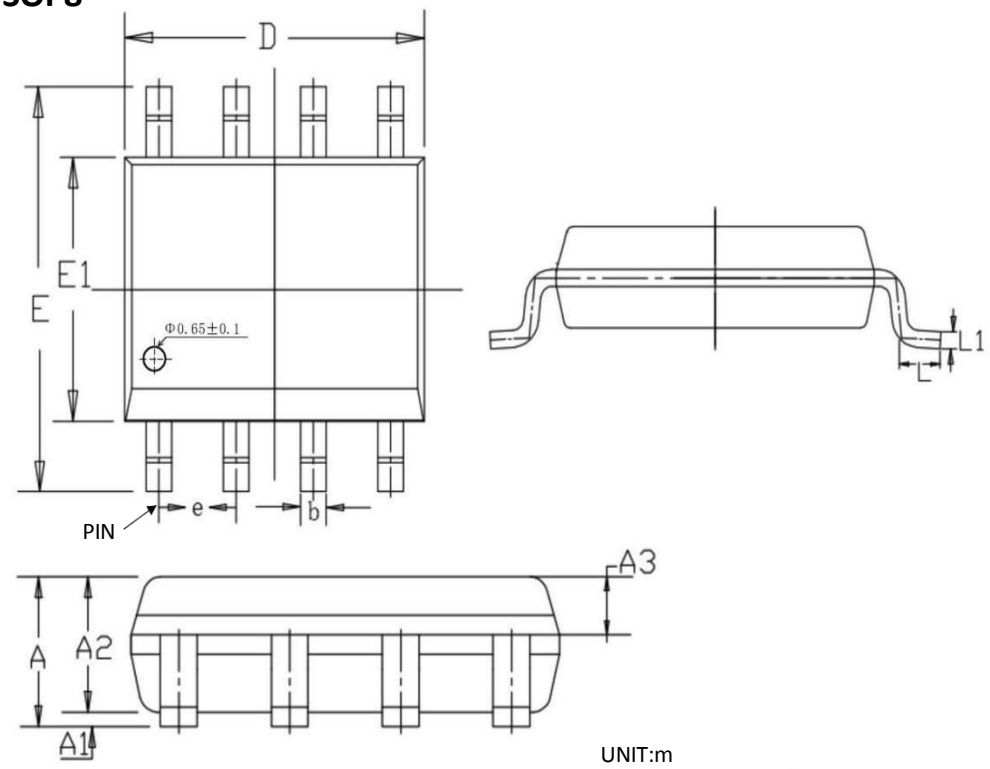
9. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL1044T/3	XL1044T3	SOP8	4.90 * 3.90	-40 to +125	MSL3	T&R	2500

10. DIMENSIONAL DRAWINGS

SOP8



UNIT:m

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E	3.800	3.900	4.000
1	0.450	0.600	0.750
L1	–	0.25BSC	–