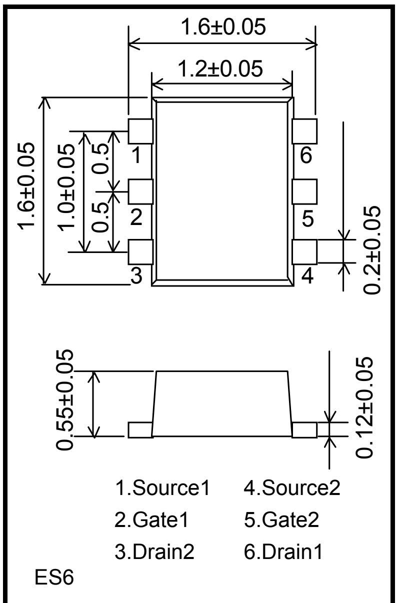
TOSHIBA Field-Effect Transistor Silicon N / P Channel MOS Type

SSM6L14FE

○ Power Management Switch Applications
○ High-Speed Switching Applications

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-2N1D

Weight: 3.0 mg (typ.)

- N-ch: 1.5-V drive
  P-ch: 1.5-V drive
- N-ch, P-ch, 2-in-1
- Low ON-resistance Q1 N-ch: $R_{DS(ON)}$ = 330 mΩ (max) (@V_{GS} = 2.5 V)
  $R_{DS(ON)}$ = 240 mΩ (max) (@V_{GS} = 4.5 V)
  Q2 P-ch: $R_{DS(ON)}$ = 440 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 300 mΩ (max) (@V_{GS} = -4.5 V)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	20	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	0.8	A
	Pulse	I_{DP}	1.6	

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−20	V
Gate-source voltage		V_{GSS}	±8	V
Drain current	DC	I_D	−0.72	A
	Pulse	I_{DP}	−1.44	

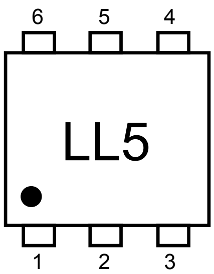
Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

Characteristics	Symbol	Rating	Unit
Power dissipation	P_D(Note 1)	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

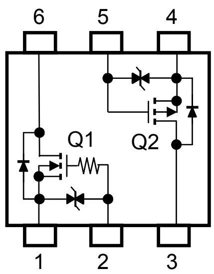
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation)
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.135 mm^2 × 6)

Marking



Equivalent Circuit (top view)



Start of commercial production
2009-12

Q1 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0 V	20	—	—	V
		$V_{(BR)DSX}$	I_D = 1 mA, V_{GS} = - 10 V	12	—	—	
Drain cutoff current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.35	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 500 mA (Note 2)	1.05	2.1	—	S
Drain-source ON-resistance		$R_{DS (ON)}$	I_D = 500 mA, V_{GS} = 4.5 V (Note 2)	—	185	240	mΩ
			I_D = 400 mA, V_{GS} = 2.5 V (Note 2)	—	245	330	
			I_D = 250 mA, V_{GS} = 1.8 V (Note 2)	—	310	450	
			I_D = 150 mA, V_{GS} = 1.5 V (Note 2)	—	370	600	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	90	—	pF
Output capacitance		C_{oss}		—	21	—	
Reverse transfer capacitance		C_{rss}		—	15	—	
Total gate charge		Q_g	V_{DS} = 10 V, I_D = 0.8 A V_{GS} = 4.5 V	—	2.00	—	nC
Gate-source charge		Q_{gs}		—	1.02	—	
Gate-drain charge		Q_{gd}		—	0.98	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 200 mA V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω	—	18	—	ns
	Turn-off time	t_{off}		—	50	—	
Drain-source forward voltage		V_{DSF}	I_D = -0.8 A, V_{GS} = 0 V (Note 2)	—	-0.84	-1.2	V

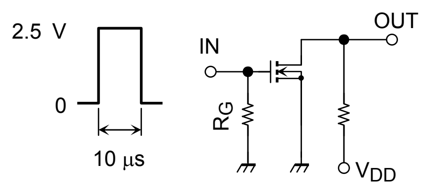
Q2 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
		$V_{(BR)DSX}$	I_D = -1 mA, V_{GS} = 8 V	-12	—	—	
Drain cutoff current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-10	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -400 mA (Note2)	850	—	—	mS
Drain-source ON-resistance		$R_{DS (ON)}$	I_D = -400 mA, V_{GS} = -4.5 V (Note2)	—	0.25	0.30	Ω
			I_D = -200 mA, V_{GS} = -2.5 V (Note2)	—	0.34	0.44	
			I_D = -100 mA, V_{GS} = -1.8 V (Note2)	—	0.44	0.67	
			I_D = -50 mA, V_{GS} = -1.5 V (Note2)	—	0.55	1.04	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	110	—	pF
Output capacitance		C_{oss}		—	28	—	
Reverse transfer capacitance		C_{rss}		—	20	—	
Total gate charge		Q_g	V_{DS} = -10 V, I_{DS}= -720 mA V_{GS} = -4.5 V	—	1.76	—	nC
Gate–source charge		Q_{gs}		—	1.22	—	
Gate–drain charge		Q_{gd}		—	0.54	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -100 mA V_{GS} = 0 to -2.5 V, R_G = 50 Ω	—	11	—	ns
	Turn-off time	t_{off}		—	38	—	
Drain-source forward voltage		V_{DSF}	I_D = 720 mA, V_{GS} = 0 V (Note2)	—	0.85	1.2	V

Note 2: Pulse test

Q1 Switching Time Test Circuit

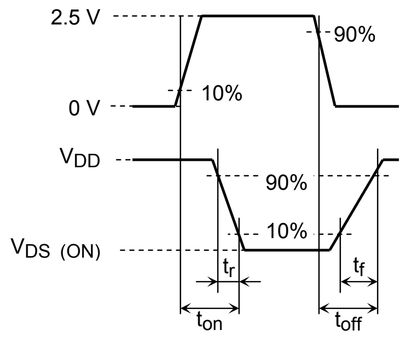
(a) Test Circuit



V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

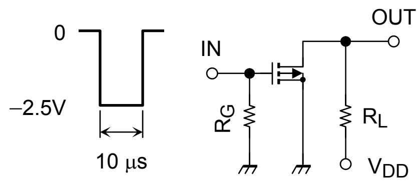
(b) V_{IN}

(c) V_{OUT}



Q2 Switching Time Test Circuit

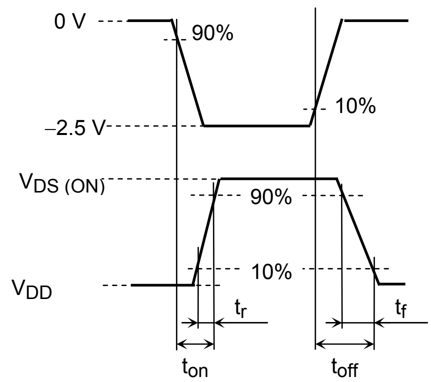
(a) Test Circuit



V_{DD} = − 10 V
R_G = 50 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Q1 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the Q1 of the SSM6L14FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

Q2 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (−1 mA for the Q2 of the SSM6L14FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

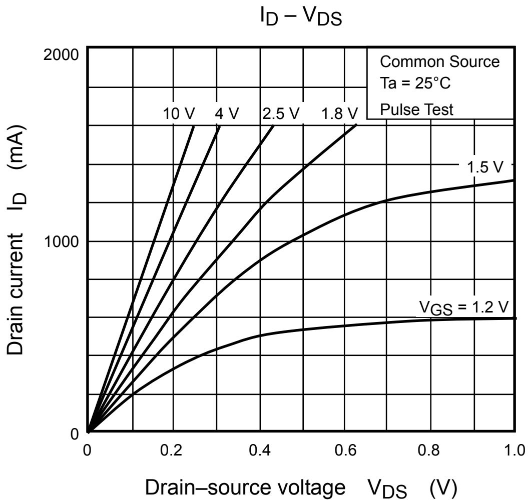
Take this into consideration when using the device.

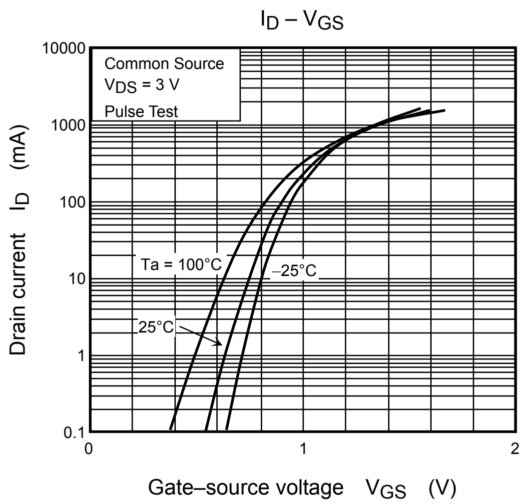
Handling Precaution

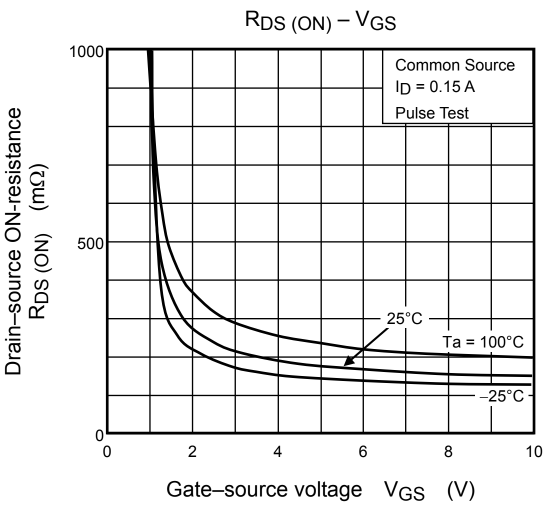
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

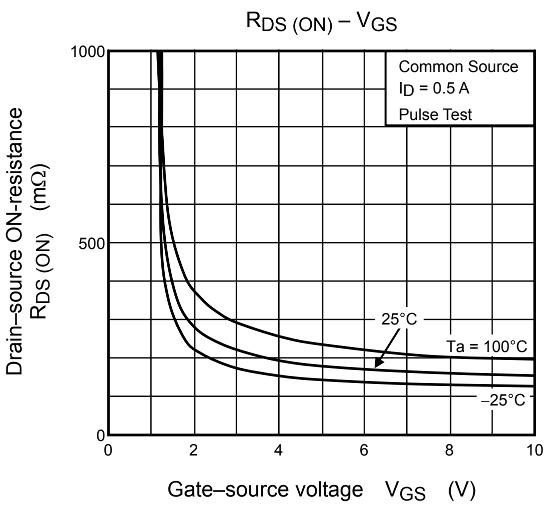
Thermal resistance $R_{th\ (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

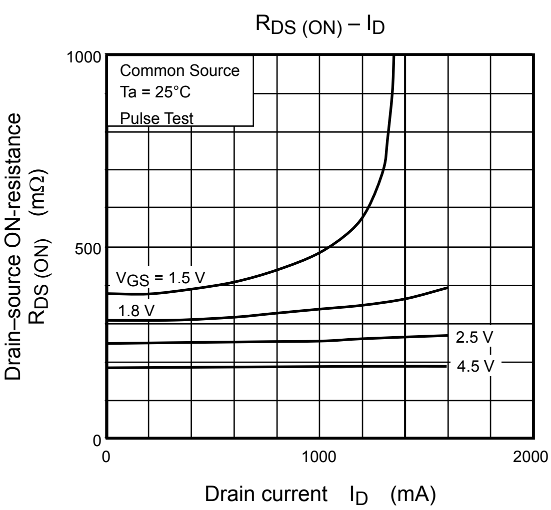
Q1 (N-ch MOSFET)

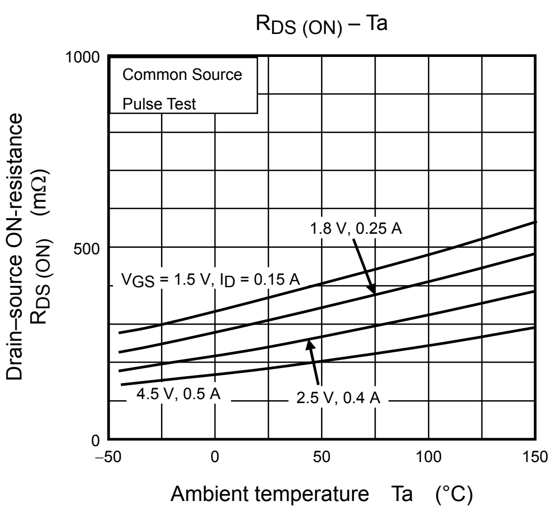




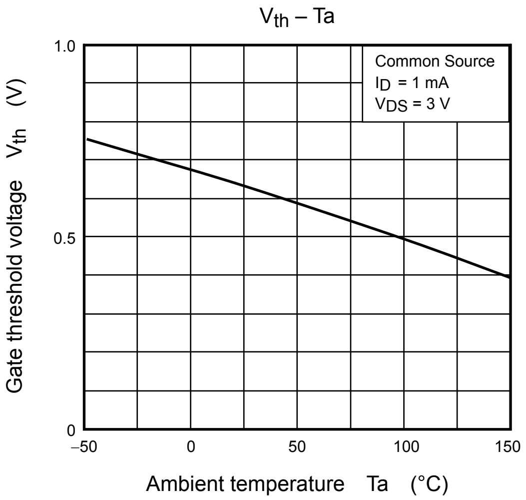


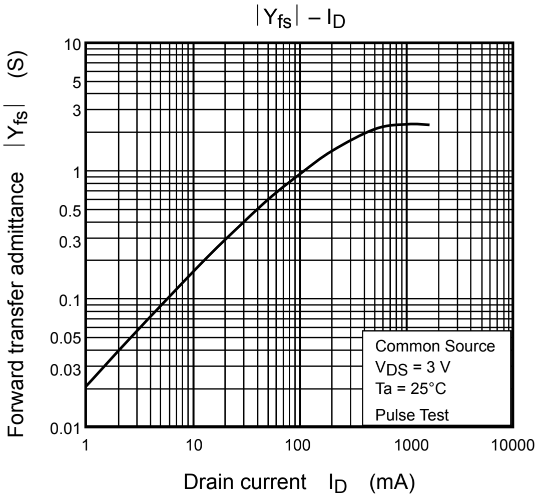


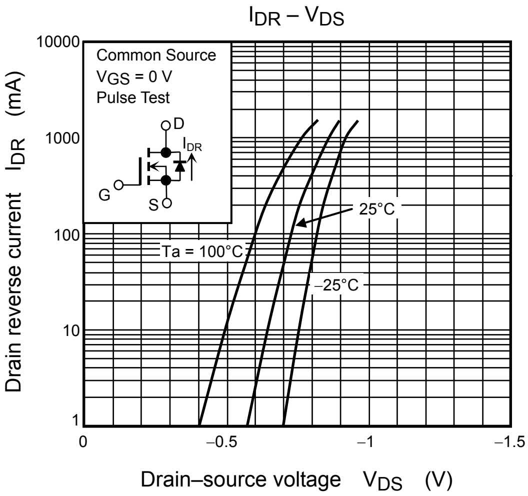


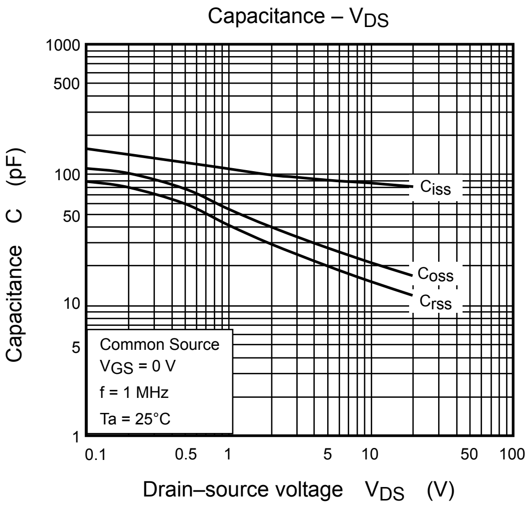


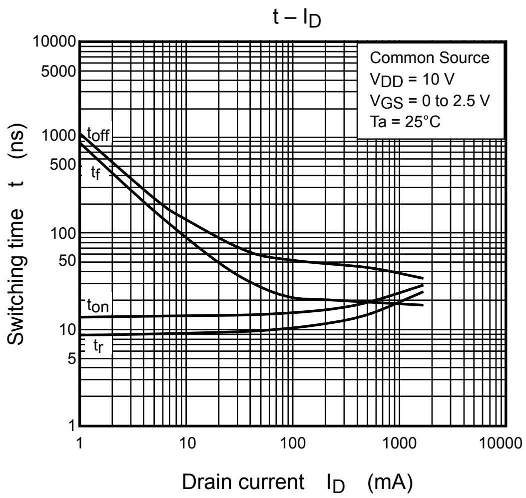
Q1 (N-ch MOSFET)

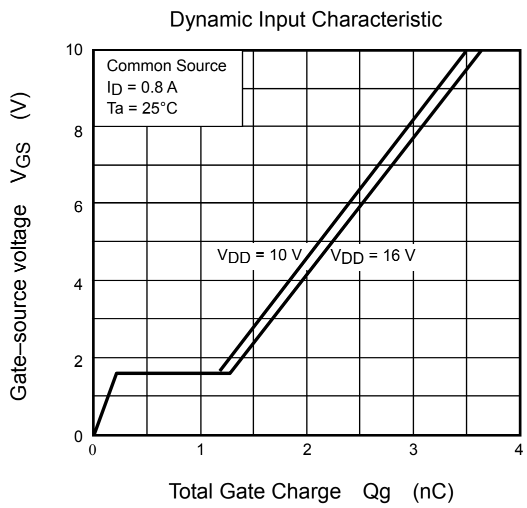




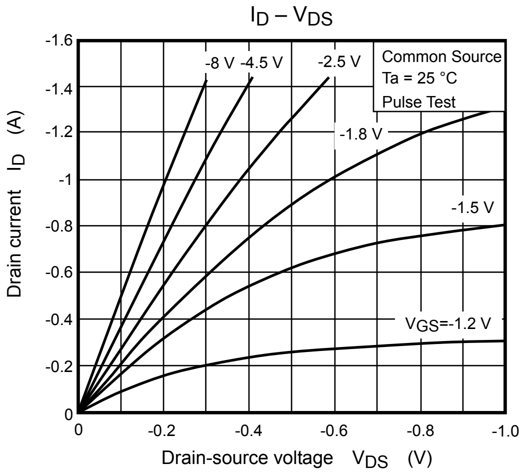


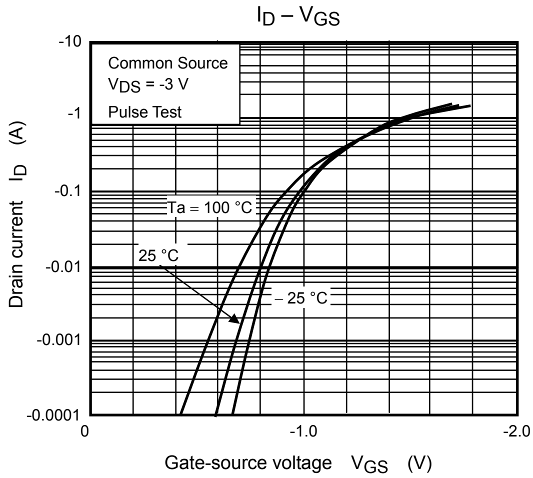


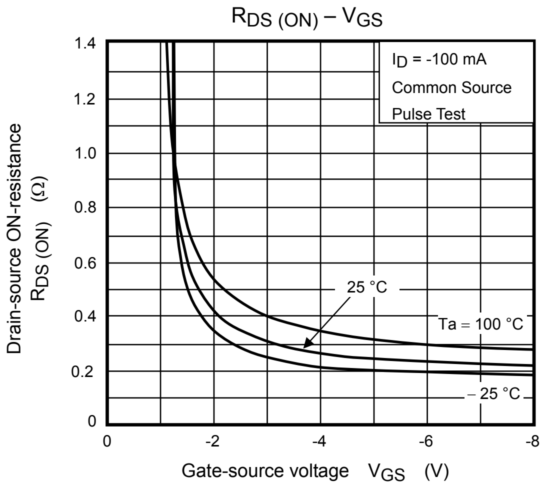


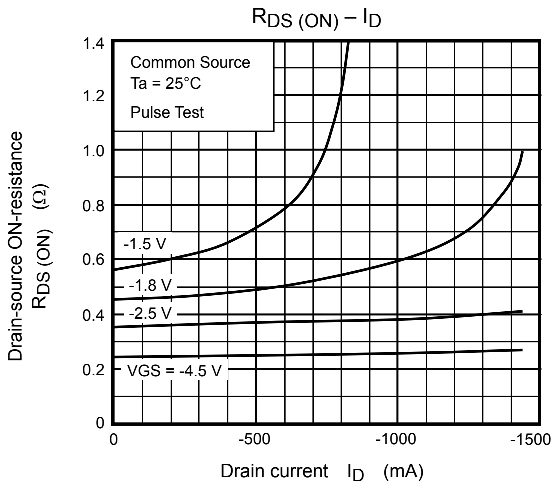


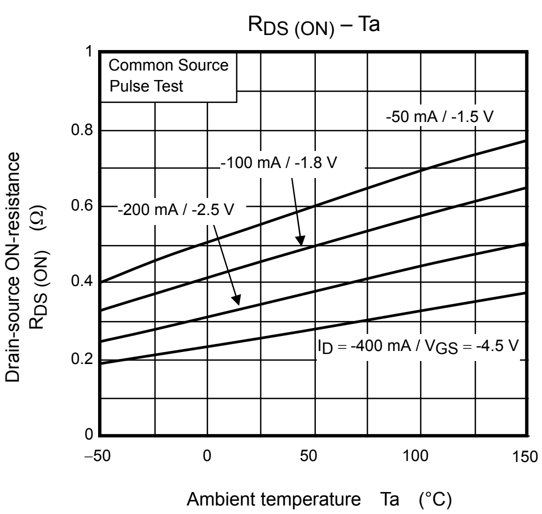
Q2 (P-ch MOSFET)

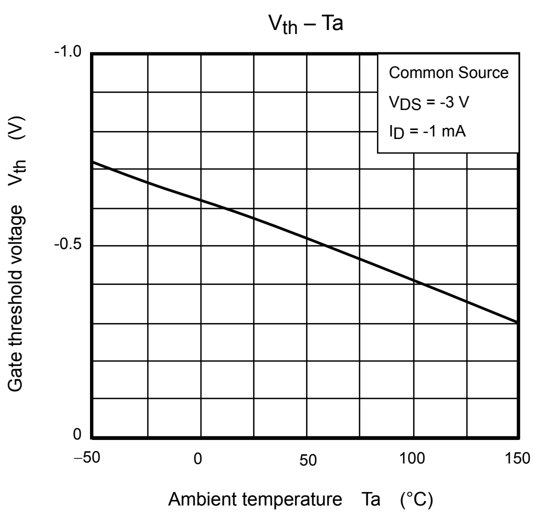




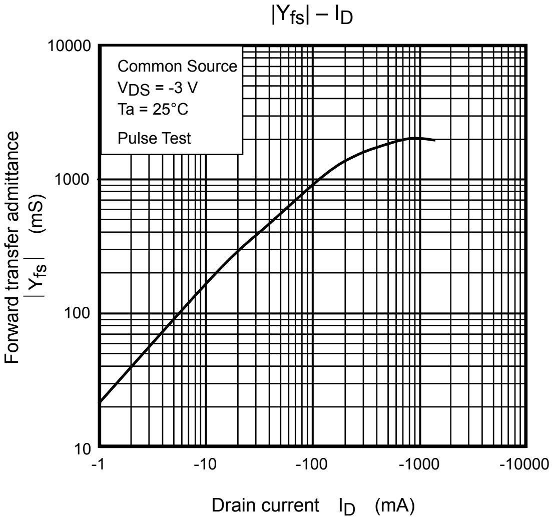


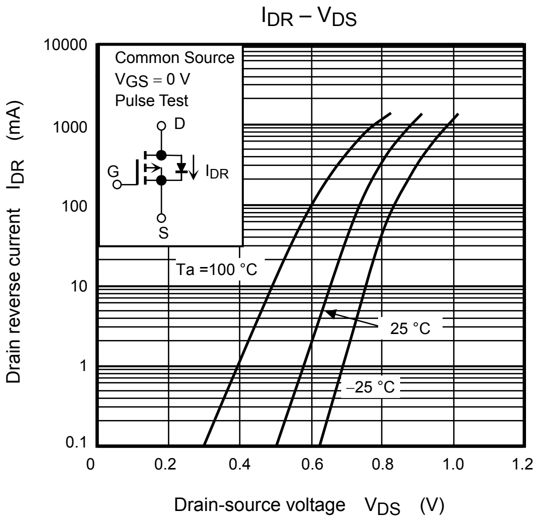


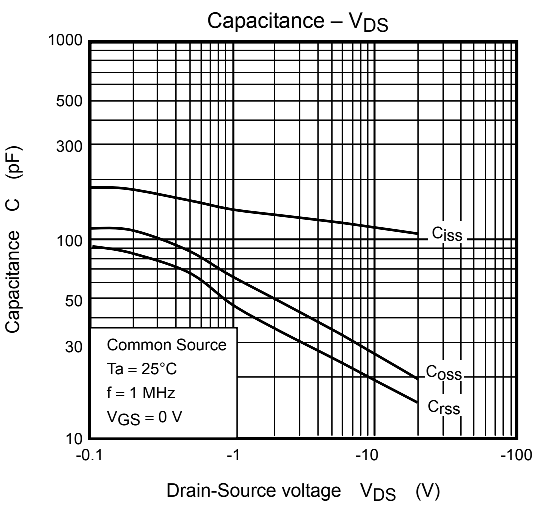


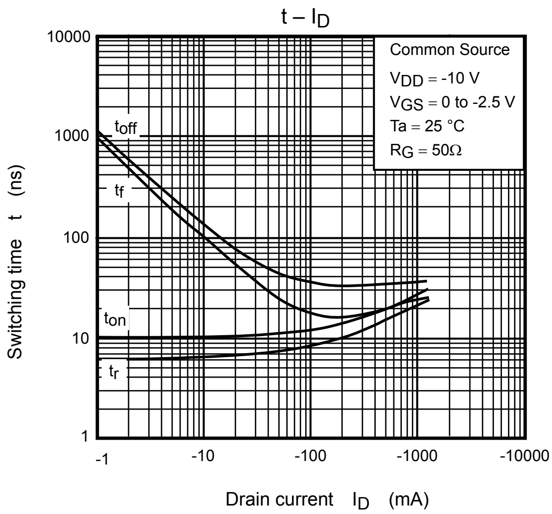


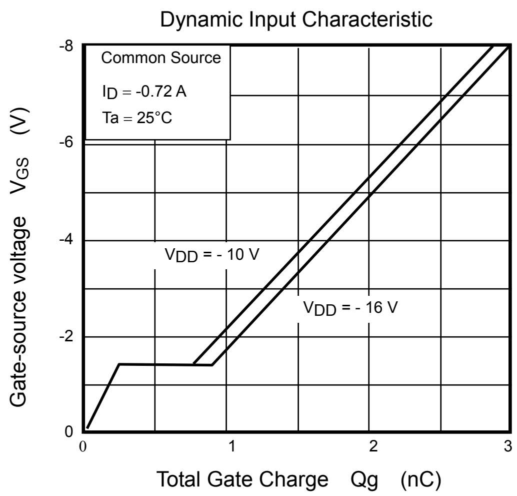
Q2 (P-ch MOSFET)



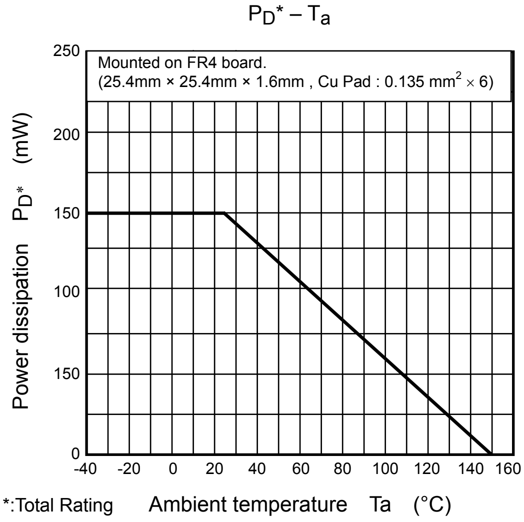








Q1, Q2 Common



*:Total Rating

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