

N-channel 100 V, 0.0062 Ω typ., 19 A, STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

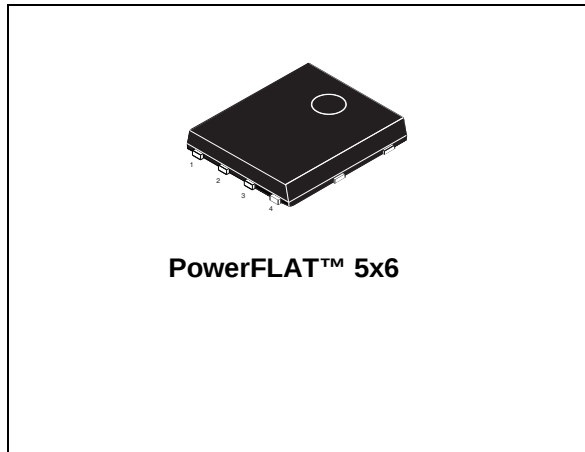
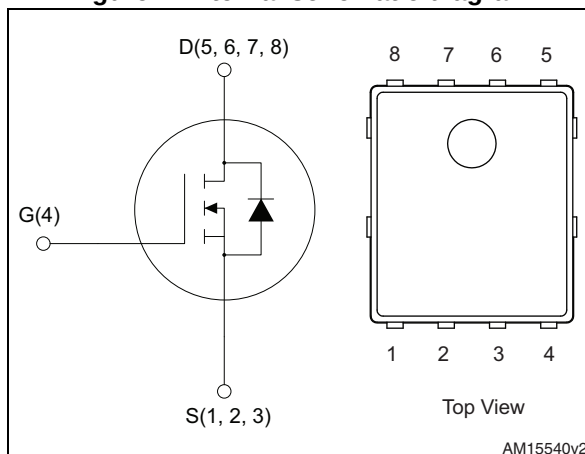


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max	I _D	P _{TOT}
STL100N10F7	100 V	0.0073 Ω	19 A	5 W

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 7th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL100N10F7	100N10F7	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	70	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	19	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	13	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	76	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	5	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. This value is rated according to R_{thj-c} .
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.56	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
E_{AS}	Single pulse avalanche energy ($T_J = 25\text{ }^\circ\text{C}$, $L = 3.5\text{ mH}$, $I_{AS} = 15\text{ A}$, $V_{DD} = 50\text{ V}$, $V_{GS} = 10\text{ V}$)	400	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 250 μA	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 100 V V _{DS} = 100 V; T _C =125 °C			1 100	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = +20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 19 A		0.0062	0.0073	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	4369	5680	pF
C _{oss}	Output capacitance		-	823	1070	pF
C _{rss}	Reverse transfer capacitance		-	36	47	pF
Q _g	Total gate charge	V _{DD} = 50 V, I _D = 19 A V _{GS} = 10 V Figure 14	-	61	80	nC
Q _{gs}	Gate-source charge		-	26		nC
Q _{gd}	Gate-drain charge		-	13		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 19 A, R _G = 4.7 Ω, V _{GS} = 10 V Figure 13	-	27	-	ns
t _r	Rise time		-	40	-	ns
t _{d(off)}	Turn-off delay time		-	46	-	ns
t _f	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		19	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		76	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 38\text{ A}$, $V_{GS}=0$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 19\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=80\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	77		ns
Q_{rr}	Reverse recovery charge		-	146		nC
I_{RRM}	Reverse recovery current		-	4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

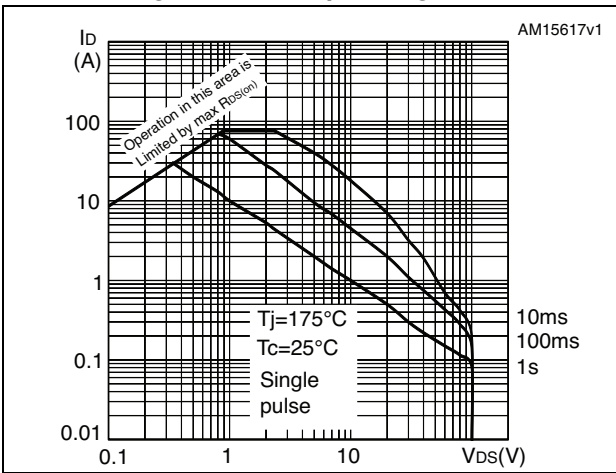


Figure 3. Thermal impedance

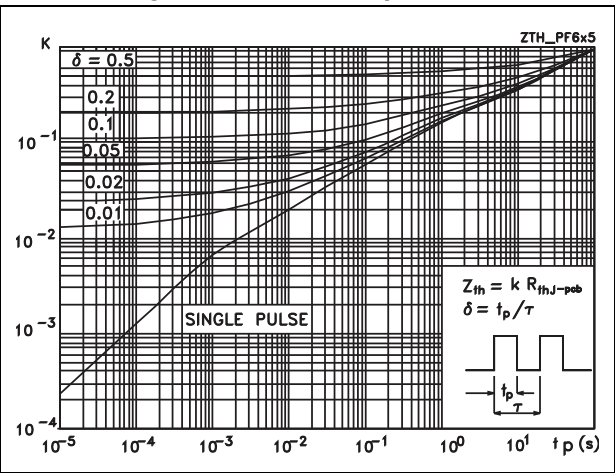


Figure 4. Output characteristics

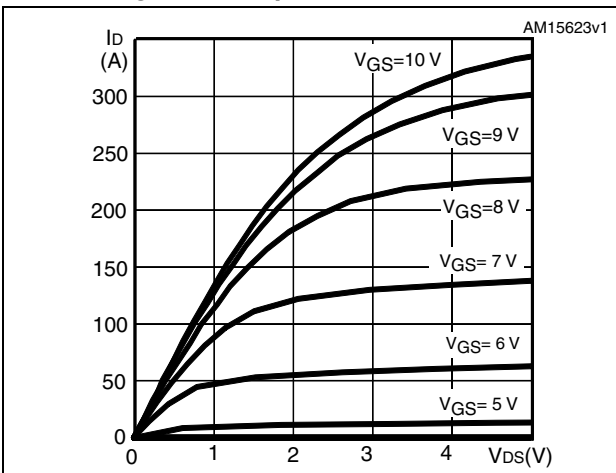


Figure 5. Transfer characteristics

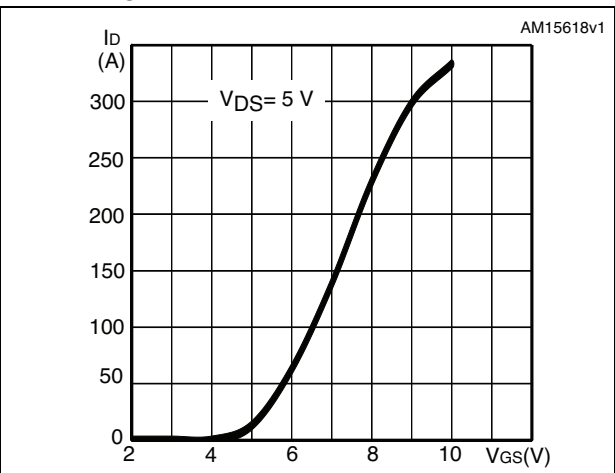


Figure 6. Gate charge vs gate-source voltage

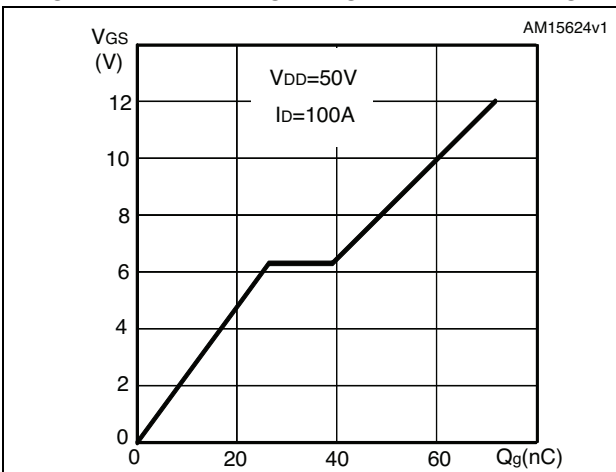


Figure 7. Static drain-source on-resistance

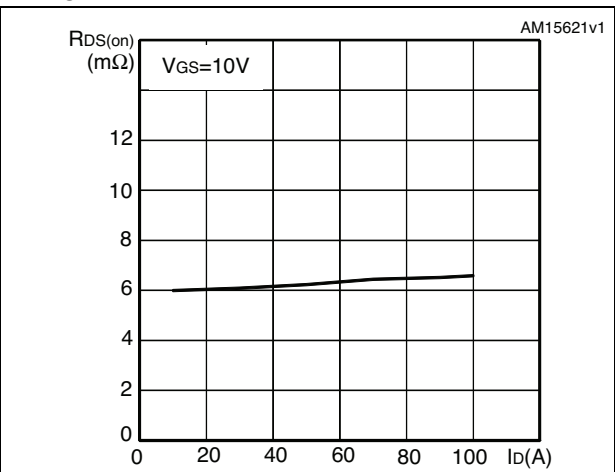


Figure 8. Capacitance variations

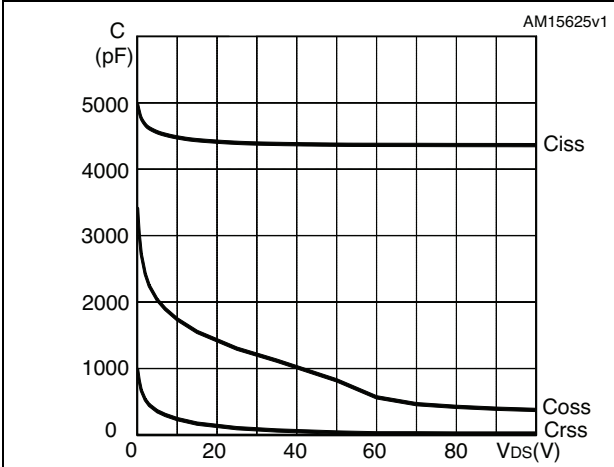


Figure 9. Normalized B_{VDS} vs temperature

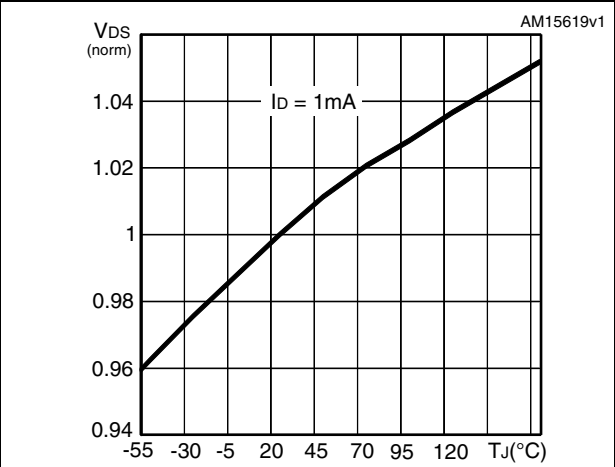


Figure 10. Normalized gate threshold voltage vs temperature

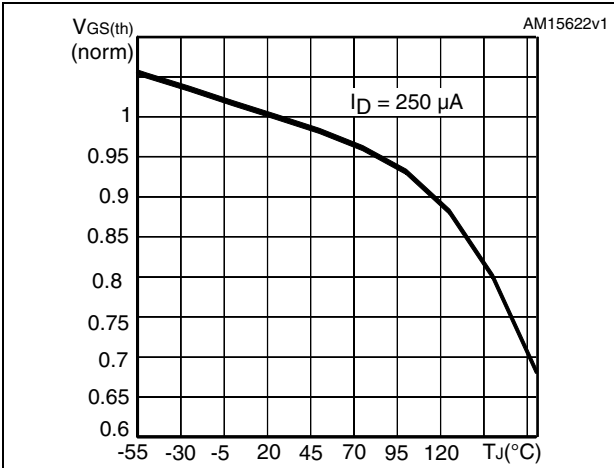


Figure 11. Normalized on-resistance vs temperature

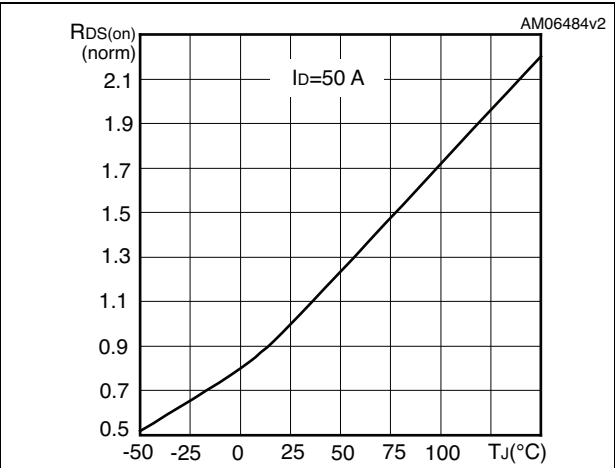
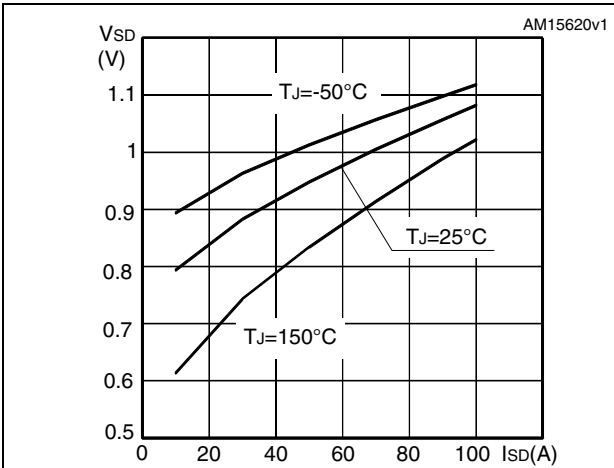


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

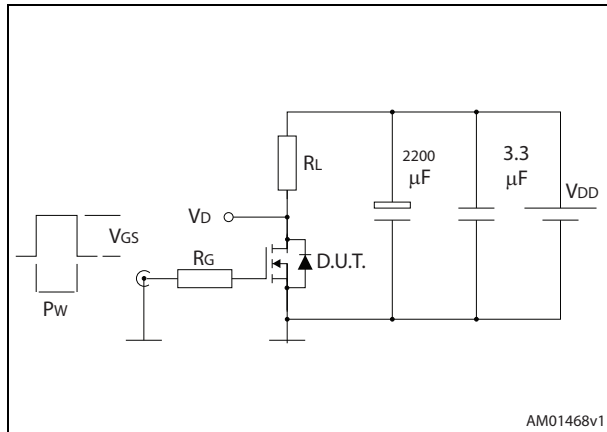


Figure 14. Gate charge test circuit

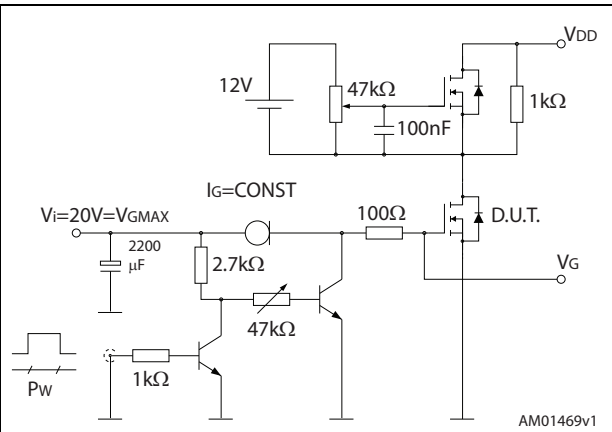


Figure 15. Test circuit for inductive load switching and diode recovery times

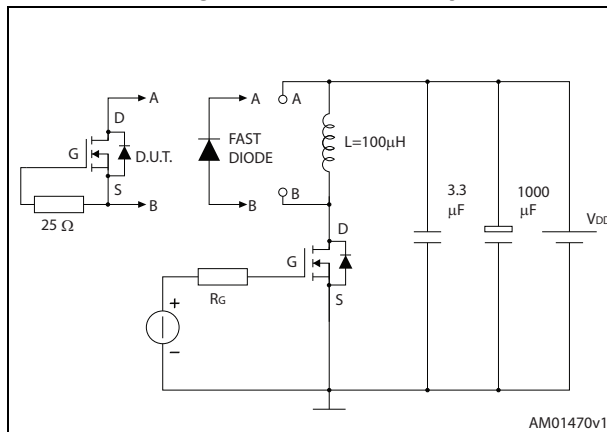


Figure 16. Unclamped inductive load test circuit

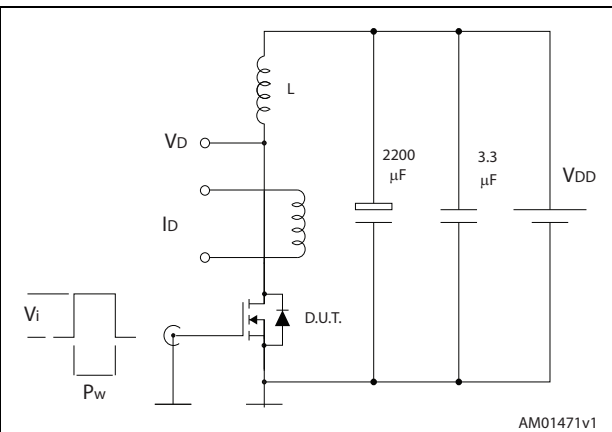


Figure 17. Unclamped inductive waveform

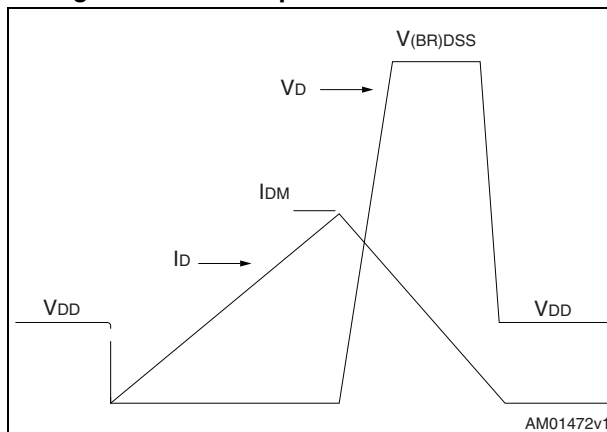
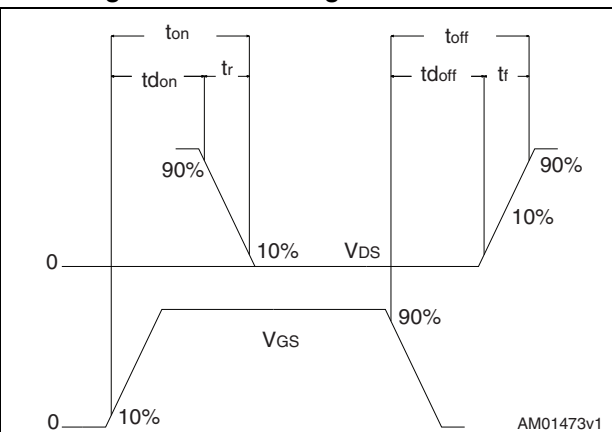


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 19. PowerFLAT 5x6 type S-R drawing

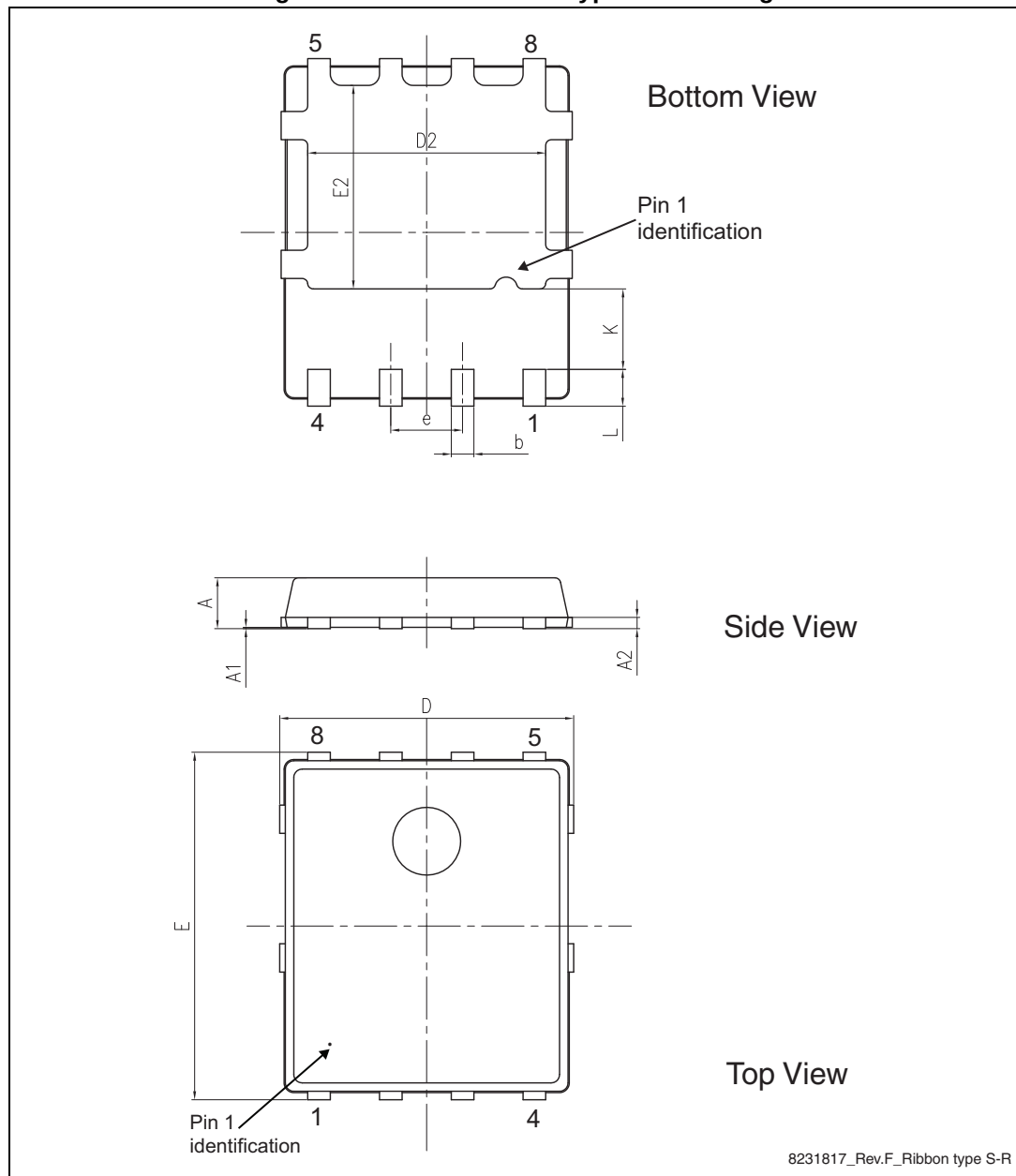
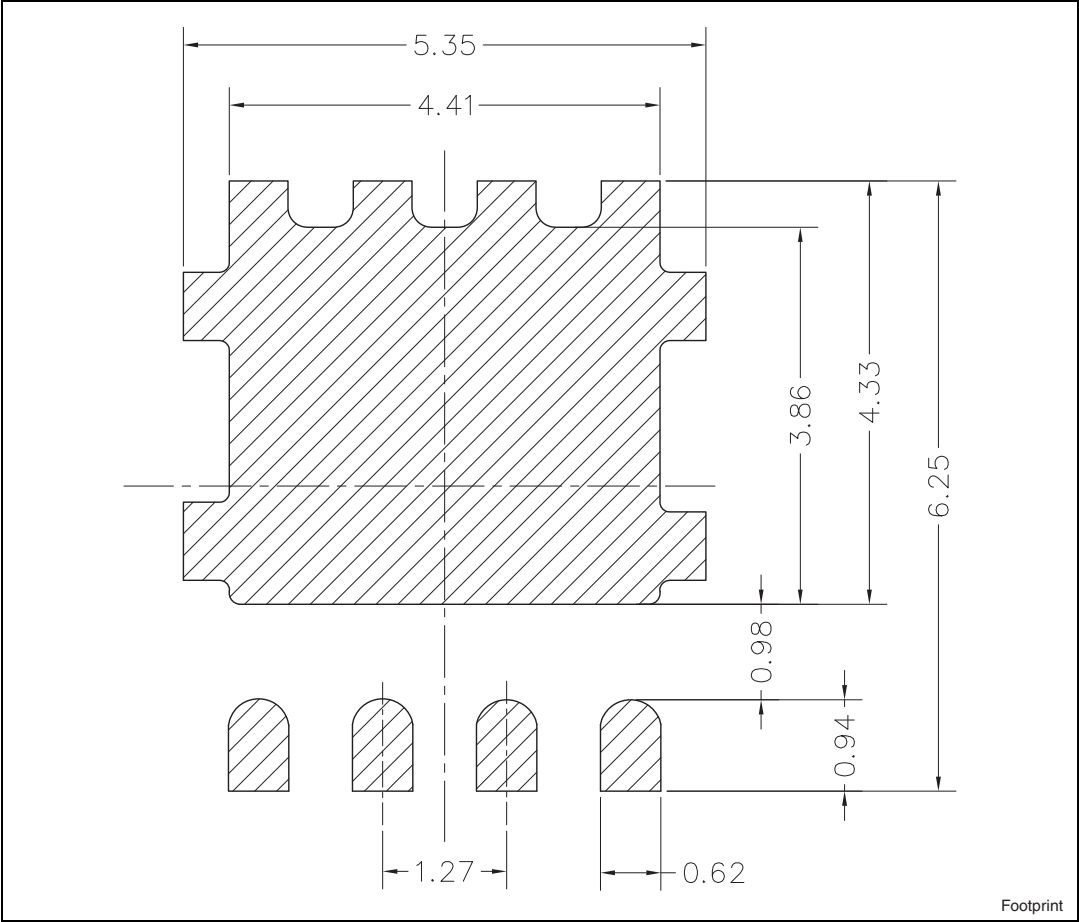


Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(a)

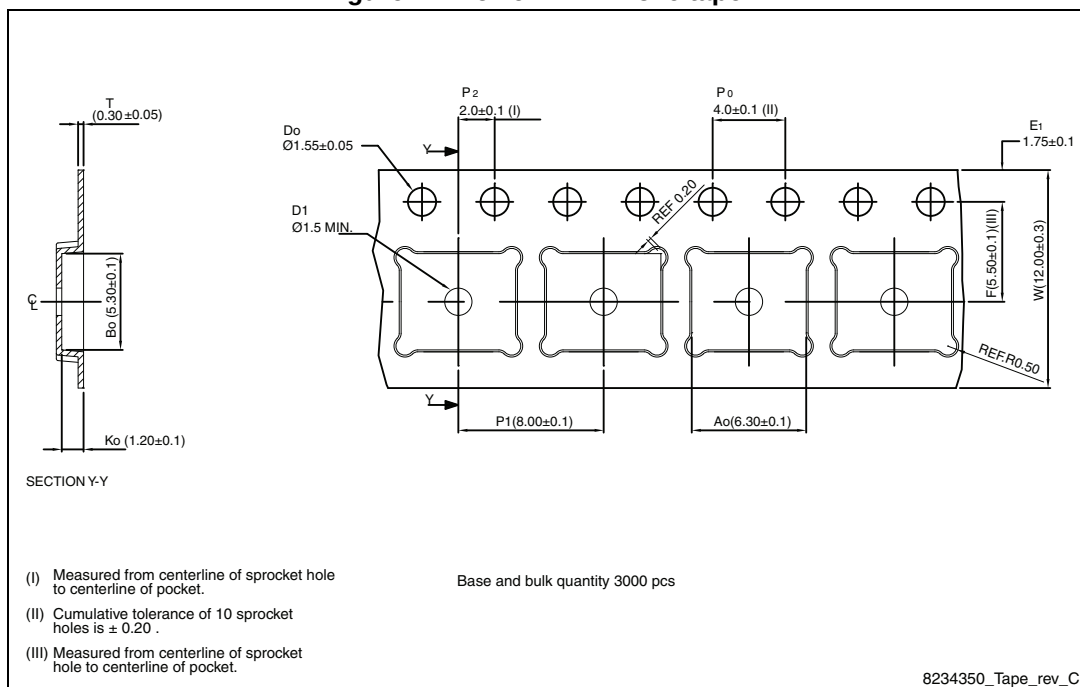
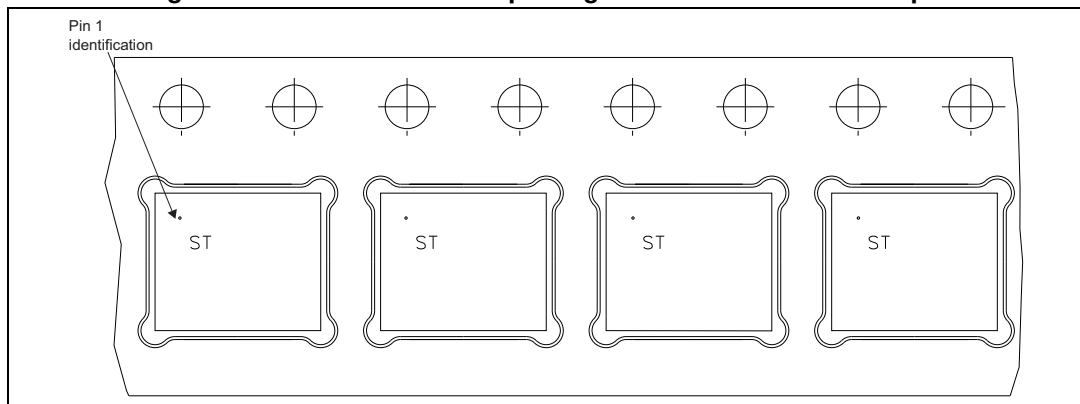
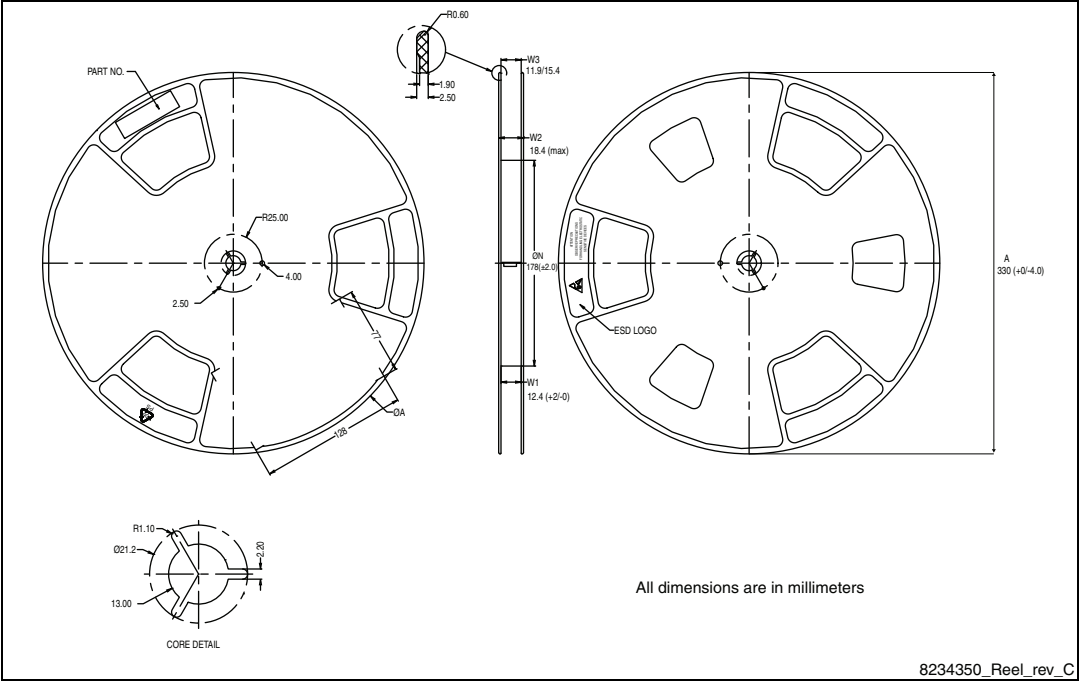


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Oct-2012	1	First release.
19-Feb-2013	2	– Document status changed from preliminary to production data – Inserted: Section 2.1: Electrical characteristics (curves) – Updated: Section 4: Package mechanical data – Added: Section 5: Packaging mechanical data – Minor text changes
21-Feb-2013	3	– Updated Table 8: Source drain diode and Figure 5: Transfer characteristics.
31-Jul-2013	4	– Updated I_D values in test conditions respectively in Table 6: Dynamic and Table 7: Switching times. – Modified: Figure 13, 14, 15 and 16 – Minor text changes

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