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REVISION HISTORY

5/11—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 8\ \Omega + 33\ \mu\text{H}$ , unless otherwise noted.

Table 1.

| Parameter                            | Symbol              | Test Conditions/Comments   | Min  | Typ   | Max                 | Unit  |
|--------------------------------------|---------------------|--|------|---|---------------------|---|
| DEVICE CHARACTERISTICS               |                     |  |      |   |                     |   |
| Output Power                         | P <sub>OUT</sub>    | f = 1 kHz, 20 kHz BW<br>R <sub>L</sub> = 8 Ω, THD = 1%, V <sub>DD</sub> = 5.0 V<br>R <sub>L</sub> = 8 Ω, THD = 1%, V <sub>DD</sub> = 3.6 V<br>R <sub>L</sub> = 8 Ω, THD = 1%, V <sub>DD</sub> = 2.5 V<br>R <sub>L</sub> = 8 Ω, THD = 10%, V <sub>DD</sub> = 5.0 V<br>R <sub>L</sub> = 8 Ω, THD = 10%, V <sub>DD</sub> = 3.6 V<br>R <sub>L</sub> = 8 Ω, THD = 10%, V <sub>DD</sub> = 2.5 V<br>R <sub>L</sub> = 4 Ω, THD = 1%, V <sub>DD</sub> = 5.0 V<br>R <sub>L</sub> = 4 Ω, THD = 1%, V <sub>DD</sub> = 3.6 V<br>R <sub>L</sub> = 4 Ω, THD = 1%, V <sub>DD</sub> = 2.5 V<br>R <sub>L</sub> = 4 Ω, THD = 10%, V <sub>DD</sub> = 5.0 V<br>R <sub>L</sub> = 4 Ω, THD = 10%, V <sub>DD</sub> = 3.6 V<br>R <sub>L</sub> = 4 Ω, THD = 10%, V <sub>DD</sub> = 2.5 V |      | 1.41<br>0.72<br>0.33<br>1.78<br>0.90<br>0.41<br>2.49<br>1.25<br>0.54<br>3.17 <sup>1</sup><br>1.56<br>0.68 |                     | W<br>W<br>W<br>W<br>W<br>W<br>W<br>W<br>W<br>W<br>W<br>W<br>W |
| Efficiency                           | η                   | P <sub>OUT</sub> = 1.4 W into 8 Ω, V <sub>DD</sub> = 5.0 V   |      | 92.4  |                     | %   |
| Total Harmonic Distortion Plus Noise | THD + N             | P <sub>OUT</sub> = 1 W into 8 Ω, f = 1 kHz, V <sub>DD</sub> = 5.0 V  |      | 0.007   |                     | %   |
|                                      |                     | P <sub>OUT</sub> = 0.5 W into 8 Ω, f = 1 kHz, V <sub>DD</sub> = 3.6 V  |      | 0.009   |                     | %   |
| Input Common-Mode Voltage Range      | V <sub>CM</sub>     |  | 1.0  |   | V <sub>DD</sub> – 1 | V   |
| Common-Mode Rejection Ratio          | CMRR                | 100 mV rms at 1 kHz  |      | 51  |                     | dB  |
| Average Switching Frequency          | f <sub>SW</sub>     |  |      | 256   |                     | kHz   |
| Clock Frequency                      | f <sub>OSC</sub>    |  |      | 6.2   |                     | MHz   |
| Differential Output Offset Voltage   | V <sub>OOS</sub>    | Gain = 6 dB  |      | 0.4   | 5.0                 | mV  |
| POWER SUPPLY                         |                     |  |      |   |                     |   |
| Supply Voltage Range                 | V <sub>DD</sub>     | Guaranteed from PSRR test  | 2.5  |   | 5.5                 | V   |
| Power Supply Rejection Ratio         | PSRR <sub>GSM</sub> | Inputs are ac-grounded, C <sub>IN</sub> = 0.1 μF, gain = 6 dB<br>V <sub>RIIPPLE</sub> = 100 mV at 217 Hz   |      | 80  |                     | dB  |
|                                      | PSRR                | V <sub>RIIPPLE</sub> = 100 mV at 1 kHz   |      | 80  |                     | dB  |
| Supply Current                       | I <sub>SY</sub>     | V <sub>IN</sub> = 0 V, no load, V <sub>DD</sub> = 5.0 V<br>V <sub>IN</sub> = 0 V, no load, V <sub>DD</sub> = 3.6 V<br>V <sub>IN</sub> = 0 V, no load, V <sub>DD</sub> = 2.5 V<br>V <sub>IN</sub> = 0 V, R <sub>L</sub> = 8 Ω + 33 μH, V <sub>DD</sub> = 5.0 V<br>V <sub>IN</sub> = 0 V, R <sub>L</sub> = 8 Ω + 33 μH, V <sub>DD</sub> = 3.6 V<br>V <sub>IN</sub> = 0 V, R <sub>L</sub> = 8 Ω + 33 μH, V <sub>DD</sub> = 2.5 V  |      | 2.5<br>2.0<br>1.9<br>2.5<br>2.0<br>1.8  |                     | mA<br>mA<br>mA<br>mA<br>mA<br>mA                              |
| Shutdown Current                     | I <sub>SD</sub>     | $\overline{SD}$ = GND  |      | 100   |                     | nA  |
| GAIN CONTROL                         |                     |  |      |   |                     |   |
| Closed-Loop Gain                     | Gain                | GAIN = GND<br>GAIN = VDD   |      | 12<br>6   |                     | dB<br>dB  |
| Input Impedance                      | Z <sub>IN</sub>     | $\overline{SD}$ = VDD, gain = 6 dB or 12 dB  |      | 80  |                     | kΩ  |
| SHUTDOWN CONTROL                     |                     |  |      |   |                     |   |
| Input Voltage High                   | V <sub>IH</sub>     |  | 1.35 |   |                     | V   |
| Input Voltage Low                    | V <sub>IL</sub>     |  |      |   | 0.35                | V   |
| Turn-On Time                         | t <sub>WU</sub>     | $\overline{SD}$ rising edge from GND to VDD  |      | 12.5  |                     | ms  |
| Turn-Off Time                        | t <sub>SD</sub>     | $\overline{SD}$ falling edge from VDD to GND   |      | 5   |                     | μs  |
| Output Impedance                     | Z <sub>OUT</sub>    | $\overline{SD}$ = GND  | 100  |   |                     | kΩ  |

# SSM2377

| Parameter             | Symbol | Test Conditions/Comments  | Min | Typ      | Max | Unit                           |
|-----------------------|--------|---|-----|----------|-----|--------------------------------|
| NOISE PERFORMANCE     |        |   |     |          |     |                                |
| Output Voltage Noise  | $e_n$  | f = 20 Hz to 20 kHz, inputs are ac-grounded,<br>gain = 6 dB, A-weighted<br>$V_{DD} = 5.0\text{ V}$<br>$V_{DD} = 3.6\text{ V}$ |     | 30<br>30 |     | $\mu\text{V}$<br>$\mu\text{V}$ |
| Signal-to-Noise Ratio | SNR    | $P_{OUT} = 1.4\text{ W}$ , $R_L = 8\ \Omega$ , A-weighted   |     | 101      |     | dB                             |

<sup>1</sup> Although the SSM2377 has good audio quality above 3 W, continuous output power beyond 3 W must be avoided due to device packaging limitations.

## ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

| Parameter                            | Rating          |
|--------------------------------------|-----------------|
| Supply Voltage                       | 6 V             |
| Input Voltage                        | $V_{DD}$        |
| Common-Mode Input Voltage            | $V_{DD}$        |
| Storage Temperature Range            | –65°C to +150°C |
| Operating Temperature Range          | –40°C to +85°C  |
| Junction Temperature Range           | –65°C to +165°C |
| Lead Temperature (Soldering, 60 sec) | 300°C           |
| ESD Susceptibility                   | 4 kV            |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

Junction-to-air thermal resistance ( $\theta_{JA}$ ) is specified for the worst-case conditions, that is, a device soldered in a printed circuit board (PCB) for surface-mount packages.  $\theta_{JA}$  is determined according to JEDEC JESD51-9 on a 4-layer PCB with natural convection cooling.

Table 3. Thermal Resistance

| Package Type                  | PCB  | $\theta_{JA}$ | Unit |
|-------------------------------|------|---------------|------|
| 9-Ball, 1.2 mm × 1.2 mm WLCSP | 2S2P | 88            | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

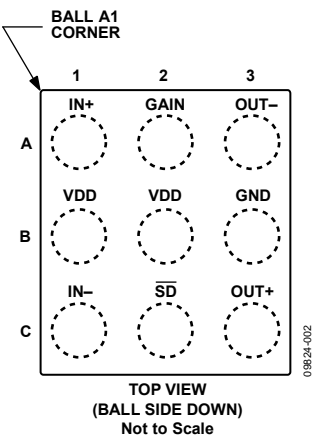
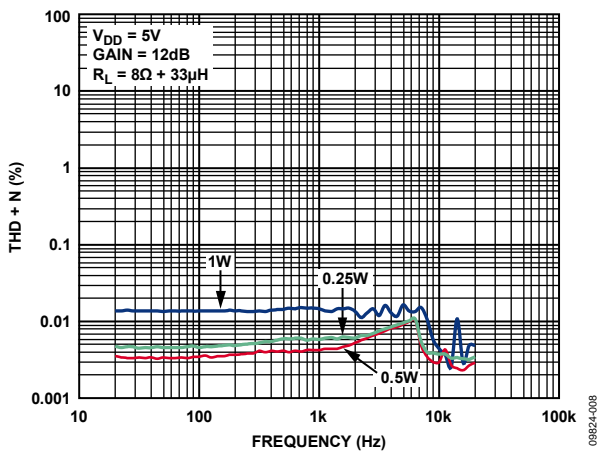
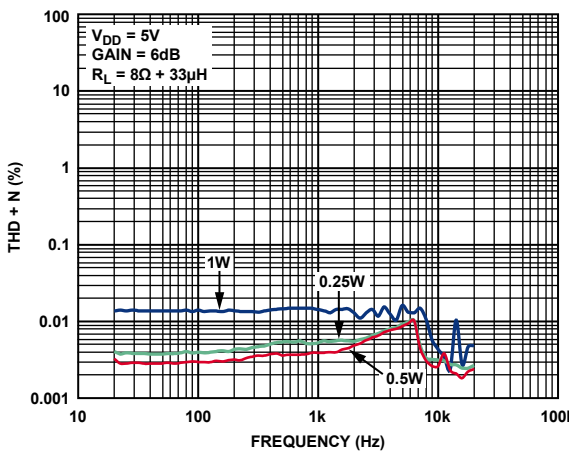
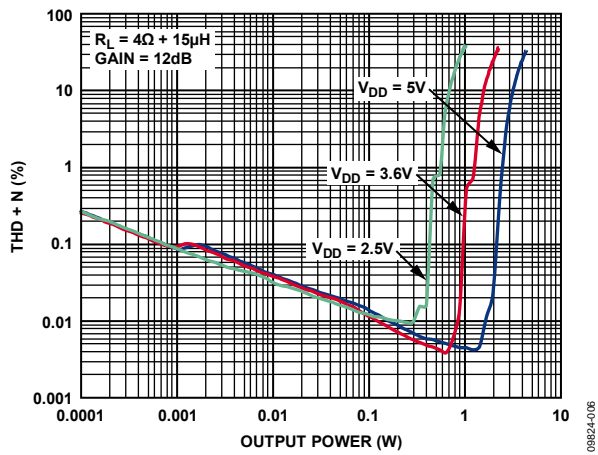
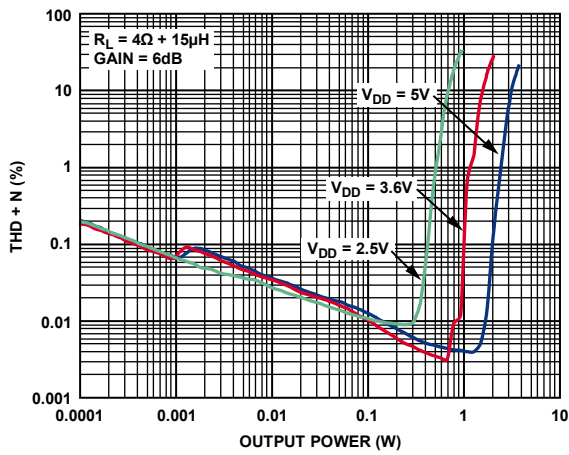
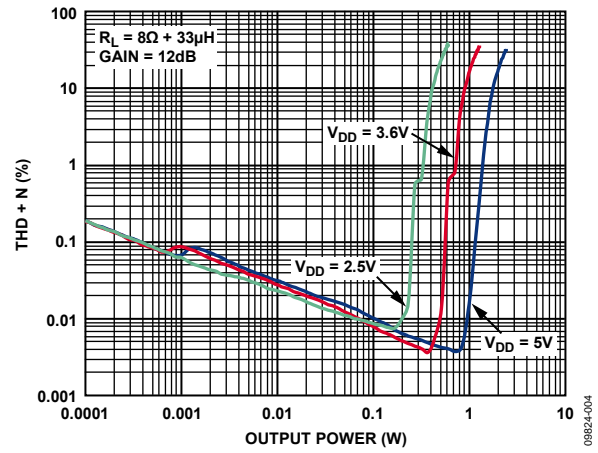
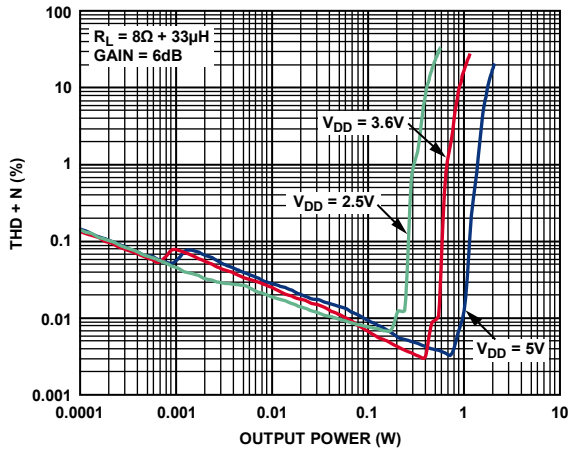


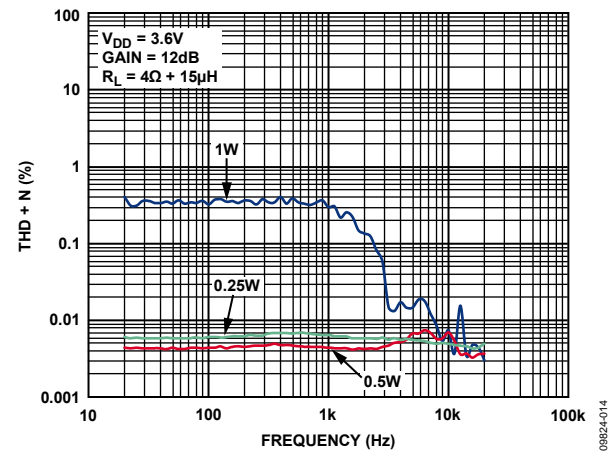
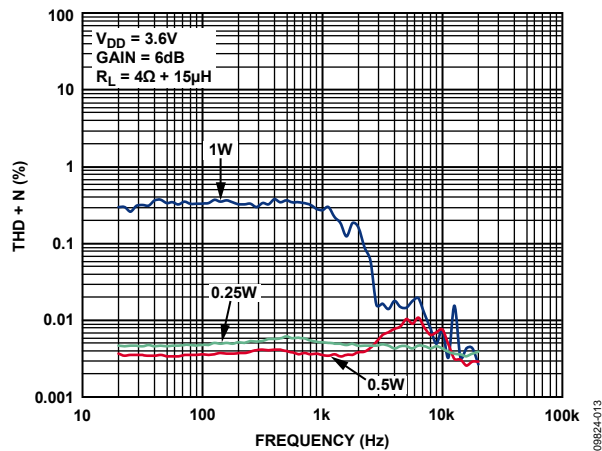
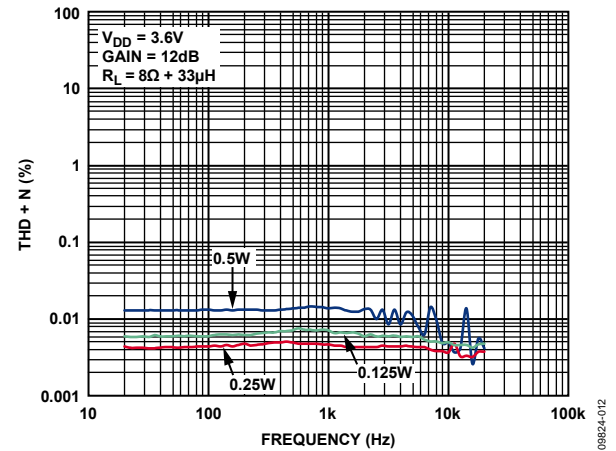
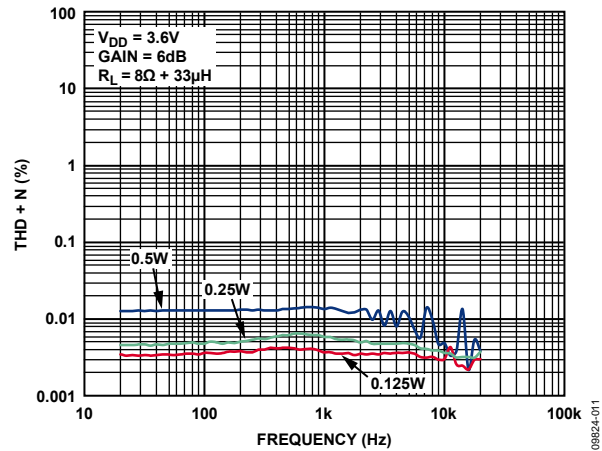
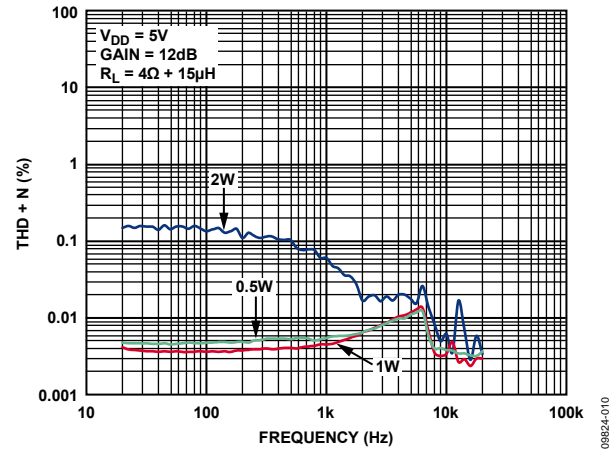
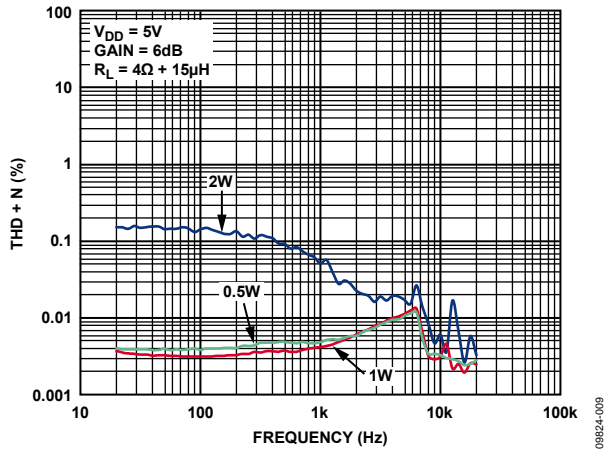
Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic        | Description                               |
|---------|-----------------|---|
| A1      | IN+             | Noninverting Input.                       |
| B1      | VDD             | Power Supply.                             |
| C1      | IN-             | Inverting Input.                          |
| A2      | GAIN            | Gain Selection Pin.                       |
| B2      | VDD             | Power Supply.                             |
| C2      | $\overline{SD}$ | Shutdown Input. Active low digital input. |
| A3      | OUT-            | Inverting Output.                         |
| B3      | GND             | Ground.                                   |
| C3      | OUT+            | Noninverting Output.                      |

## TYPICAL PERFORMANCE CHARACTERISTICS







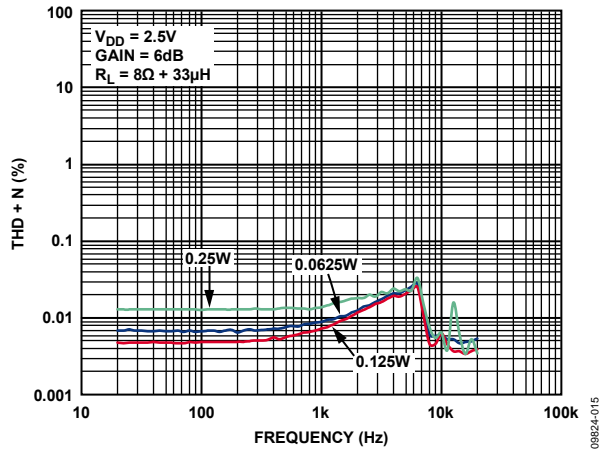


Figure 15. THD + N vs. Frequency,  $V_{DD} = 2.5\text{ V}$ ,  $R_L = 8\ \Omega$ , Gain = 6 dB

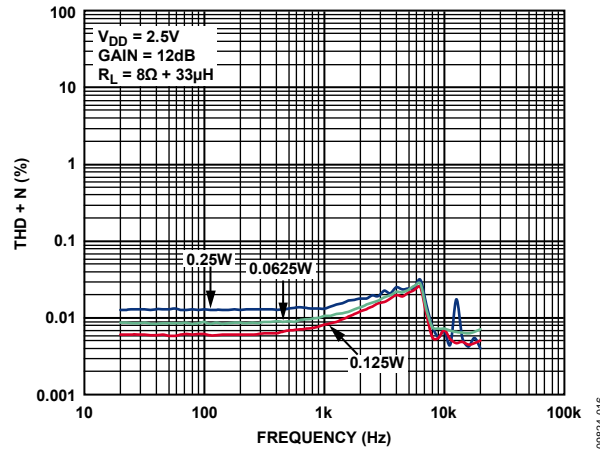


Figure 18. THD + N vs. Frequency,  $V_{DD} = 2.5\text{ V}$ ,  $R_L = 8\ \Omega$ , Gain = 12 dB

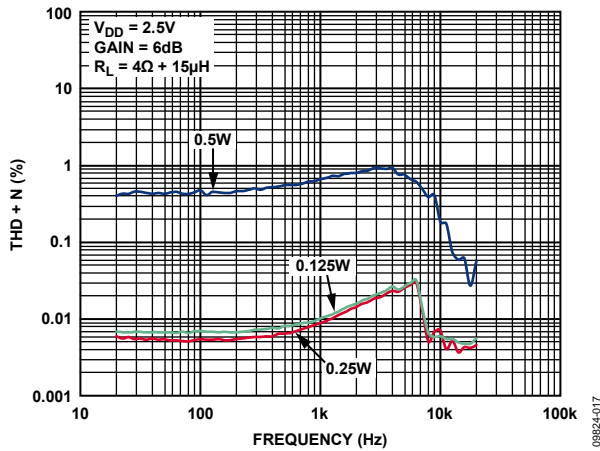


Figure 16. THD + N vs. Frequency,  $V_{DD} = 2.5\text{ V}$ ,  $R_L = 4\ \Omega$ , Gain = 6 dB

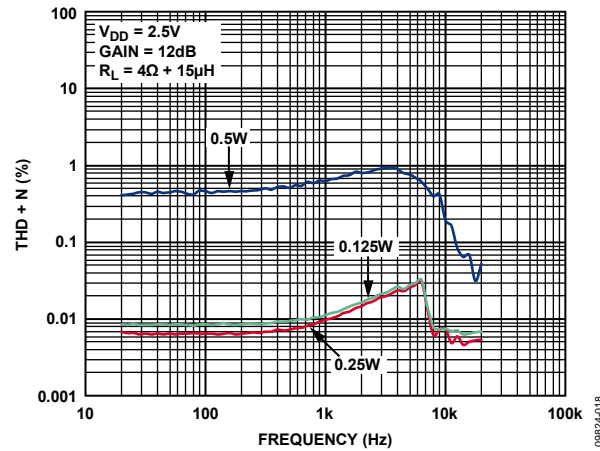


Figure 19. THD + N vs. Frequency,  $V_{DD} = 2.5\text{ V}$ ,  $R_L = 4\ \Omega$ , Gain = 12 dB

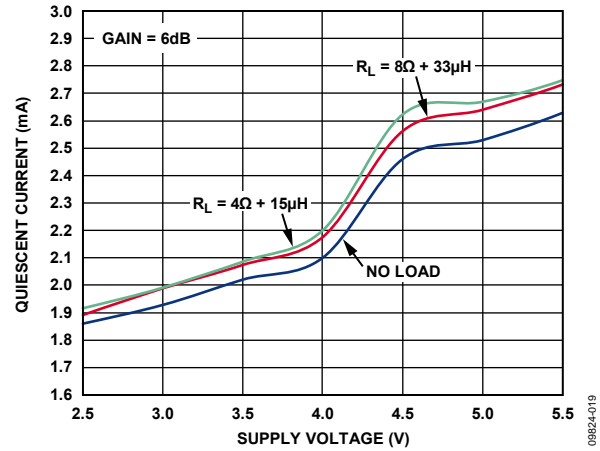


Figure 17. Quiescent Current vs. Supply Voltage, Gain = 6 dB

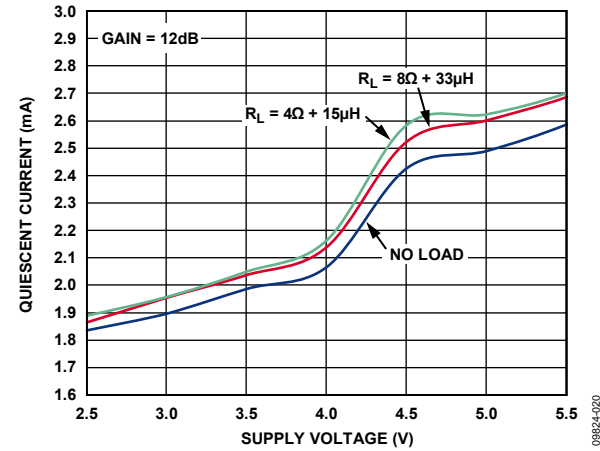


Figure 20. Quiescent Current vs. Supply Voltage, Gain = 12 dB

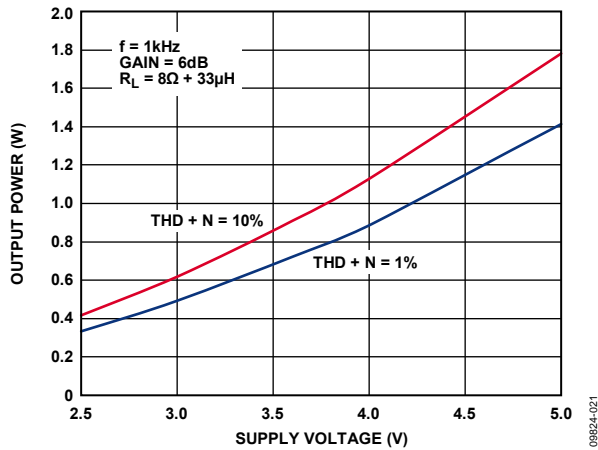


Figure 21. Maximum Output Power vs. Supply Voltage,  $R_L = 8\ \Omega$ , Gain = 6 dB

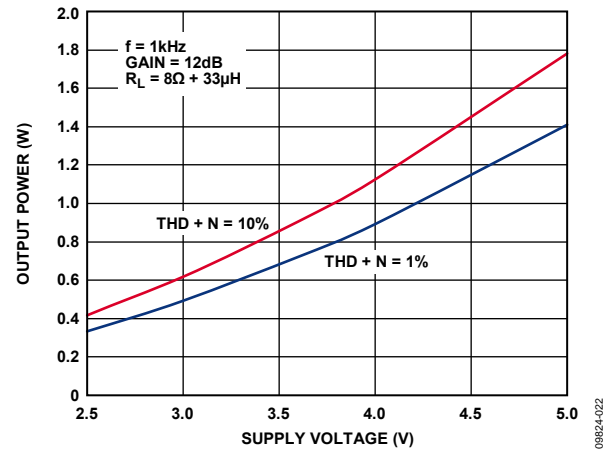


Figure 24. Maximum Output Power vs. Supply Voltage,  $R_L = 8\ \Omega$ , Gain = 12 dB

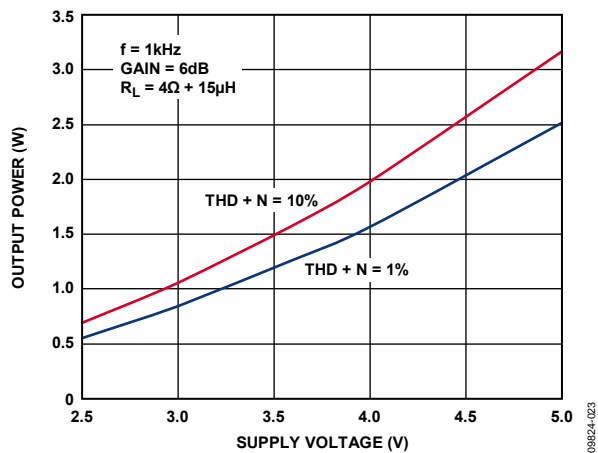


Figure 22. Maximum Output Power vs. Supply Voltage,  $R_L = 4\ \Omega$ , Gain = 6 dB

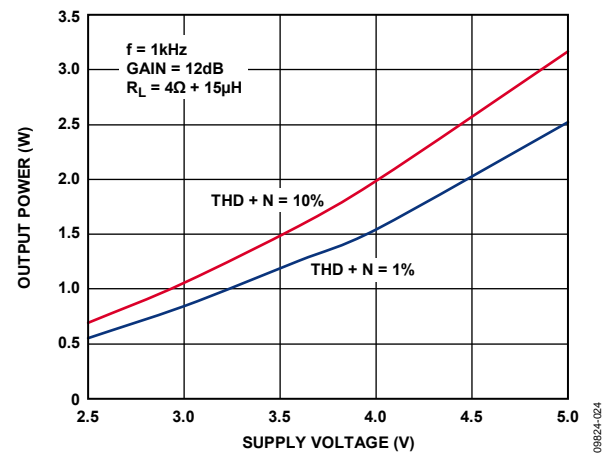


Figure 25. Maximum Output Power vs. Supply Voltage,  $R_L = 4\ \Omega$ , Gain = 12 dB

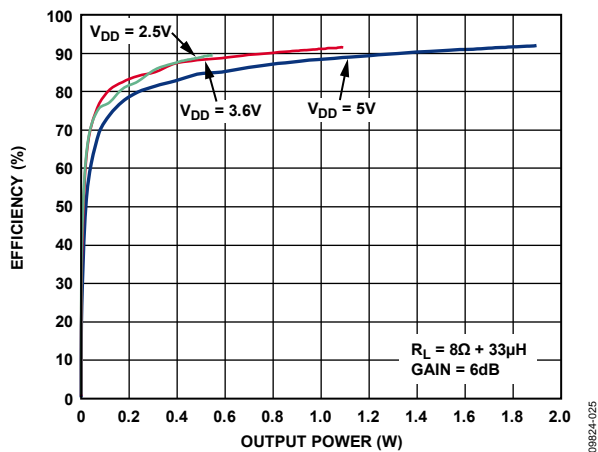


Figure 23. Efficiency vs. Output Power into  $8\ \Omega$ , Gain = 6 dB

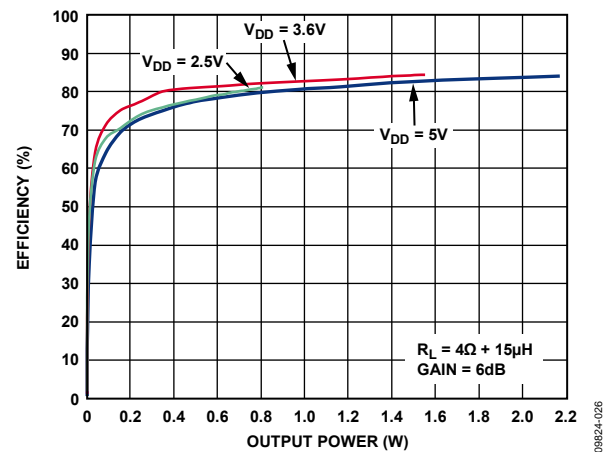


Figure 26. Efficiency vs. Output Power into  $4\ \Omega$ , Gain = 6 dB

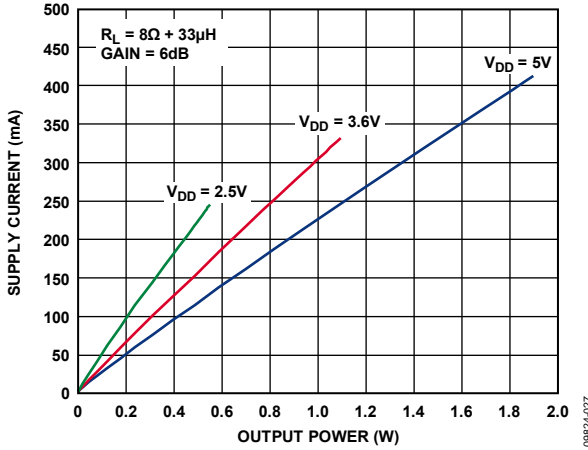


Figure 27. Supply Current vs. Output Power into 8  $\Omega$ , Gain = 6 dB

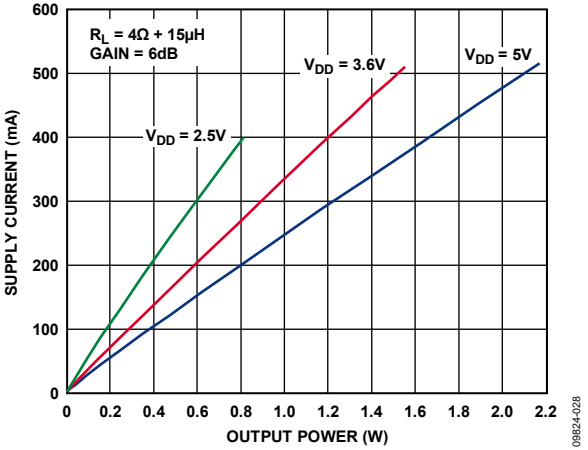


Figure 30. Supply Current vs. Output Power into 4  $\Omega$ , Gain = 6 dB

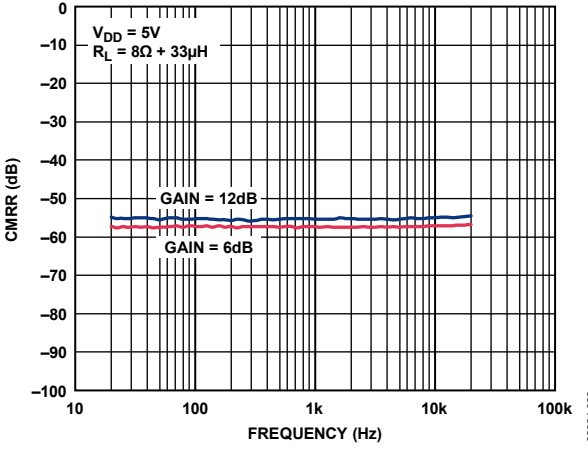


Figure 28. Common-Mode Rejection Ratio (CMRR) vs. Frequency

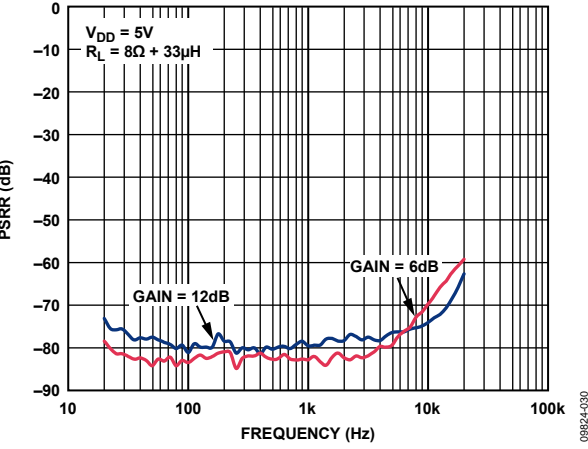


Figure 31. Power Supply Rejection Ratio (PSRR) vs. Frequency

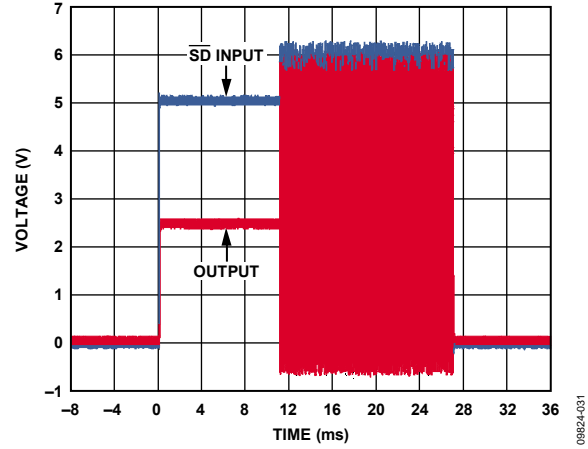


Figure 29. Turn-On Response

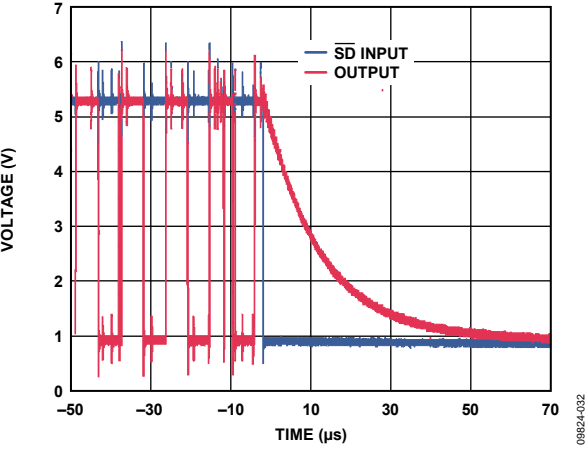


Figure 32. Turn-Off Response

## TYPICAL APPLICATION CIRCUITS

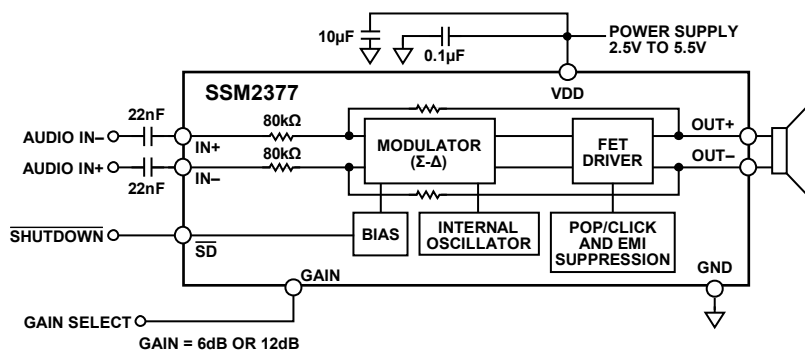


Figure 33. Monaural Differential Input Configuration

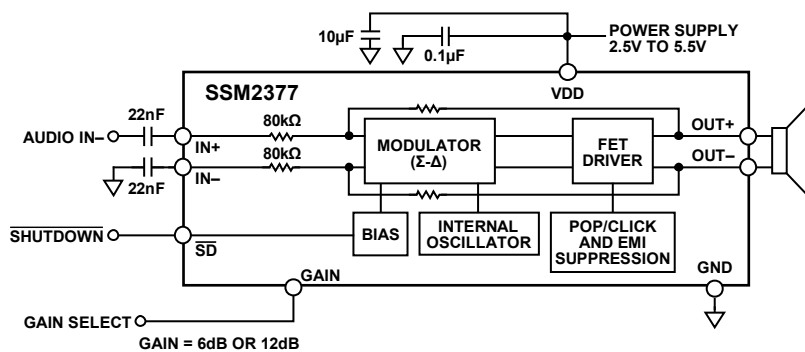


Figure 34. Monaural Single-Ended Input Configuration

## THEORY OF OPERATION

### OVERVIEW

The SSM2377 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing system cost. The SSM2377 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2377 uses  $\Sigma$ - $\Delta$  modulation to determine the switching pattern of the output devices, resulting in a number of important benefits.

- $\Sigma$ - $\Delta$  modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do.
- $\Sigma$ - $\Delta$  modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emissions that might otherwise be radiated by speakers and long cable traces.
- Due to the inherent spread-spectrum nature of  $\Sigma$ - $\Delta$  modulation, the need for oscillator synchronization is eliminated for designs that incorporate multiple SSM2377 amplifiers.

The SSM2377 also integrates overcurrent and overtemperature protection.

### GAIN SELECTION

The preset gain of the SSM2377 can be set to 6 dB or 12 dB using the GAIN pin, as shown in Table 5.

**Table 5. GAIN Pin Function Description**

| Gain Setting (dB) | GAIN Pin Configuration |
|-------------------|------------------------|
| 6                 | Tie to VDD             |
| 12                | Tie to GND             |

### POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audible pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal.

The SSM2377 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation from the  $\overline{\text{SD}}$  control pin.

### EMI NOISE

The SSM2377 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. For applications that have difficulty passing FCC Class B emission tests or experience antenna and RF sensitivity problems, the ultralow EMI architecture of the SSM2377 significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. Figure 35 shows the low radiated emissions from the SSM2377 due to its ultralow EMI architecture.

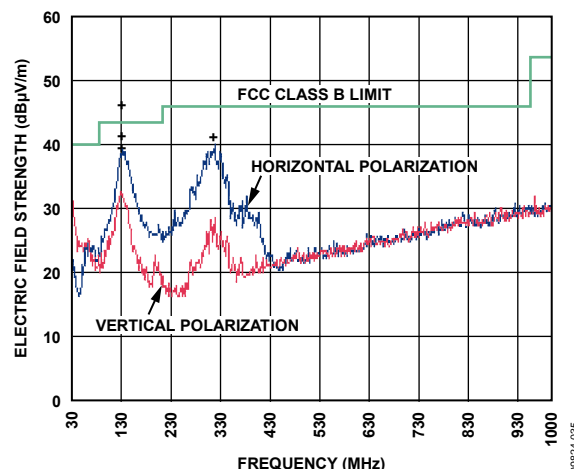


Figure 35. EMI Emissions from the SSM2377

The measurements for Figure 35 were taken in an FCC-certified EMI laboratory with a 1 kHz input signal, producing 1.0 W of output power into an 8  $\Omega$  load from a 5.0 V supply. The SSM2377 passed FCC Class B limits with 50 cm, unshielded twisted pair speaker cable. Note that reducing the power supply voltage greatly reduces radiated emissions.

### OUTPUT MODULATION DESCRIPTION

The SSM2377 uses three-level,  $\Sigma$ - $\Delta$  output modulation. Each output can swing from GND to  $V_{DD}$  and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to the constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level,  $\Sigma$ - $\Delta$  output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUT+ and OUT–) is generated to follow the input voltage. The differential pulse density ( $V_{OUT}$ ) is increased by raising the input signal level. Figure 36 depicts three-level,  $\Sigma$ - $\Delta$  output modulation with and without input stimulus.

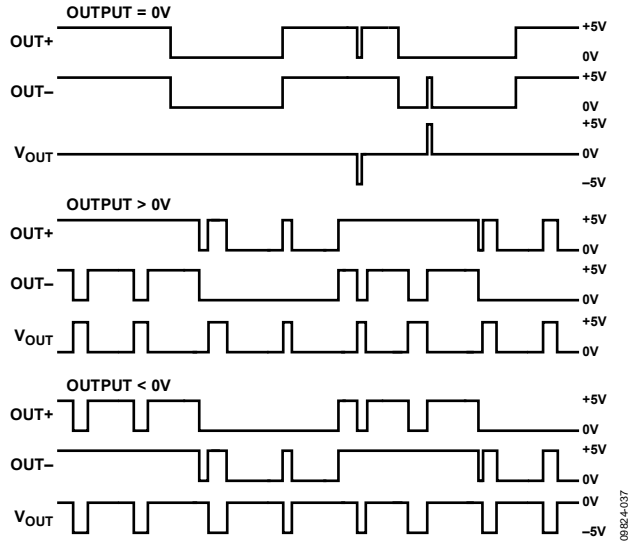


Figure 36. Three-Level,  $\Sigma$ - $\Delta$  Output Modulation With and Without Input Stimulus

## LAYOUT

As output power increases, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be directly beneath the analog power plane, and, similarly, the digital ground plane should be directly beneath the digital power plane. There should be no overlap between the analog and digital ground planes or between the analog and digital power planes.

## INPUT CAPACITOR SELECTION

The SSM2377 does not require input coupling capacitors if the input signal is biased from 1.0 V to  $V_{DD} - 1.0$  V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor ( $C_{IN}$ ) and the input impedance of the SSM2377 form a high-pass filter with a corner frequency determined by the following equation:

$$f_c = 1/(2\pi \times 80 \text{ k}\Omega \times C_{IN})$$

The input capacitor value and the dielectric material can significantly affect the performance of the circuit. Not using input capacitors can generate a large dc output offset voltage and degrade the dc PSRR performance.

## POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with a good quality, low ESL, low ESR capacitor, with a minimum value of 4.7  $\mu$ F. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1  $\mu$ F capacitor as close as possible to the VDD pins of the device. Placing the decoupling capacitors as close as possible to the SSM2377 helps to maintain efficient performance.

OUTLINE DIMENSIONS

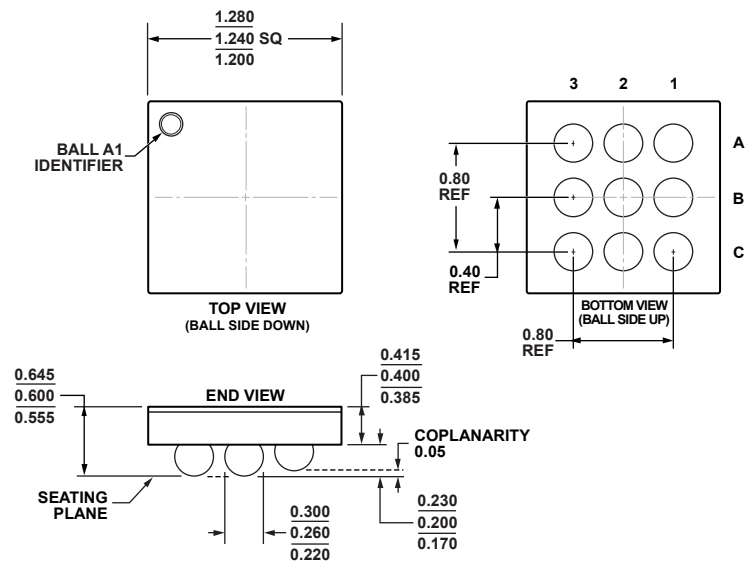


Figure 37. 9-Ball Wafer Level Chip Scale Package [WLCSP]  
(CB-9-4)  
Dimensions shown in millimeters

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ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                           | Package Option <sup>2</sup> | Branding |
|--------------------|-------------------|---|-----------------------------|----------|
| SSM2377ACBZ-RL     | −40°C to +85°C    | 9-Ball Wafer Level Chip Scale Package [WLCSP] | CB-9-4                      | Y48      |
| SSM2377ACBZ-R7     | −40°C to +85°C    | 9-Ball Wafer Level Chip Scale Package [WLCSP] | CB-9-4                      | Y48      |
| EVAL-SSM2377Z      |                   | Evaluation Board                              |                             |          |

<sup>1</sup> Z = RoHS Compliant Part.  
<sup>2</sup> This package option is halide free.

**SSM2377**

## NOTES