

### Features

- Two Independent Drivers, Each Capable of Sourcing and Sinking 5A
- CMOS and TTL Compatible Inputs
- Independent Enable for Each Driver
- 5V to 20V Supply Voltage Range
- -40°C to +125°C Extended Operating Temperature Range
- ±4kV ESD Rating (Human Body Model)
- Thermally enhanced 8-pin SOIC and 8-pin MSOP packages and standard 8-pin SOIC package
- Under Voltage Lockout Circuitry
- Fast Propagation Delays (16ns typical)
- Fast Rise and Fall Times (7ns typical)

### Applications

- Switch-Mode Power Supplies
- DC-DC Converters
- Motor Controllers
- Power Inverters



### Description

The IX4340 is a dual, high current, low side gate driver. Each of the two outputs is capable of sourcing and sinking 5A of peak current, and has a maximum voltage rating of 20V. The two outputs can be paralleled for higher current applications. Fast propagation delay times (16ns typical) and fast rise and fall times (7ns) make the IX4340 well suited for high frequency applications.

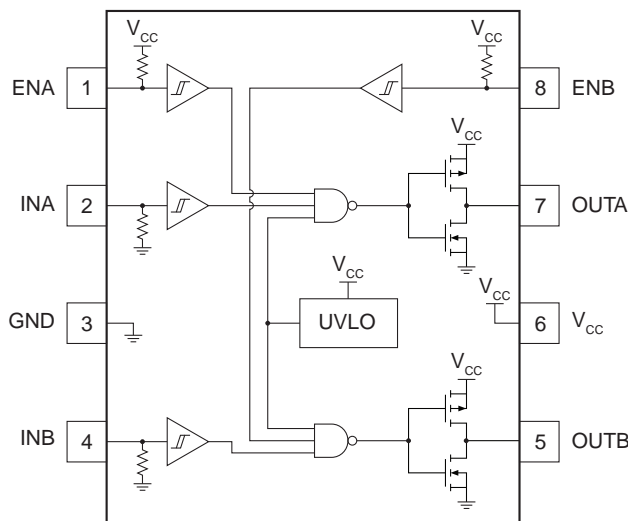
The inputs are TTL and CMOS logic compatible, and there is an independent Enable function for each output. Under voltage lockout circuitry (UVLO) prevents the high side source driver from conducting until there is sufficient supply voltage. The outputs are held low if the logic inputs are floating.

The IX4340 is available in standard 8-pin SOIC and thermally enhanced 8-pin SOIC and MSOP packages.

### Ordering Information

Part Number	Description
IX4340N	8-Pin SOIC (100/Tube)
IX4340NTR	8-Pin SOIC (4000/Reel)
IX4340NE	8-Pin SOIC w/ Exposed Thermal Pad (100/Tube)
IX4340NETR	8-Pin SOIC w/ Exposed Thermal Pad (4000/Reel)
IX4340UE	8-Pin MSOP w/ Exposed Thermal Pad (80/Tube)
IX4340UETR	8-Pin MSOP w/ Exposed Thermal Pad (5000/Reel)

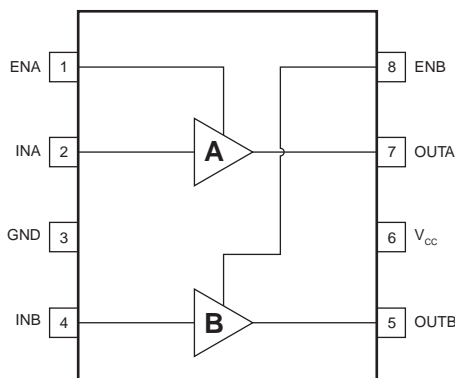
### IX4340 Functional Block Diagram



<b>1. Specifications</b>	<b>3</b>
1.1 Pin Configuration	3
1.2 Logic Table	3
1.3 Pin Definitions	3
1.4 Absolute Maximum Ratings	3
1.5 Electrical Characteristics	4
1.6 Thermal Characteristics	4
<b>2. Performance Data</b>	<b>5</b>
<b>3. Manufacturing Information</b>	<b>7</b>
3.1 Moisture Sensitivity	7
3.2 ESD Sensitivity	7
3.3 Soldering Profile	7
3.4 Board Wash	7
3.5 Mechanical Dimensions	8

## 1 Specifications

### 1.1 Pin Configuration



### 1.2 Logic Table

IXx	ENx	V <sub>CC</sub>	OUTx
1	1	V <sub>CC</sub> >UVLO <sub>ON</sub>	1
0	1	V <sub>CC</sub> >UVLO <sub>ON</sub>	0
x	0	V <sub>CC</sub> >UVLO <sub>ON</sub>	0
x	x	V <sub>CC</sub> <UVLO <sub>ON</sub>	0

### 1.3 Pin Definitions

Pin #	Name	Description
1	ENA	Enable input for Channel A. A logic high (or floating) enables Channel A (the state of OUTA is determined by INA). A logic low disables OUTA (OUTA held low regardless of INA).
2	INA	Channel A logic input. Internally pulled to GND.
3	GND	Ground. Common ground reference for the device.
4	INB	Channel B logic input. Internally pulled to GND.
5	OUTB	Channel B output, capable of sourcing and sinking 5A
6	V <sub>CC</sub>	Supply Voltage.
7	OUTA	Channel A output, capable of sourcing and sinking 5A
8	ENB	Enable input for Channel B. A logic high (or floating) enables Channel B (the state of OUTB is determined by INB). A logic low disables OUTB (OUTB held low regardless of INB).

The thermal pad on the bottom of the thermally enhanced devices, IX4340NE and IX4340UE, may be connected to GND or left floating; it must not be connected to any other net. The thermal pad is not intended to carry current.

### 1.4 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V <sub>CC</sub>	-0.3	20	V
Input Voltage	V <sub>IN</sub>	-0.3	20	V
Output Current	I <sub>OUT</sub>	-	±5	A
ESD Rating (Human Body Model)	V <sub>ESD</sub>	-4000	+4000	V
Junction Temperature	T <sub>J</sub>	-55	+150	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C

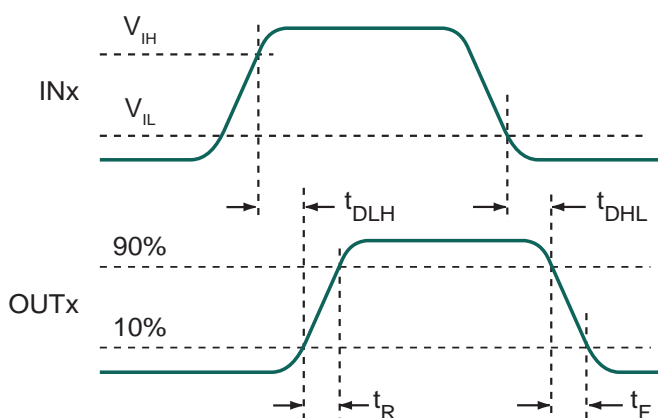
Absolute maximum electrical ratings are at T<sub>A</sub>=25°C

*Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.*

## 1.5 Electrical Characteristics

$V_{CC} = 12V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Supply						
Supply Current	OUTA and OUTB Open	I <sub>CC</sub>	-	1.4	2.5	mA
Under Voltage Lockout (UVLO)						
UVLO Rising Threshold	V <sub>CC</sub> Rising	UVLO <sub>ON</sub>	3.5	3.85	4.2	V
UVLO Falling Threshold	V <sub>CC</sub> Falling	UVLO <sub>OFF</sub>	3.1	3.3	3.5	
UVLO Threshold Hysteresis	-	UVLO <sub>HYS</sub>	0.2	0.5	0.8	
Logic Inputs (INA, INB, ENA, ENB)						
Input Low Voltage	-	V <sub>IL</sub>	-	-	0.8	V
Input High Voltage	-	V <sub>IH</sub>	2.5	-	-	
Output Drivers (OUTA, OUTB)						
Output Pull-Up Resistance	I <sub>OUT</sub> = -100mA, T <sub>J</sub> = 25°C	R <sub>OH</sub>	-	1	1.5	Ω
	I <sub>OUT</sub> = -100mA		-	1.3	1.8	
Output Pull-Down Resistance	I <sub>OUT</sub> = 100mA, T <sub>J</sub> = 25°C	R <sub>OL</sub>	-	0.6	1.1	
	I <sub>OUT</sub> = 100mA		-	0.8	1.4	
Rise Time	C <sub>LOAD</sub> = 1.8nF	t <sub>R</sub>	-	7	15	ns
Fall Time	C <sub>LOAD</sub> = 1.8nF	t <sub>F</sub>	-	7	15	
Propagation Delay, Low to High	C <sub>LOAD</sub> = 1.8nF	t <sub>DLH</sub>	5	16	30	
Propagation Delay, High to Low	C <sub>LOAD</sub> = 1.8nF	t <sub>DHL</sub>	5	16	30	
Propagation Delay Matching	-	t <sub>M</sub>	-5	-	5	

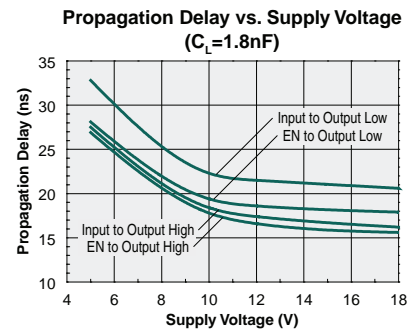
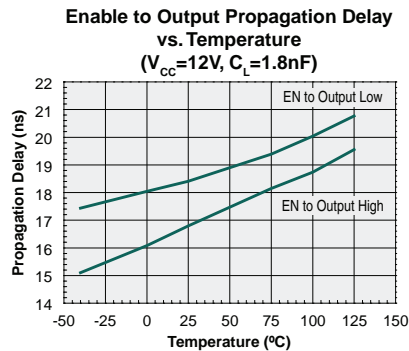
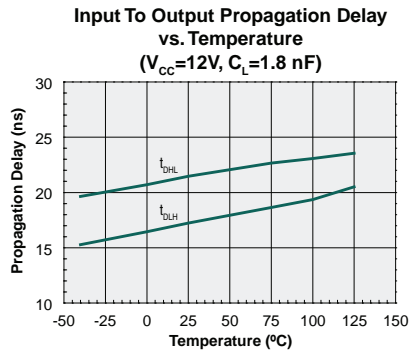
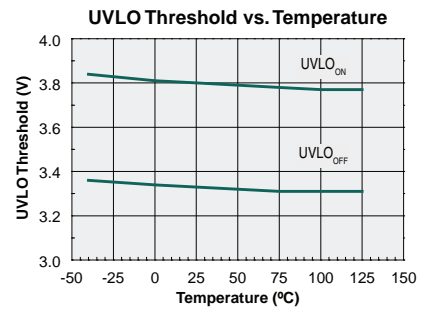
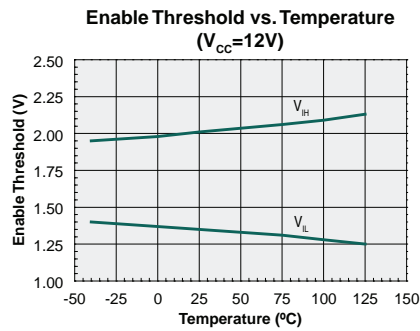
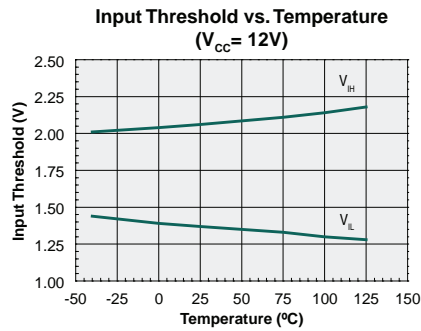
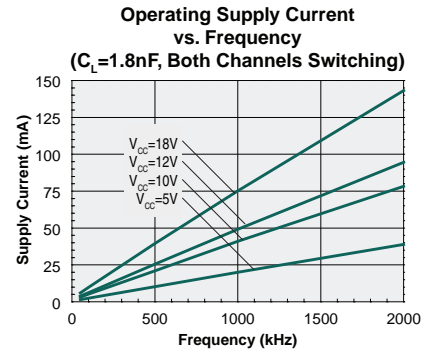
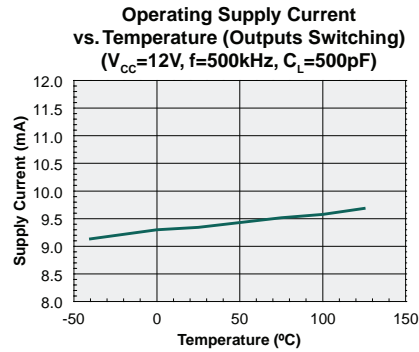
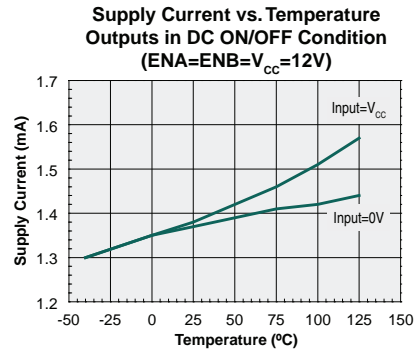


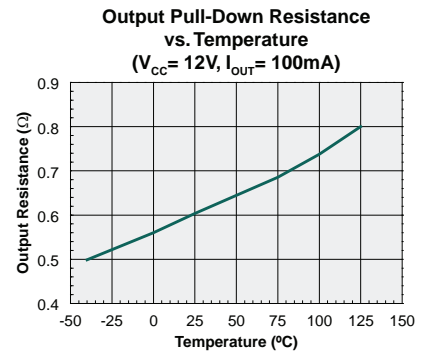
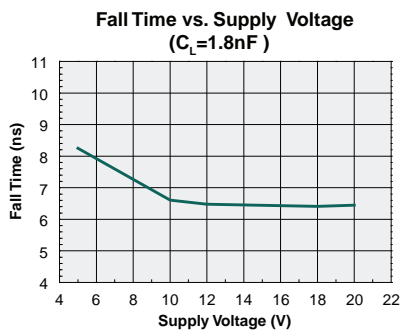
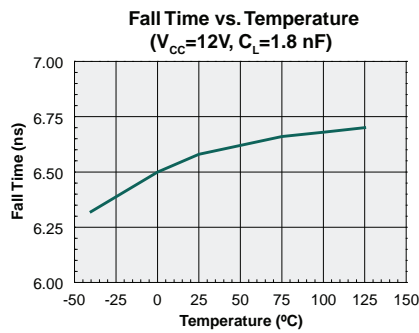
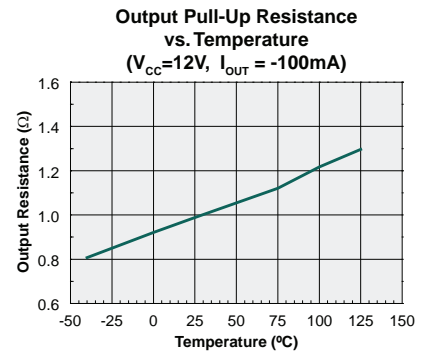
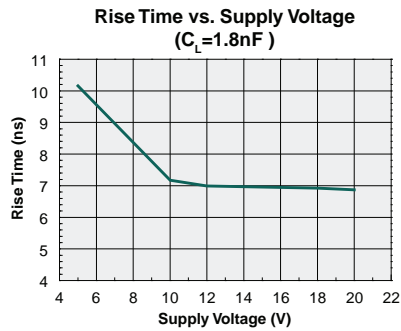
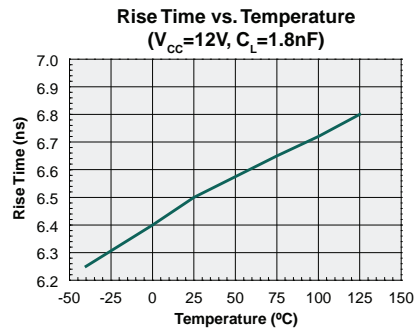
## 1.6 Thermal Characteristics

Parameter	Symbol	Rating	Units
IX4340N Thermal Impedance, Junction to Ambient	$\theta_{JA}$	120	$^{\circ}C/W$
IX4340NE Thermal Impedance, Junction-to-Ambient	$\theta_{JA}$	85	
IX4340NE Thermal Impedance, Junction-to-Case	$\theta_{JC}$	10	
IX4340UE Thermal Impedance, Junction-to-Ambient	$\theta_{JA}$	40	
IX4340UE Thermal Impedance, Junction-to-Case	$\theta_{JC}$	10	

## 2 Performance Data

Unless otherwise noted, data presented in these graphs is typical of device operation at  $T_A=25^\circ\text{C}$ .





### 3 Manufacturing Information

#### 3.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation.

We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4340N & IX4340NE	MSL 1
IX4340UE	MSL 2

#### 3.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 3.3 Soldering Profile

Provided in the table below is the Classification Temperature ( $T_C$ ) of this product and the maximum dwell time the body temperature of this device may be ( $T_C - 5$ )°C or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

Device	Classification Temperature ( $T_C$ )	Dwell Time ( $t_p$ )	Max Reflow Cycles
IX4340N, IX4340NE, & IX4340UE	260°C	30 seconds	3

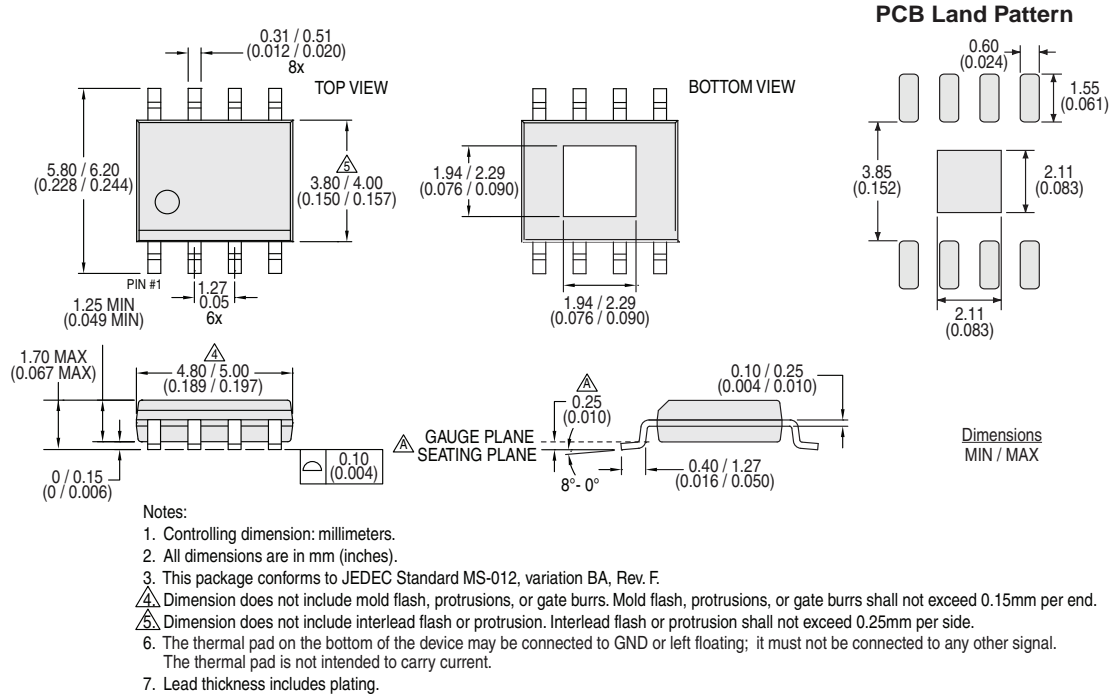
#### 3.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

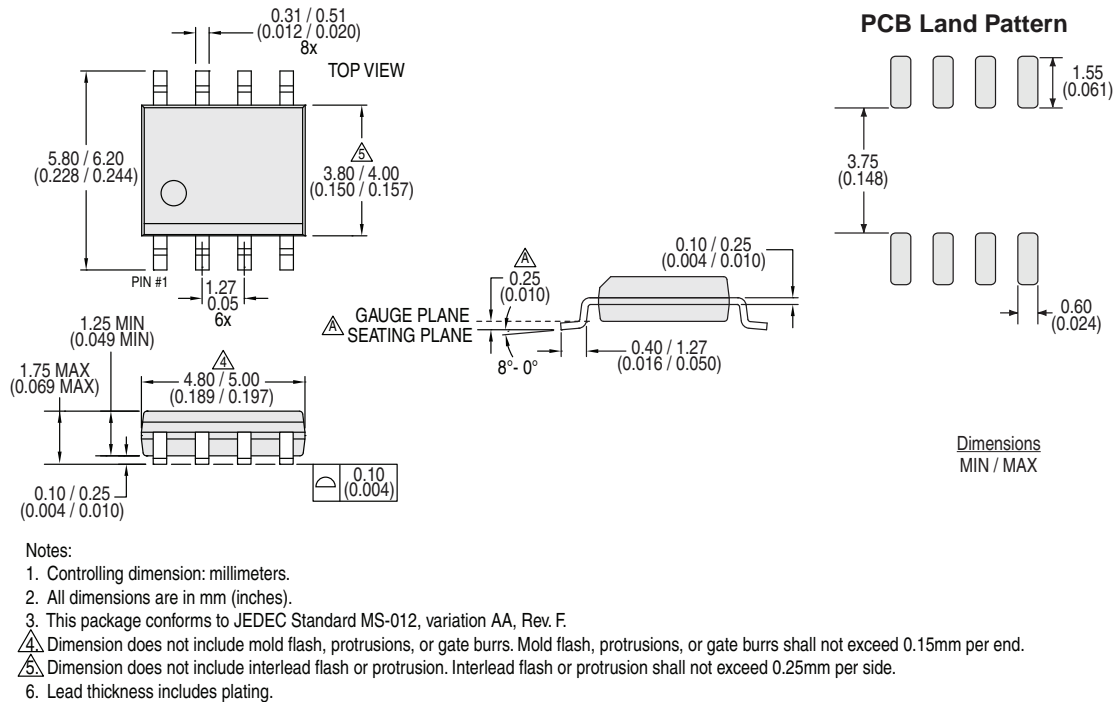


### 3.5 Mechanical Dimensions

#### 3.5.1 IX4340NE Package Dimensions

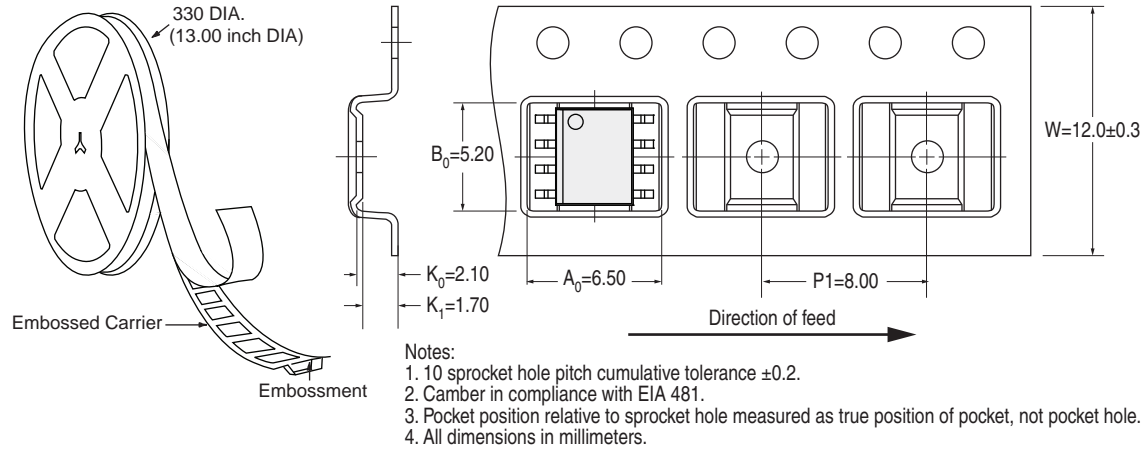


#### 3.5.2 IX4340N Package Dimensions

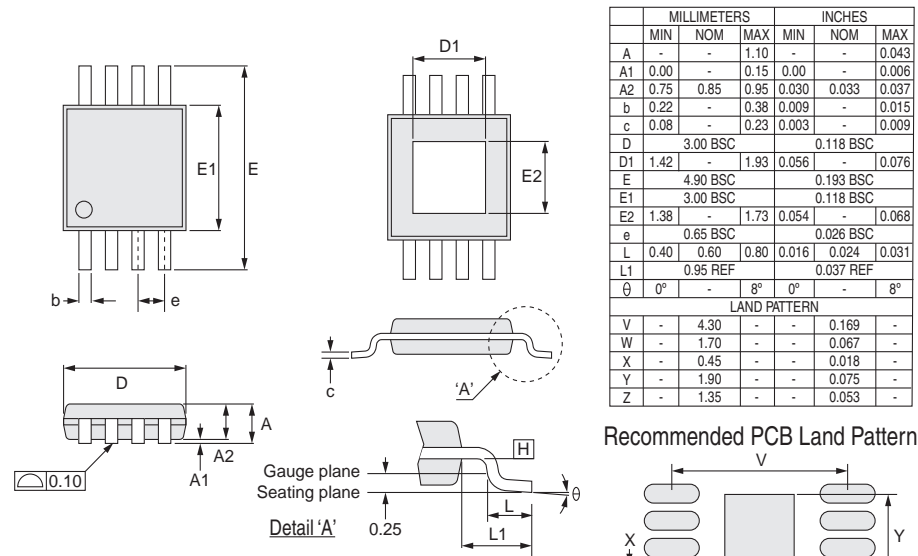




### 3.5.3 IX4340NTR & IX4340NETR Tape & Reel Dimensions



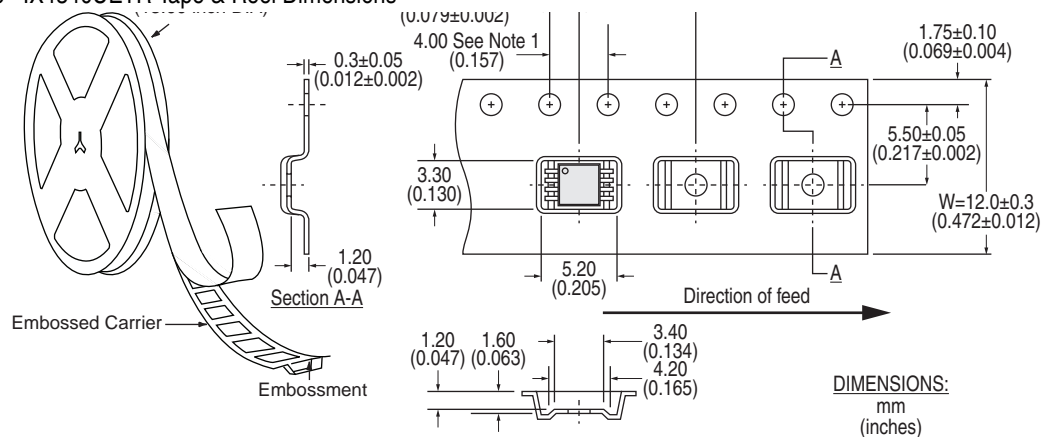
### 3.5.4 IX4340UE Package Dimensions



#### Notes:

1. JEDEC outline: Thermally enhanced: MO-187 AA-T.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per end.
3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07mm.
4. D and E1 dimensions are determined at datum [H].
5. The thermal pad on the bottom of the device may be connected to GND or left floating; it must not be connected to any other signal. The thermal pad is not intended to carry current.

### 3.5.5 IX4340UETR Tape & Reel Dimensions



1. 10 sprocket hole pitch cumulative tolerance: ±0.2 (0.008).
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

For additional information please visit our website at: [www.ixysic.com](http://www.ixysic.com)

IXYS Integrated Circuits Division makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. Neither circuit patent licenses nor indemnity are expressed or implied. Except as set forth in IXYS Integrated Circuits Division's Standard Terms and Conditions of Sale, IXYS Integrated Circuits Division assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

The products described in this document are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or where malfunction of IXYS Integrated Circuits Division's product may result in direct physical harm, injury, or death to a person or severe property or environmental damage. IXYS Integrated Circuits Division reserves the right to discontinue or make changes to its products at any time without notice.

Specification: DS-IX4340-R06  
©Copyright 2019, IXYS Integrated Circuits Division  
All rights reserved. Printed in USA.  
1/2/2019