



STD12NF06L STD12NF06L-1

N-channel 60V - 0.08Ω - 12A - DPAK - IPAK
STripFET™ II Power MOSFET

General features

Type	V _{DSSS}	R _{DS(on)}	I _D
STD12NF06L	60V	<0.1Ω	12A
STD12NF06L-1	60V	<0.1Ω	12A

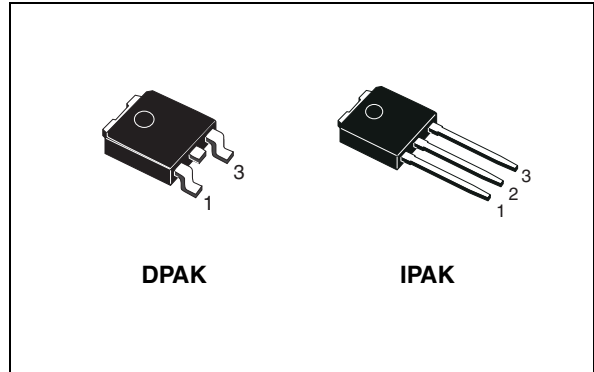
- Exceptional dv/dt capability
- Low gate charge

Description

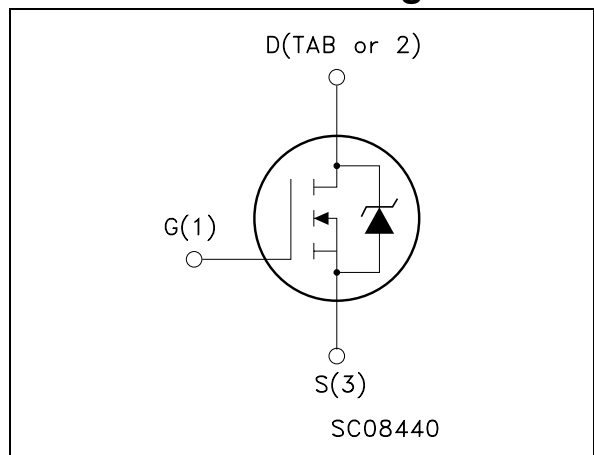
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD12NF06LT4	D12NF06L	DPAK	Tape & reel
STD12NF06L-1	D12NF06L	IPAK	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	60	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	12	A
I_D	Drain current (continuous) at $T_C = 100^\circ C$	8.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	30	W
	Derating factor	0.2	W/ $^\circ C$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	100	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ C$
T_J	Max. operating junction temperature		

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 12A$, $di/dt \leq 200A/\mu s$, $V_{DS} \leq 40V$, $T_J \leq T_{JMAX}$

3. Starting $T_J = 25^\circ C$, $I_D = 6A$, $V_{DD} = 30V$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	5	$^\circ C/W$
R_{thJA}	Thermal resistance junction-ambient Max	100	$^\circ C/W$
T_I	Maximum lead temperature for soldering purpose	275	$^\circ C$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25\text{mA}$, $V_{GS} = 0$	60			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1		2	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$ $V_{GS} = 5\text{V}$, $I_D = 6\text{A}$		0.08 0.10	0.10 0.12	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 25\text{V}$, $I_D = 6\text{A}$		7		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		350		pF
C_{oss}	Output capacitance			75		pF
C_{rss}	Reverse transfer capacitance			30		pF
Q_g	Total gate charge	$V_{DD} = 48\text{V}$, $I_D = 12\text{A}$ $V_{GS} = 5\text{V}$		7.5	10	nC
Q_{gs}	Gate-source charge			2.5		nC
Q_{gd}	Gate-drain charge			3.0		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{V}$, $I_D = 6\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ <i>Figure 12 on page 8</i>		10		ns
t_r	Rise time			35		ns
$t_{d(off)}$	Turn-off delay time			20		ns
t_f	Fall time			13		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				12	A
I_{SDM}	Source-drain current (pulsed)				48	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12A, V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 12A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 16V, T_J = 150^\circ C$ Figure 14 on page 8		50 65 2.5		ns μC A

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

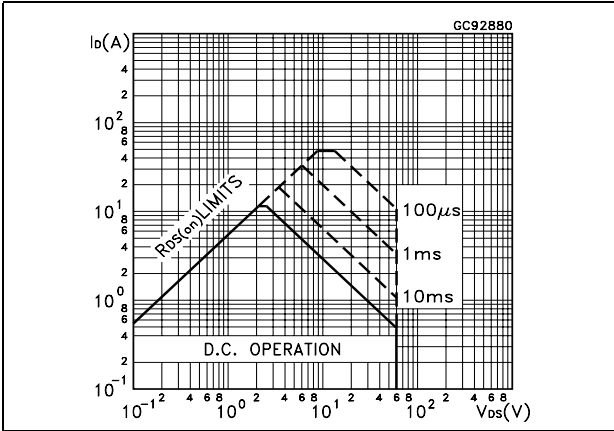


Figure 2. Thermal impedance

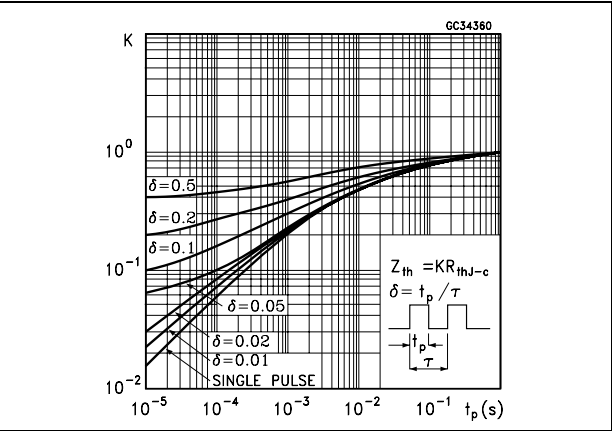


Figure 3. Output characteristics

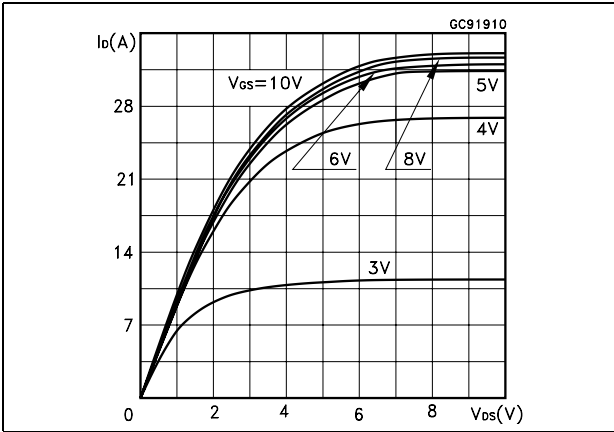


Figure 4. Transfer characteristics

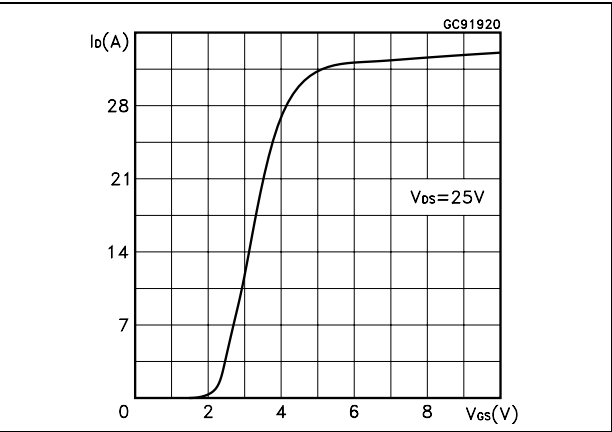


Figure 5. Transconductance

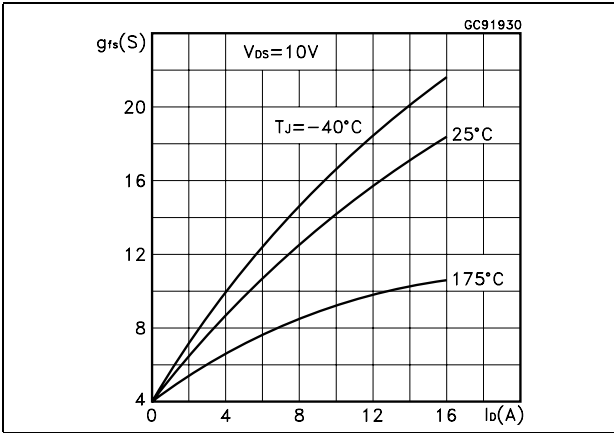


Figure 6. Static drain-source on resistance

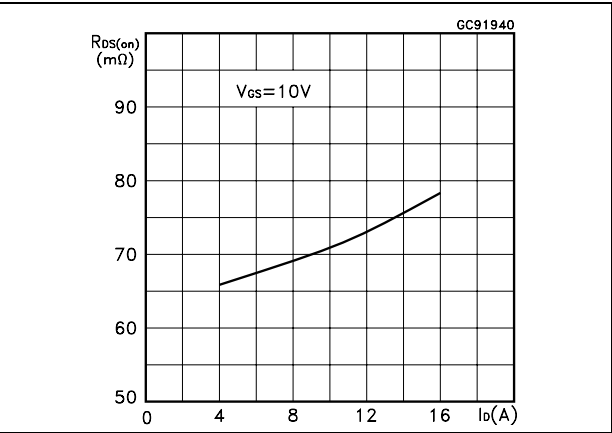


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

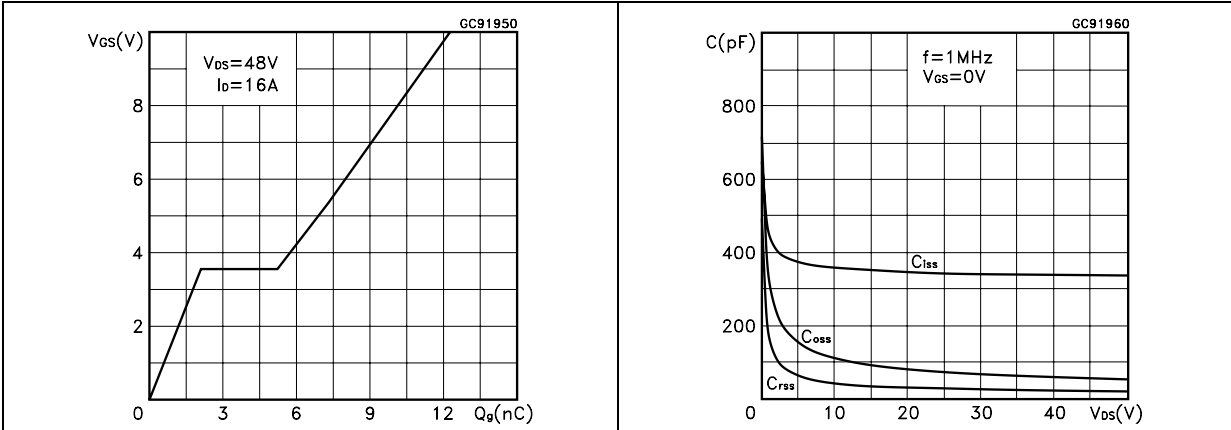


Figure 9. Normalized gate threshold voltage vs. temperature Figure 10. Normalized on resistance vs. temperature

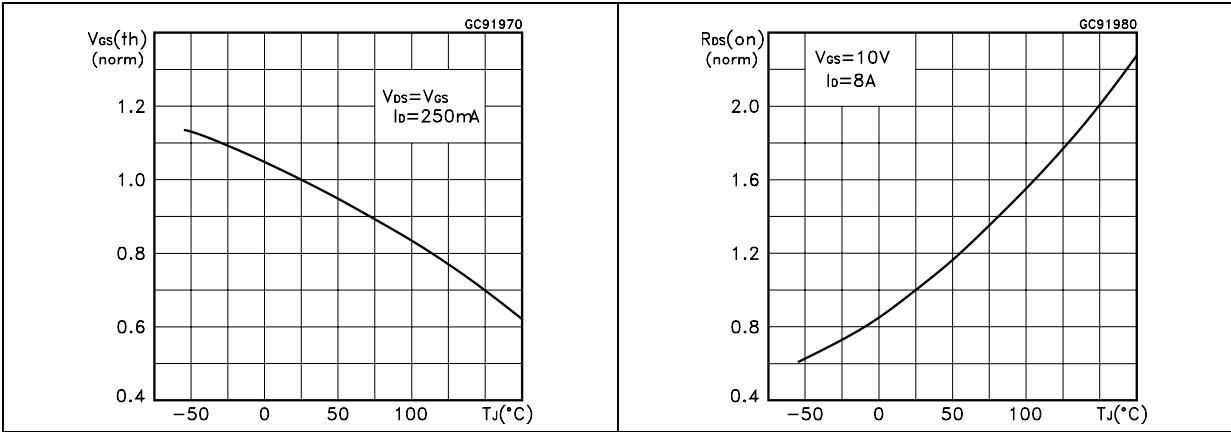
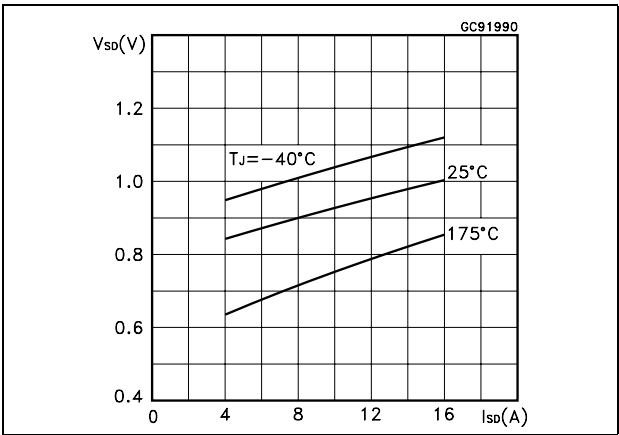


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

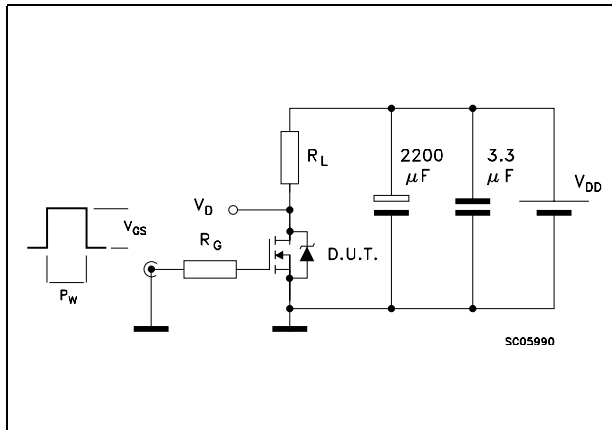


Figure 13. Gate charge test circuit

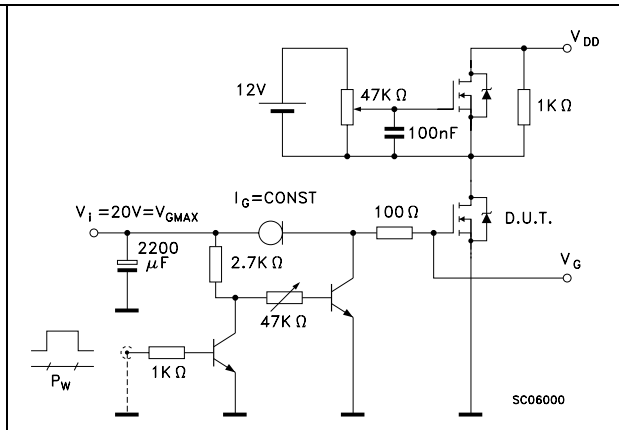


Figure 14. Test circuit for inductive load switching and diode recovery times

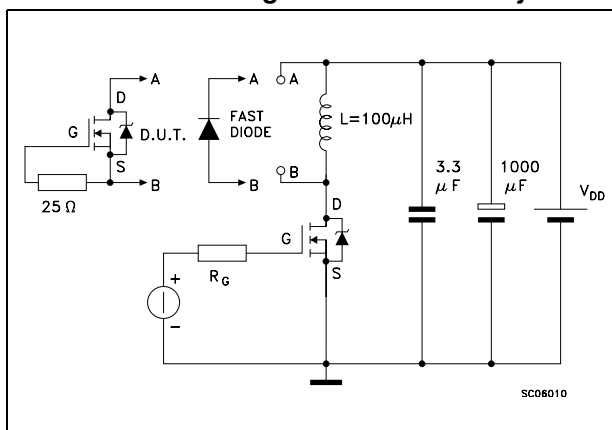


Figure 15. Unclamped Inductive load test circuit

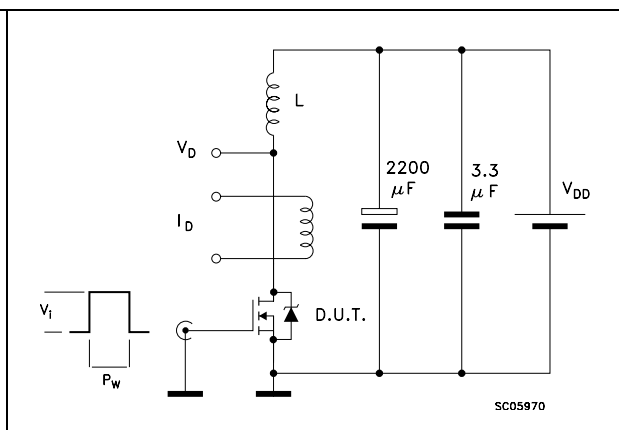
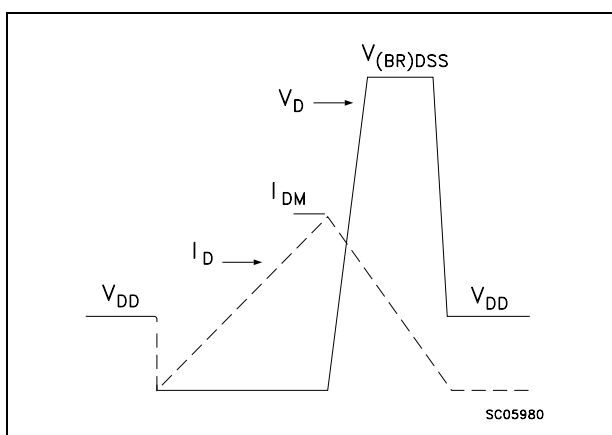


Figure 16. Unclamped inductive waveform

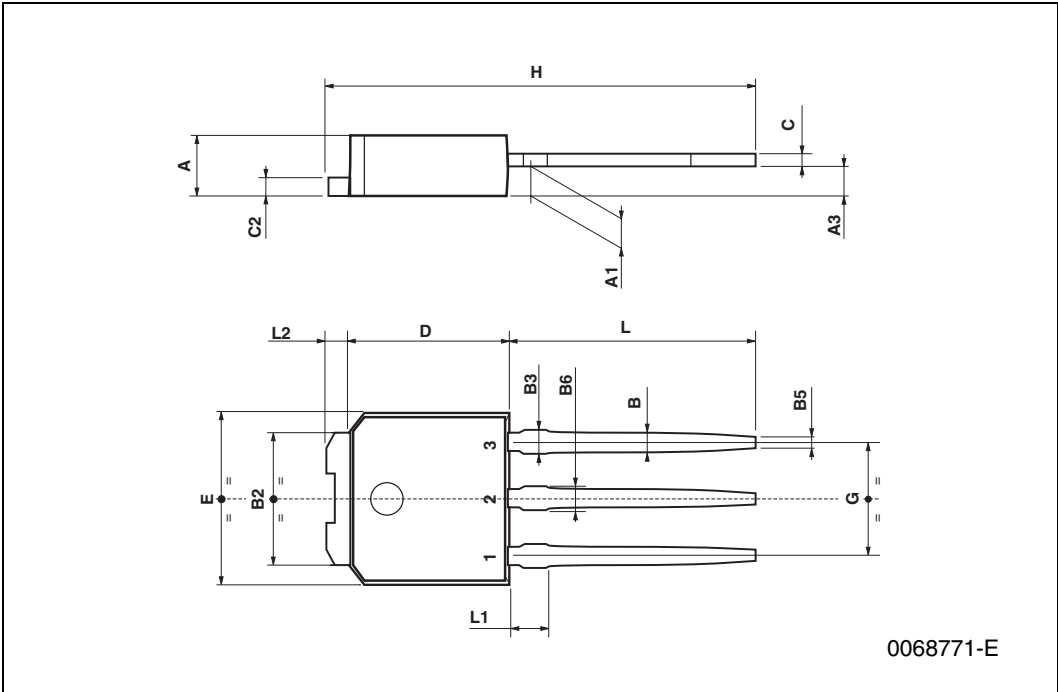


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



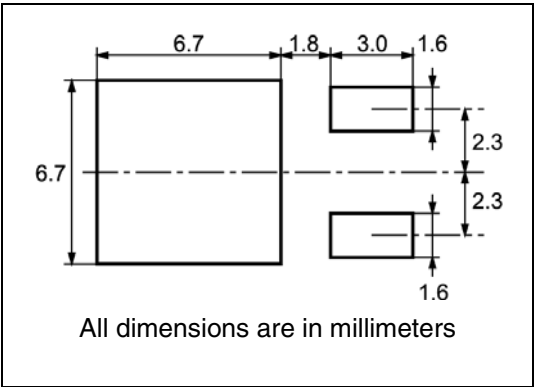
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the STD12NF06L DPAK package. It includes a top view showing dimensions E, b4, L2, L4, H, e, e1, and b(2x). A side view shows dimensions A, c2, D, A1, c, and R. A detail view of the thermal pad shows dimensions E1, D1, and a thermal pad area. A bottom view shows dimensions A2, L, (L1), V2, and a gauge plane with a 0.25mm dimension. The drawing also indicates the seating plane and the gauge plane.

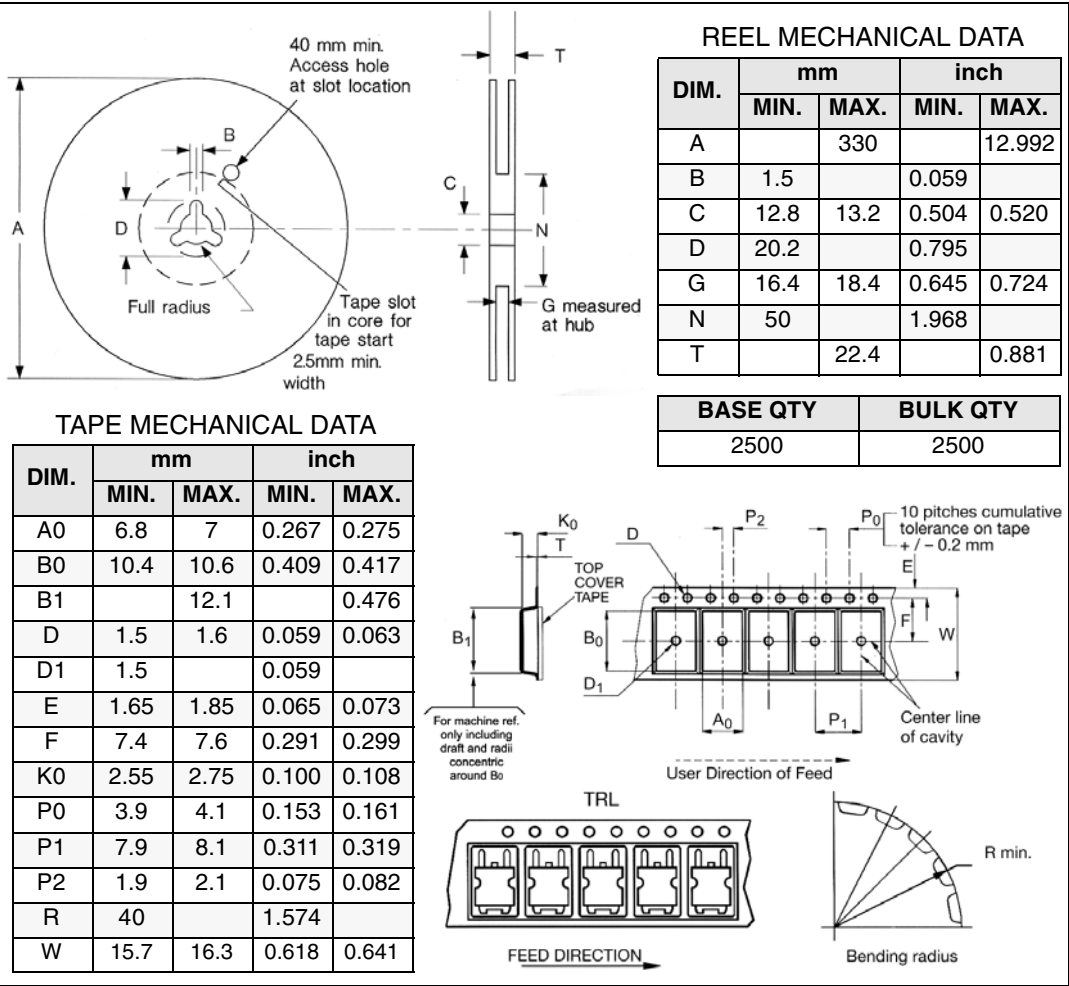
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5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	4	Complete document
08-Aug-2006	5	New template, no content change
19-Feb-2007	6	Typo mistake on page 1

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