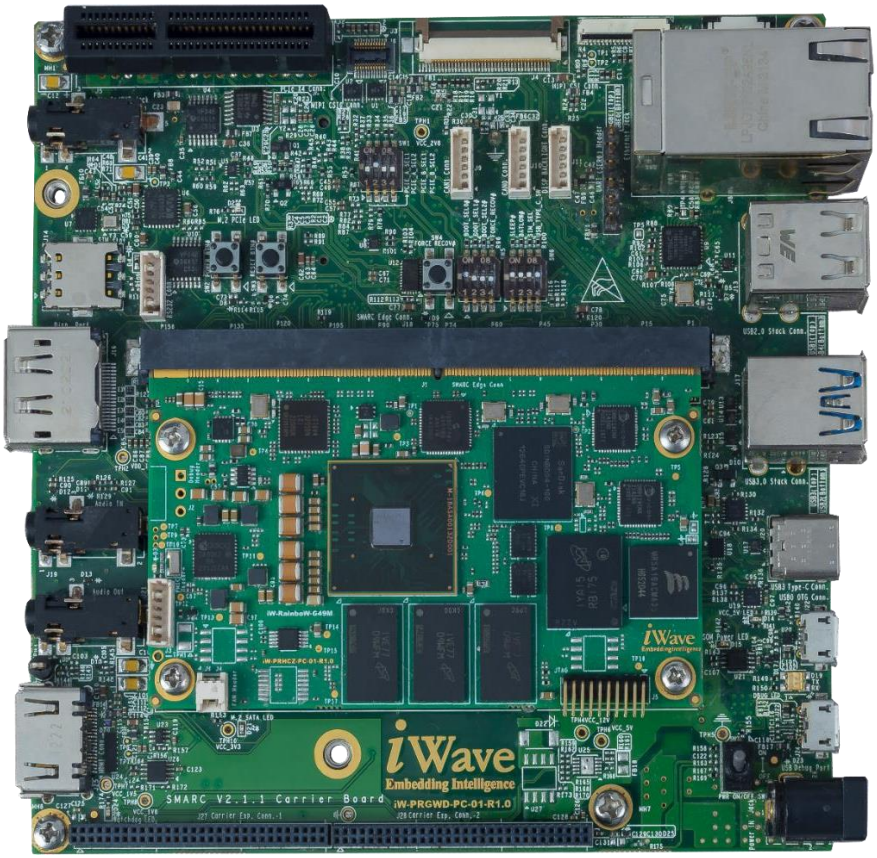
iW-RainboW-G49D
QorIQ Layerscape LS1021A
SMARC Development Platform
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Layerscape LS1021A SMARC V2.1.1 Development platform "iW-RainboW-G49D" based on the NXP's LS1021A Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Layerscape LS1021A based SMARC development platform from a Hardware Systems perspective. Complete information about the Layerscape LS1021A SMARC SOM is explained in another document "iW-RainboW-G49M_LS1021A_SMARC_SOM-HardwareUserGuide".

1.2 Overview

The SMARC V2.1.1 ("Smart Mobility Architecture") is a versatile small form factor computer Module definition targeting application that require low power, low costs, and high performance. The Module power envelope is typically under 6W although designs up to about 15W are possible.

iW-RainboW-G49D Development Platform comes with SMARC V2.1.1 Generic Carrier, Layerscape LS1021A based SMARC V2.1.1 SOM. The development board can be used for quick prototyping of various applications targeted by the LS1021A processor. With the 120mmx120mm Nano ITX size, SMARC carrier board is highly packed with all the necessary on-board connectors to validate the SMARC features of Layerscape LS1021A SMARC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DP	Display Port
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
Hz	Hertz
I2C	Inter-Integrated Circuit

Acronyms	Abbreviations
I2S	Inter-IC Sound
IC	Integrated Circuit
LVDS	Low Voltage Differential Signalling
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
MXM	Mobile PCI Express Module
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SMARC	Smart Mobility ARChitecture
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface signals
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

1.5 References

- LS1021A_Rev7.pdf
- LS1021ARM_Rev3.1.pdf
- SMARC Specification V2.1.1

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Layerscape LS1021A SMARC SOM features and Hardware architecture with high level block diagram.

2.1 Layerscape LS1021A SMARC Development Platform Block Diagram

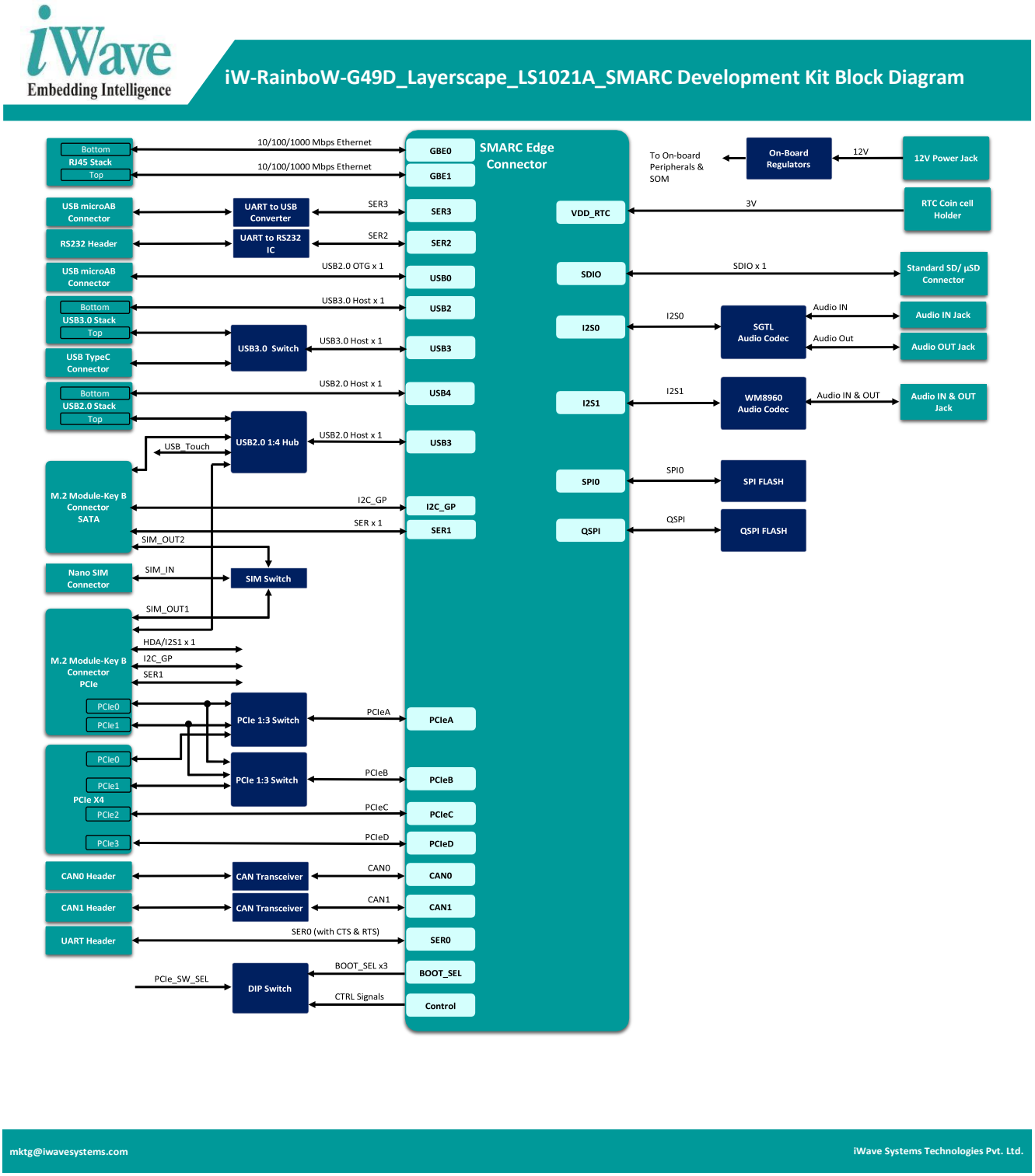


Figure 1: Layerscape LS1021A SMARC Development Platform Block Diagram

2.2 Layerscape LS1021A SMARC Development Platform Features

The NXP's Layerscape LS1021A SMARC carrier board supports the following features to validate the NXP's Layerscape LS1021A SMARC SOM Edge connector interface.

Serial Interface Features

- Debug UART through USB Micro AB Connector
- RS232 UART x 1 Port through Header (Optional)
- Data UART x 1 Port through Header

High Speed Interface Features

- PCIe x 1 Port through x4 connector or M.2 connector [1,2]
- SATA x 1 Port through M.2 connector (Optional)
- USB 3.0 Host x 2 Port through USB 3.0 Type A Connector[3]
- USB Type C x 1 Port[3]

Communication Features

- Dual 10/100/1000Mbps Ethernet through RJ45MagJack
- USB 2.0 Host x 2 Port through USB 2.0 Type A Connector
- USB 2.0 OTG x 1 Port through Micro AB Connector
- SDHC/SDIO (4bit) x 1 Port through Standard SD Connector (Optional)
- CAN x 2 Port Through Header

Audio/Video Features

- Dual I2S Audio Codec with 3.5mm Audio IN and OUT Jack

Additional Features

- QSPI and SPI Flash
- RTC Coin Cell holder

On Board Switches

- Power ON/OFF Switch
- Board Configuration Switch
- Reset Switch
- Force Boot Switch (Not supported)

Carrier board Expansion Connectors

- SPI x 1 Port
- CAN x 1 Port
- USB3.0 Host x 2 Ports (through On-SOM USB Hub)
- UART x 1 Port

- I2C x 1 Port
- WDT Time Out x 1
- TAMPER In & Out
- GPIOs

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Temperature Supported : 0°C to +60°C
- Form Factor : 120mm X 120mm Nano ITX

[1.] PCIe Channel A can be connected to either M.2 Connector or PETp0 of PCIe X4 connector by using on Board Switches, whereas PCIe Channel B can be connected to either M.2 Connector or PETp1 of PCIe X4 connector by using on Board Switches.

[2.] At a time, do not set Both the PCIe Channel A & B neither to M.2 connector nor to PCIe X4 connector.

[3.] Either USB Type C connector or USB 3.0 Type A TOP connector can be supported at a time. Anyone can be selected using on Board Switches.

2.3 SMARC MXM Connector

The Layerscape LS1021A SMARC carrier board supports 314Pin SMARC MXM Edge mating connector for SMARC SOM attachment. This standard 314-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This SMARC MXM connector (J18) is physically located at the top of the board as shown below.

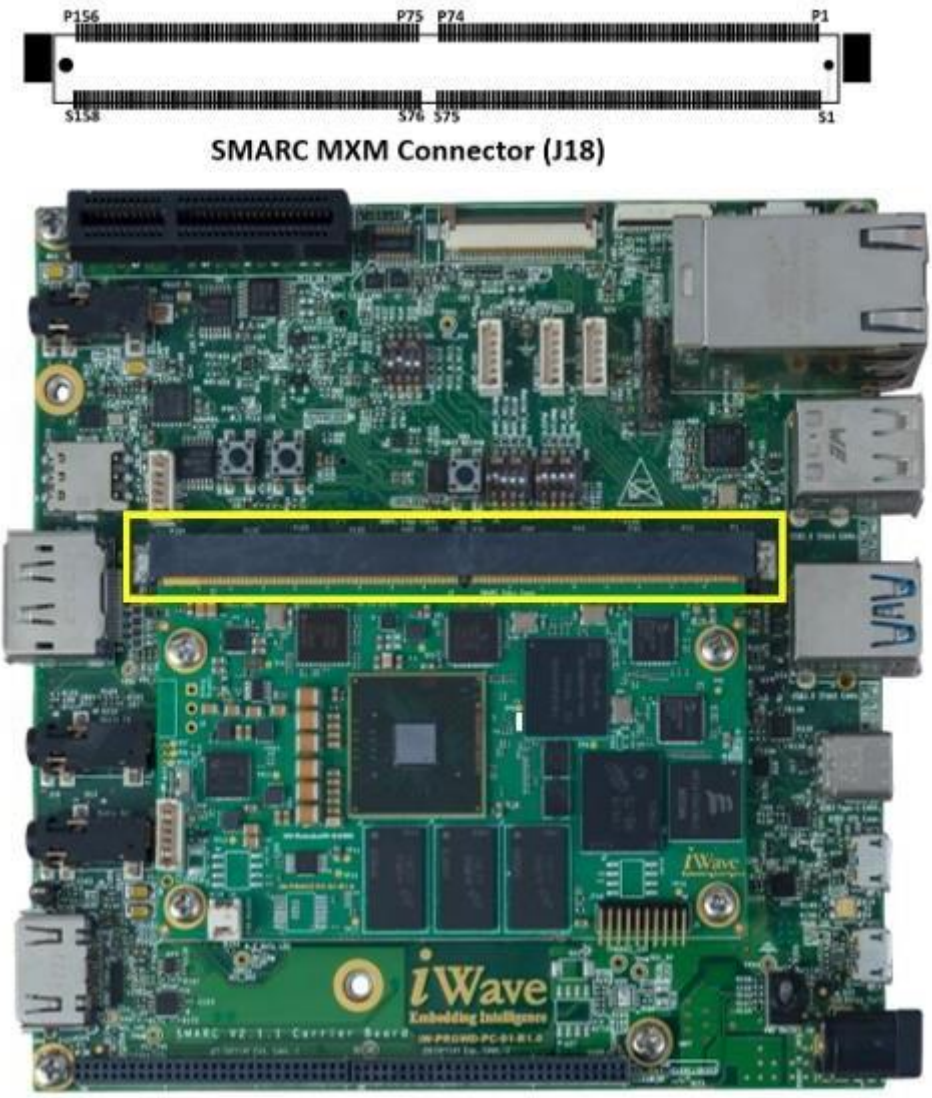


Figure 2: SMARC MXM Connector

2.3.1 SMARC PCB Edge Connector Pin Assignment

Table 3: SMARC PCB Edge Connector Pin Assignment

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
SMARC Primary Side					
P1	SMB_ALERT#	SMBUS_ALERT(GPIO 0_16)	GPT0_COMPARE/ AW53	O, 1.8V CMOS	SM Bus Alert# (interrupt) signal
P2	GND	GND	NA	Power	Ground.
P3	CSI1_CK+	NC	NA	NA	NA
P4	CSI1_CK-	NC	NA	NA	NA
P5	GBE1_SDP	NC	NA	NA	NA
P6	GBE0_SDP	NC	NA	NA	NA
P7	CSI1_RX0+	NC	NA	NA	NA
P8	CSI1_RX0-	NC	NA	NA	NA
P9	GND	GND	NA	Power	Ground.
P10	CSI1_RX1+	NC	NA	NA	NA
P11	CSI1_RX1-	NC	NA	NA	NA
P12	GND	GND	NA	Power	Ground.
P13	CSI1_RX2+	NC	NA	NA	NA
P14	CSI1_RX2-	NC	NA	NA	NA
P15	GND	GND	NA	Power	Ground.
P16	CSI1_RX3+	NC	NA	NA	NA
P17	CSI1_RX3-	NC	NA	NA	NA
P18	GND	GND	NA	Power	Ground.
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	GBE0_LINK100#	NA	I, 3.3V CMOS	100Mbps Ethernet link status LED
P22	GBE0_LINK1000#	GBE0_LINK1000#	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet activity status
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
P28	GBE0_CTREF	VCC_2V5_ETH	NA	Power	Power for the Centre Tap of Mack Jack connector
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.
P31	SPI0_CS1#	NC	NA	NA	NA
P32	GND	GND	NA	Power	Ground.
P33	SDIO_WP	SDIO_WP_SMARC	SDHC_DAT4/H2	0, 3.3V CMOS	NC (Note: Optionally SD write Protect.) Note: 10K pullup option is provided.
P34	SDIO_CMD	EMMC_CMD_SMARC	eMMC_CMD/E2	IO, 1.8/3.3V CMOS	NC (Note: Optionally SD command..) Note: 10K pullup option is provided.
P35	SDIO_CD#	SDIO_CD#_SMARC	eMMC_DATA5/H1	I,3.3V/CMOS 10K PU	NC (Note: Optionally SD Card Detect.) 10K pullup option is provided.
P36	SDIO_CK	EMMC_CLK_SMARC	eMMC_CLK_B/D1	O, 1.8/3.3V CMOS	NC (Note: Optionally SD Clock.)
P37	SDIO_PWR_EN	GPIO3_06_3V3	GPIO3_06/W6	O, 3.3V CMOS	NC (Note: Optionally SD Power enable.)
P38	GND	GND	NA	Power	Ground.
P39	SDIO_D0	EMMC_DATA0_SMARC	eMMC_DATA0/E1	IO, 1.8/3.3V CMOS 10K PU	NC (Note: Optionally SD data 0.) 10K pullup option is provided.
P40	SDIO_D1	EMMC_DATA1_SMARC	eMMC_DATA1/F2	IO, 1.8/3.3V CMOS 10K PU	NC (Note: Optionally SD data 1.) 10K pullup option is provided.
P41	SDIO_D2	EMMC_DATA2_SMARC	eMMC_DATA2/F1	IO, 1.8/3.3V CMOS 10K PU	NC (Note: Optionally SD data 2.) 10K pullup option is provided.
P42	SDIO_D3	EMMC_DATA3_SMARC	eMMC_DATA3/G1	IO, 1.8/3.3V CMOS 10K PU	NC (Note: Optionally SD Data3.) Note: 10K pullup option is provided.
P43	SPI0_CS0#	SPI0_CS0#	SPI1_PCS0	SPI1_PCS0/D17	O, 1.8V CMOS
P44	SPI0_CK	SPI0_CK	SPI1_SCK	SPI1_SCK/C18	O, 1.8V CMOS/ 33E Series

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P45	SPI0_DIN	SPI0_DIN	SPI1_SIN	NA	I, 1.8V CMOS
P46	SPI0_DO	SPI0_DO	SPI1_SOUT	IFC_AD13/SPI1_SOUT/B15	O, 1.8V CMOS
P47	GND	GND	NA	Power	Ground.
P48	SATA_TX+	SATA_TX+	LS_SD1_TX1_P/W11	I, SATA / 0.022uF AC Couple	NC (Note: OptionallySATA Transmit Lane Positive)
P49	SATA_TX-	SATA_TX-	LS_SD1_TX1_N/Y11	I, SATA / 0.022uF AC Couple	NC (Note: Optionally SATA Transmit Lane Negative)
P50	GND	GND	NA	Power	Ground.
P51	SATA_RX+	SATA_RX+	LS_SD1_RX1_P/AC11	O, SATA / 0.022uF AC Couple	NC (Note: Optionally SATA Receive Lane Positive)
P52	SATA_RX-	SATA_RX-	LS_SD1_RX1_N/AB11	O, SATA / 0.022uF AC Couple	NC (Note: Optionally SATA Receive Lane Negative)
P53	GND	GND	NA	Power	Ground.
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	QSPI_CS_A0	IFC_ADD16/QSPI_CS_A0/C8	O, 1.8V CMOS	NC (Note: Optionally QSPI Chip Select 0.)
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	QSPI_CS_A1	IFC_ADD17/QSPI_CS_A1 /D8	O, 1.8V CMOS	NC (Note: Optionally QSPI Chip Select 1.)
P56	SPI1_CK / ESPI_CK / QSPI_CK	QSPI_CK_A	IFC_ADD18/QSPI_CK_A /C9	O, 1.8V CMOS	NC (Note: Optionally QSPI Clock)
P57	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	QSPI_DIO_A1	IFC_ADD23/QSPI_DIO_A1 /D11	IO,1V8 CMOS	NC (Note: Optionally QSPI1A DATA lane 1)
P58	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	QSPI_DIO_A0	IFC_ADD22/QSPI_DIO_A0 /C11	IO,1V8 CMOS	NC (Note: Optionally QSPI1A DATA lane 0)
P59	GND	GND	NA	Power	Ground.
P60	USB0+	LS_USB1_DP_OTG	LS_USB1_DP/D3	IO, USB	USB2.0 Port0 Data Plus.
P61	USB0-	LS_USB1_DM_OTG	LS_USB1_DM/C3	IO, USB	USB2.0 Port0 Data Minus.
P62	USB0_EN_OC#	GPIO3_14_3V3	GPIO3_14/AC6	IO, 3.3V CMOS 10k PU	SMARC General Purpose Input/output
P63	USB0_VBUS_DET	LS_USB1_VBUS	LS_USB1_VBUS/C1	5V, Power	USB host power detection, when this port is used as a device.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P64	USB0_OTG_ID	USB0_OTG_ID	LS_USB1_ID/E3	I, 3.3V CMOS	USB0 OTG ID.
P65	USB1+	USB_HUB3OUT_DP	NA	IO, USB	USB2.0 Port2 Data Plus. Note: Connected to USB Hub.
P66	USB1-	USB_HUB3OUT_DM	NA	IO, USB	USB2.0 Port2 Data Minus. Note: Connected to USB Hub.
P67	USB1_EN_OC#	USB_HUB3_OC	NA	IO, 3.3V CMOS 10K PU	USB Port2 Over Current Indicator. Note: Connected to USB Hub.
P68	GND	GND	NA	Power	Ground.
P69	USB2+	USB_HUB1OUT_DP	NA	IO, USB	USB2.0 Port0 Data Plus. Note: Connected to USB Hub.
P70	USB2-	USB_HUB1OUT_DM	NA	IO, USB	USB2.0 Port1 Data Minus. Note: Connected to USB Hub.
P71	USB2_EN_OC#	USB_HUB1_OC	NA	IO, 3.3V CMOS 10K PU	USB Port0 Over Current Indicator. Note: Connected to USB Hub.
P72	RSVD4	NC	NA	NA	NA
P73	RSVD5	NC	NA	NA	NA
P74	USB3_EN_OC#	USB_HUB2_OC	NA	IO, 3.3V CMOS 10K PU	USB Port1 Over Current Indicator. Note: Connected to USB Hub.
KEY					
P75	PCIE_A_RST#	GPIO3_05_3V3	GPIO3_05/AA6	IO, 3.3V CMOS	SMARC General Purpose Input/output
P76	USB4_EN_OC#	USB_HUB4_OC	NA	IO, 3.3V CMOS 10K PU	USB Port3 Over Current Indicator. Note: Connected to USB Hub.
P77	PCIE_B_CKREQ#	GPIO2_15_3V3	IFC_PERR_B/C15	IO, 3.3V CMOS 10k PU	NC: (Optionally SMARC General Purpose Input/output.)
P78	PCIE_A_CKREQ#	GPIO2_15_3V3	IFC_PERR_B/C15	IO, 3.3V CMOS 10k PU	NC: (Optionally SMARC General Purpose Input/output.)

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P79	GND	GND	NA	Power	Ground.
P80	PCIE_C_REFCK+	PCIE_C_REFCLK_P	NA	O, PCIe	PCIe Channel-C Clock Positive. Note: From External Oscillator.
P81	PCIE_C_REFCK-	PCIE_C_REFCLK_N	NA	O, PCIe	PCIe Channel-C Clock Negative. Note: From External Oscillator.
P82	GND	GND	NA	Power	Ground.
P83	PCIE_A_REFCK+	PCIE_A_REFCLK_P	NA	O, PCIe	PCIe Channel-A Clock Positive. Note: From External Oscillator.
P84	PCIE_A_REFCK-	PCIE_A_REFCLK_N	NA	O, PCIe	PCIe Channel-A Clock Negative. Note: From External Oscillator.
P85	GND	GND	NA	Power	Ground.
P86	PCIE_A_RX+	LS_SD1_RX0_P	LS_SD1_RX0_P/AC 10	I, PCIe	PCIe Channel-A Receive Positive.
P87	PCIE_A_RX-	LS_SD1_RX0_N	LS_SD1_RX0_P/AB 10	I, PCIe	PCIe Channel-A Receive Negative.
P88	GND	GND	NA	Power	Ground.
P89	PCIE_A_TX+	LS_SD1_TX0_P	LS_SD1_TX0_P/W1 0	O, PCIe 0.1uF AC Couple	PCIe Channel-A Transmit Positive.
P90	PCIE_A_TX-	LS_SD1_TX0_N	LS_SD1_TX0_N/Y10	O, PCIe 0.1uF AC Couple	PCIe Channel-A Transmit Negative.
P91	GND	GND	NA	Power	Ground.
P92	HDMI_D2+ / DP1_LANE0+	USB3_HUB4_RXP	NA	I, USB SS	NC (Note: Optionally USB3.0 Port3 Receive Plus,Connected to USB Hub.)
P93	HDMI_D2- / DP1_LANE0-	USB3_HUB4_RXM	NA	I, USB SS	NC (Note: Optionally USB3.0 Port3 Receive Minus,Connected to USB Hub.)
P94	GND	GND	NA	Power	Ground.
P95	HDMI_D1+ / DP1_LANE1+	USB3_HUB4_TXP	NA	O, USB SS	NC (Note: Optionally USB3.0 Port3 Transmit Plus,Connected to USB Hub.)

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P96	HDMI_D1- / DP1_LANE1-	USB3_HUB4_TXM	NA	O, USB SS	NC (Note: Optionally USB3.0 Port3 Transmit Minus,Connected to USB Hub.)
P97	GND	GND	NA	Power	Ground.
P98	HDMI_D0+ / DP1_LANE2+	USB3_HUB3_RXP	NA	I, USB SS	NC (Note: Optionally USB3.0 Port2 Receive Plus,Connected to USB Hub.)
P99	HDMI_D0- / DP1_LANE2-	USB3_HUB3_RXM	NA	I, USB SS	NC (Note: Optionally USB3.0 Port2 Receive Minus,Connected to USB Hub.)
P100	GND	GND	NA	Power	Ground.
P101	HDMI_CK+ / DP1_LANE3+	USB3_HUB3_TXP	NA	O, USB SS	NC (Note: Optionally USB3.0 Port2 Transmit Plus,Connected to USB Hub.)
P102	HDMI_CK- / DP1_LANE3-	USB3_HUB3_TXM	NA	O, USB SS	NC (Note: Optionally USB3.0 Port2 Transmit Minus,Connected to USB Hub.)
P103	GND	GND	NA	Power	Ground.
P104	HDMI_HPD / DP1_HPD	NC	NA	NA	NA
P105	HDMI_CTRL_CK / DP1_AUX+	NC	NA	NA	NA
P106	HDMI_CTRL_DAT / DP1_AUX-	NC	NA	NA	NA
P107	DP1_AUX_SEL	NC	NA	NA	NA
P108	GPIO0 / CAM0_PWR#	GPIO1_24	GPIO1_24/L2	IO, 1.8V CMOS	SMARC General Purpose Input/output
P109	GPIO1 / CAM1_PWR#	GPIO1_25	GPIO1_25/M2	IO, 1.8V CMOS	SMARC General Purpose Input/output
P110	GPIO2 / CAM0_RST#	GPIO3_08_1V8	GPIO3_08/AA4	IO, 1.8V CMOS	SMARC General Purpose Input/output
P111	GPIO3 / CAM1_RST#	GPIO3_13_1V8	GPIO3_13/AC3	IO, 1.8V CMOS	SMARC General Purpose Input/output
P112	GPIO4 / HDA_RST#	GPIO1_13	ASLEEP/E6	IO, 1.8V CMOS	SMARC General Purpose Input/output

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P113	GPIO5 / PWM_OUT	GPIO2_24	GPIO2_24/D7	IO, 1.8V CMOS	SMARC General Purpose Input/output
P114	GPIO6 / TACHIN	GPIO4_18	GPIO4_18/K4	IO, 1.8V CMOS	SMARC General Purpose Input/output
P115	GPIO7	GPIO3_12_1V8	GPIO3_12/AB6	IO, 1.8V CMOS	SMARC General Purpose Input/output
P116	GPIO8	GPIO4_21	GPIO4_21/M5	IO, 1.8V CMOS	SMARC General Purpose Input/output
P117	GPIO9	GPIO4_22	GPIO4_22/N5	IO, 1.8V CMOS	NC: (Optionally SMARC General Purpose Input/output.)
P118	GPIO10	GPIO2_13	GPIO2_13/D15	IO, 1.8V CMOS	SMARC General Purpose Input/output.(Also is connected to Nor flash Reset B_NOR_RSTn)
P119	GPIO11	GPIO4_20	GPIO4_20/L5	IO, 1.8V CMOS	SMARC General Purpose Input/output
P120	GND	GND	NA	Power	Ground.
P121	I2C_PM_CK	IIC1_SCL	IIC1_SCL/N6	O, 1.8V CMOS/ 1K PU	NC
P122	I2C_PM_DAT	IIC1_SDA	IIC1_SDA/P6	IO, 1.8V CMOS/ 1K PU	NC
P123	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 0 from 4bit DIP Switch (SW5).
P124	BOOT_SEL1#	BOOT_SEL1#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 1 from 4bit DIP Switch (SW5).
P125	BOOT_SEL2#	BOOT_SEL2#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 2 from 4bit DIP Switch (SW5).
P126	RESET_OUT#	RESET_OUT#	GPIO4_19/K5	I, 1.8V CMOS	RESET OUT from CPU
P127	RESET_IN#	RESET_IN#		I, 1.8V CMOS 10K PU	Hard RESET Input to SOM.
P128	POWER_BTN#	ON_OFF_BUTTON	NA	I, 1.8V CMOS	Power ON /OFF Input to SOM. Note:Its connected to PMIC
P129	SER0_TX	UART1_SOUT	UART1_SOUT/N1	O, 1.8V CMOS	UART1 Transmitter.
P130	SER0_RX	UART1_SIN	UART1_SIN/M1	I, 1.8V CMOS	UART1 Receiver.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P131	SER0_RTS#	UART1_RTS_B	UART1_RTS_B/UART3_SOUT/N3	O, 1.8V CMOS	UART1 Request to Send.
P132	SER0_CTS#	UART1_CTS_B	UART1_CTS_B/UART3_SIN/N4	I, 1.8V CMOS	UART1 Clear to Send.
P133	GND	GND	NA	Power	Ground.
P134	SER1_TX	UART4_SOUT	UART2_RTS_B/UART4_SOUT	O, 1.8V CMOS	UART4 Transmitter.
P135	SER1_RX	UART4_SIN	UART2_CTS_B/UART4_SIN	I, 1.8V CMOS	UART4 Receiver.
P136	SER2_TX	UART2_SOUT	UART2_SOUT/P1	O, 1.8V CMOS	UART2 Transmitter.
P137	SER2_RX	UART2_SIN	UART2_SIN/P2	I, 1.8V CMOS	UART2 Receiver.
P138	SER2_RTS#	UART2_RTS_B	UART2_RTS_B/UART4_SOUT	O, 1.8V CMOS	NC (Note: Optionally UART2 Request to Send.)
P139	SER2_CTS#	UART2_CTS_B	UART2_CTS_B/UART4_SIN	I, 1.8V CMOS	NC (Note: Optionally UART2 Clear to Send.)
P140	SER3_TX	UART3_SOUT	UART1_RTS_B/UART3_SOUT/N3	O, 1.8V CMOS	NC (Note: Optionally UART3 Transmitter.)
P141	SER3_RX	UART3_SIN	UART1_CTS_B/UART3_SIN/N4	I, 1.8V CMOS	NC (Note: Optionally UART3 Receiver.)
P142	GND	GND	NA	Power	Ground.
P143	CAN0_TX	CAN1_TX_CON	CAN1_TX/AA5	O, 1.8V CMOS	CAN 1 Transmitter.
P144	CAN0_RX	CAN1_RX_CON	CAN1_RX/AC4	I, 1.8V CMOS	CAN 1 Receiver.
P145	CAN1_TX	CAN2_TX_CON	CAN2_TX/W5	O, 1.8V CMOS	CAN 1 Transmitter.
P146	CAN1_RX	CAN2_RX_CON	CAN2_RX/AB4	I, 1.8V CMOS	CAN 1 Receiver.
P147	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P148	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P149	VDD_IN	VDD_SMARC_IN	NA	0, 5V Power	Supply Voltage
P150	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P151	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P152	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P153	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P154	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P155	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
P156	VDD_IN	VDD_SMARC_IN	NA	O, 5V Power	Supply Voltage
SMARC Secondary Side					
S1	CSI1_TX+ / I2C_CAM1_CK	NC	NA	NA	NA

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S2	CSI1_TX- / I2C_CAM1_DAT	NC	NA	NA	NA
S3	GND	GND	NA	Power	Ground.
S4	RSVD1	NC	NA	NA	NA
S5	CSI0_TX- / I2C_CAM0_CK	NC	NA	NA	NA
S6	CAM_MCK	NC	NA	NA	NA
S7	CSI0_TX+ / I2C_CAM0_DAT	NC	NA	NA	NA
S8	CSI0_CK+	NC	NA	NA	NA
S9	CSI0_CK-	NC	NA	NA	NA
S10	GND	GND	NA	Power	Ground.
S11	CSI0_RX0+	NC	NA	NA	NA
S12	CSI0_RX0-	NC	NA	NA	NA
S13	GND	GND	NA	Power	Ground.
S14	CSI0_RX1+	NC	NA	NA	NA
S15	CSI0_RX1-	NC	NA	NA	NA
S16	GND	GND	NA	Power	Ground.
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 positive.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 negative.
S19	GBE1_LINK100#	GBE1_LINK100#	NA	O, 3.3V CMOS	Second 100Mbps Ethernet link status LED. Note: Connect to Cathode of LED.
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 positive.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 negative.
S22	GBE1_LINK1000#	GBE1_LINK1000#	NA	O, 3.3V CMOS	Second Gigabit Ethernet link status LED. Note: Connect to Cathode of LED.
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 positive.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 negative.
S25	GND	GND	NA	NA	Power
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 positive.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 negative.
S28	GBE1_CTREF	VCC_2V5_ETH	NA	Power	Power for the Centre Tap of Mack Jack connector.
S29	PCIE_D_TX+ / SERDES_0_TX+	LS_SD1_TX3_P	LS_SD1_TX3_P/W14	O, PCIe 0.1uF AC Couple	PCIe Channel-D Transmit Positive.
S30	PCIE_D_TX- / SERDES_0_TX-	LS_SD1_TX3_N	LS_SD1_TX3_N/Y14	O, PCIe 0.1uF AC Couple	PCIe Channel-D Transmit Negative.
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	NA	O, 3.3V CMOS	Second Gigabit Ethernet activity status Note: Connect to Cathode of LED.
S32	PCIE_D_RX+ / SERDES_0_RX+	LS_SD1_RX3_P	LS_SD1_RX3_P/AC14	I, PCIe	PCIe Channel-D Receive Positive.
S33	PCIE_D_RX- / SERDES_0_RX-	LS_SD1_RX3_N	LS_SD1_RX3_N/AB14	I, PCIe	PCIe Channel-D Receive Negative.
S34	GND	GND	NA	Power	Ground.
S35	USB4+	USB_HUB4OUT_DP	NA	IO, USB	USB2.0 Port3 Data Plus. Note: Connected to USB Hub.
S36	USB4-	USB_HUB4OUT_DM	NA	IO, USB	USB2.0 Port3 Data Minus. Note: Connected to USB Hub.
S37	USB3_VBUS_DET	LS_USB1_VBUS	LS_USB1_VBUS/C1	5V, Power	USB host power detection, when this port is used as a device.
S38	AUDIO_MCK	EXT_AUDIO_MCLK1	EXT_AUDIO_MCLK1/H5	O, 1.8V CMOS	Master Clock for Audio codec
S39	I2S0_LRCK	SAI3_TX_SYNC	SAI3_TX_SYNC/J5	O, 1.8V CMOS	Serial Audio Interface Channel3 Frame Sync /Left Right Clock
S40	I2S0_SDOUT	SAI3_TX_DATA	SAI3_TX_DATA/J4	O, 1.8V CMOS	Serial Audio Interface Channel3 Data Output
S41	I2S0_SDIN	SAI3_RX_DATA	SAI3_RX_DATA/H3	I, 1.8V CMOS	Serial Audio Interface Channel3 Data Input
S42	I2S0_CK	SAI3_TX_BCLK	SAI3_TX_BCLK/J3	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel3 Clock
S43	ESPI_ALERT0#	NC	NA	NA	NA
S44	ESPI_ALERT1#	NC	NA	NA	NA
S45	MDIO_CLK	SMARC_EMI1_MDC	LS_EMI1_MDC/AB2	I, 1.8V CMOS	Management Interface Clock

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S46	MDIO_DAT	SMARC_EMI1_MDIO	LS_EMI1_MDIO/AB3	IO, 1.8V CMOS	Management Interface Data
S47	GND	GND	NA	Power	Ground.
S48	I2C_GP_CK	IIC2_SCL	IIC2_SCL/K1	O, 1.8V CMOS/ 1K PU	I2C CLK
S49	I2C_GP_DAT	IIC2_SDA	IIC2_SDA/L1	IO, 1.8V CMOS/ 1K PU	I2C Data
S50	HDA_SYNC / I2S2_LRCK	SAI4_TX_SYNC	SAI4_TX_SYNC/M4	O, 1.8V CMOS	Serial Audio Interface Channel4 Frame Sync /Left Right Clock
S51	HDA_SDO / I2S2_SDOUT	SAI4_TX_DATA	SAI4_TX_DATA/M3	O, 1.8V CMOS	Serial Audio Interface Channel4 Data Output
S52	HDA_SDI / I2S2_SDIN	SAI4_RX_DATA	SAI4_RX_DATA/K3	I, 1.8V CMOS	Serial Audio Interface Channel4 Data Input
S53	HDA_CK / I2S2_CK	SAI4_TX_BCLK	SAI4_TX_BCLK/L3	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel4 Clock
S54	SATA_ACT#	GPIO2_27_3V3	GPIO2_27/D13	IO, 3.3V CMOS 10k PU	SMARC General Purpose Input/output
S55	USB5_EN_OC#	NC	NA	NA	NA
S56	QSPI_IO_2 / ESPI_IO_2	QSPI_DIO_A2	IFC_ADD24/QSPI_DIO_A2/C12	IO,1V8 CMOS	NC (Note: Optionally QSPI1A DATA lane 2)
S57	QSPI_IO_3 / ESPI_IO_3	QSPI_DIO_A3	IFC_ADD25/QSPI_DIO_A3/D12	IO,1V8 CMOS	NC (Note: Optionally QSPI1A DATA lane 3)
S58	ESPI_RESET#	NC	NA	NA	NA
S59	USB5+	NC	NA	NA	NA
S60	USB5-	NC	NA	NA	NA
S61	GND	GND	NA	Power	Ground.
S62	USB3_SSTX+	USB3_HUB2_TXP	NA	O, USB SS	NC (Note: Optionally USB3.0 Port1 Transmit Plus,Connected to USB Hub.)
S63	USB3_SSTX-	USB3_HUB2_TXM	NA	O, USB SS	NC (Note: Optionally USB3.0 Port1 Transmit Minus,Connected to USB Hub.)

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S64	GND	GND	NA	Power	Ground.
S65	USB3_SSRX+	USB3_HUB2_RXP	NA	I, USB SS	NC (Note: Optionally USB3.0 Port1 Receive Plus,Connected to USB Hub.)
S66	USB3_SSRX-	USB3_HUB2_RXM	NA	I, USB SS	NC (Note: Optionally USB3.0 Port1 Receive Minus,Connected to USB Hub.)
S67	GND	GND	NA	Power	Ground.
S68	USB3+	USB_HUB2OUT_DP	NA	IO, USB	USB2.0 Port1 Data Plus. Note: Connected to USB Hub.
S69	USB3-	USB_HUB2OUT_DM	NA	IO, USB	USB2.0 Port1 Data Minus. Note: Connected to USB Hub.
S70	GND	GND	NA	Power	Ground.
S71	USB2_SSTX+	USB3_HUB1_TXP	NA	O, USB SS	NC (Note: Optionally USB3.0 Port0 Transmit Plus,Connected to USB Hub.)
S72	USB2_SSTX-	USB3_HUB1_TXM	NA	O, USB SS	NC (Note: Optionally USB3.0 Port0 Transmit Minus,Connected to USB Hub.)
S73	GND	GND	NA	Power	Ground.
S74	USB2_SSRX+	USB3_HUB1_RXP	NA	I, USB SS	NC (Note: Optionally USB3.0 Port0 Receive Plus,Connected to USB Hub.)
S75	USB2_SSRX-	USB3_HUB1_RXM	NA	I, USB SS	NC (Note: Optionally USB3.0 Port0 Receive Minus,Connected to USB Hub.)
KEY					
S76	PCIE_B_RST#	USB3_HUB1_RXP	NA	I, USB SS	NC (Note: Optionally USB3.0 Port0 Receive Plus,Connected to USB Hub.)
S77	PCIE_C_RST#	GPIO2_15_3V3	IFC_PERR_B/C15	IO, 3.3V CMOS 10k PU	SMARC General Purpose Input/output
S78	PCIE_C_RX+ / SERDES_1_RX+	LS_SD1_RX2_P	LS_SD1_RX2_P/AC13	I, PCIe	PCIe Channel-C Receive Positive.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S79	PCIE_C_RX- / SERDES_1_RX-	LS_SD1_RX2_N	LS_SD1_RX2_N/AB13	I, PCIe	PCIe Channel-C Receive Negative.
S80	GND	GND	NA	Power	Ground.
S81	PCIE_C_TX+ / SERDES_1_TX+	LS_SD1_TX2_P	LS_SD1_TX2_P/W13	O, PCIe 0.1uF AC Couple	PCIe Channel-C Transmit Positive.
S82	PCIE_C_TX- / SERDES_1_TX-	LS_SD1_TX2_N	LS_SD1_TX2_N/Y13	O, PCIe 0.1uF AC Couple	PCIe Channel-C Transmit Negative.
S83	GND	GND	NA	Power	Ground.
S84	PCIE_B_REFCK+	PCIE_B_REFCLK_P	NA	O, PCIe	PCIe Channel-B Clock Positive. Note: From External Oscillator.
S85	PCIE_B_REFCK-	PCIE_B_REFCLK_N	NA	O, PCIe	PCIe Channel-B Clock Negative. Note: From External Oscillator.
S86	GND	GND	NA	Power	Ground.
S87	PCIE_B_RX+	LS_SD1_RX1_P	LS_SD1_RX1_P/AC11	I, PCIe	PCIe Channel-B Receive Positive.
S88	PCIE_B_RX-	LS_SD1_RX1_N	LS_SD1_RX1_N/AB11	I, PCIe	PCIe Channel-B Receive Negative.
S89	GND	GND	NA	Power	Ground.
S90	PCIE_B_TX+	LS_SD1_TX1_P	LS_SD1_TX1_P/W11	O, PCIe 0.1uF AC Couple	PCIe Channel-B Transmit Positive.
S91	PCIE_B_TX-	LS_SD1_TX1_N	LS_SD1_TX1_N/Y11	O, PCIe 0.1uF AC Couple	PCIe Channel-B Transmit Negative.
S92	GND	GND	NA	Power	Ground.
S93	DP0_LANE0+	NC	NA	NA	NA
S94	DP0_LANE0-	NC	NA	NA	NA
S95	DP0_AUX_SEL	NC	NA	NA	NA
S96	DP0_LANE1+	NC	NA	NA	NA
S97	DP0_LANE1-	NC	NA	NA	NA
S98	DP0_HPD	NC	NA	NA	NA
S99	DP0_LANE2+	NC	NA	NA	NA
S100	DP0_LANE2-	NC	NA	NA	NA
S101	GND	GND	NA	Power	Ground.
S102	DP0_LANE3+	NC	NA	NA	NA

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S103	DP0_LANE3-	NC	NA	NA	NA
S104	USB3_OTG_ID	USB_OTG_ID	LS_USB1_ID/E3	I, 3.3V CMOS	USB0 OTG ID.
S105	DP0_AUX+	NC	NA	NA	NA
S106	DP0_AUX-	NC	NA	NA	NA
S107	LCD1_BKLT_EN	NC	NA	NA	NA
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	NC	NA	NA	NA
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	NC	NA	NA	NA
S110	GND	GND	NA	Power	Ground.
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	CLK0_25MHz	NA	I, DIFF	NC (Note: 25MHz clock)
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	CLK1_25MHz	NA	I, DIFF	NC (Note: 25MHz clock)
S113	eDP1_HPD / DSI1_TE	CLK0_2.048MHz	NA	IO, 1.8V CMOS	NC (Note: 2.048MHz clock)
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	CLK1_2.048MHz	NA	I, DIFF	NC (Note: 2.048MHz clock)
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	NC	NA	NA	NA
S116	LCD1_VDD_EN	NC	NA	NA	NA
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	NC	NA	NA	NA
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	NC	NA	NA	NA
S119	GND	GND	NA	Power	Ground.
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	NC	NA	NA	NA
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	NC	NA	NA	NA
S122	LCD1_BKLT_PWM	NC	NA	NA	NA

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S123	GPIO13	NC	NA	NA	NA
S124	GND	GND	NA	Power	Ground.
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	NC	NA	NA	NA
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	NC	NA	NA	NA
S127	LCD0_BKLT_EN	NC	NA	NA	NA
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	NC	NA	NA	NA
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	NC	NA	NA	NA
S130	GND	GND	NA	Power	Ground.
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	NC	NA	NA	NA
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	NC	NA	NA	NA
S133	LCD0_VDD_EN	NC	NA	NA	NA
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	NC	NA	NA	NA
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	NC	NA	NA	NA
S136	GND	GND	NA	Power	Ground.
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	NC	NA	NA	NA
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	NC	NA	NA	NA
S139	I2C_LCD_CK	NC	NA	NA	NA

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S140	I2C_LCD_DAT	NC	NA	NA	NA
S141	LCD0_BKLT_PWM	NC	NA	NA	NA
S142	GPIO12	NC	NA	NA	NA
S143	GND	GND	NA	Power	Ground.
S144	eDP0_HPD / DSI0_TE	NC	NA	NA	NA
S145	WDT_TIME_OUT#	RESET_REQb	RESET_REQ_B / G5	I, 1.8V CMOS	RESET OUT from CPU
S146	PCIE_WAKE#	GPIO3_04_3V3	GPIO3_04/Y6	IO, 3.3V CMOS 10k PU	SMARC General Purpose Input/output
S147	VDD_RTC	VDD_RTC	NA	O, 3V Power	RTC backup power. Connected to RTC battery holder.
S148	LID#	NC	NA	-	NC.
S149	SLEEP#	NC	NA	-	NC.
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	O, 5V CMOS 10K PU	Power bad indication from Carrier board. Module and Carrier power supplies shall not be enabled while this signal is held low by the Carrier.
S151	CHARGING#	NC	NA	-	NC.
S152	CHARGER_PRSNT#	NC	NA	-	NC.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	I, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_STBY# goes High.
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	I, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_PWR_ON is High
S155	FORCE_RECOV#	FORCE_RECOV#	NA	O, 1.8V CMOS 10K PU	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked.
S156	BATLOW#	NC	NA	-	NC.

Pin No.	SMARC Edge Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S157	TEST#	TEST_MODE_SELECT	TEST_MODE_SELECT/BC49	O, 1.8V CMOS 2.2K PD	Only for Module vendor specific use. Connected to 4bit DIP switch (SW6).
S158	GND	GND	NA	Power	Ground.

2.4 Serial Interface Features

2.4.1 Debug UART Interface

The Layerscape LS1021A SMARC development board supports debug interface through Layerscape LS1021A CPU's UART3 interface. This UART3 signals from SMARC MXM connector is connected to UART to USB Convertor "FT232RQ" via 1.8V to 3.3V level Translator and FT232RQ is connected to USB Micro AB Connector (J24). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

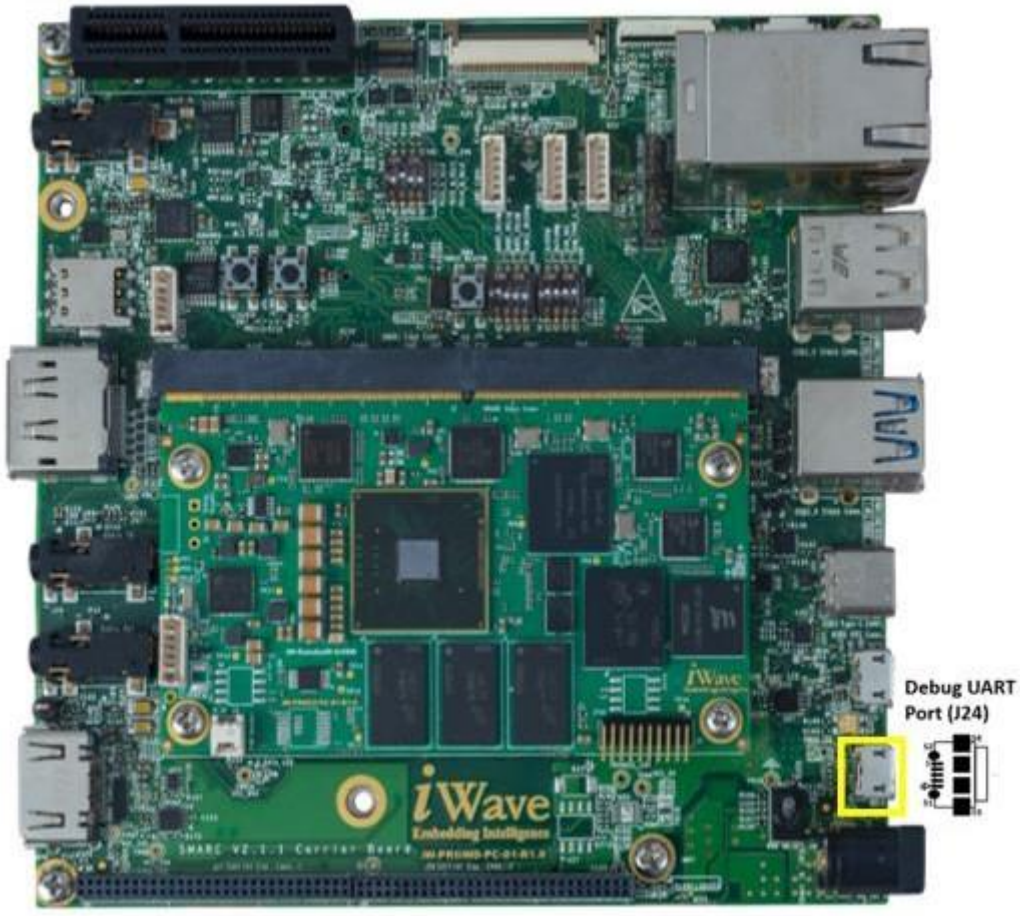


Figure 3: Debug UART Port

2.4.2 Data UART Interface

The Layerscape LS1021A SMARC carrier board supports full functional Data UART interface through Layerscape LS1021A CPU's UART1 interface. This UART1 signals from SMARC MXM connector is connected to 6pin Header (J12) via 1.8 to 3.3V volatge level translator for easy accessibilty. This Data UART header is physically located at the top of the board as shown below.

Number of Pins 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

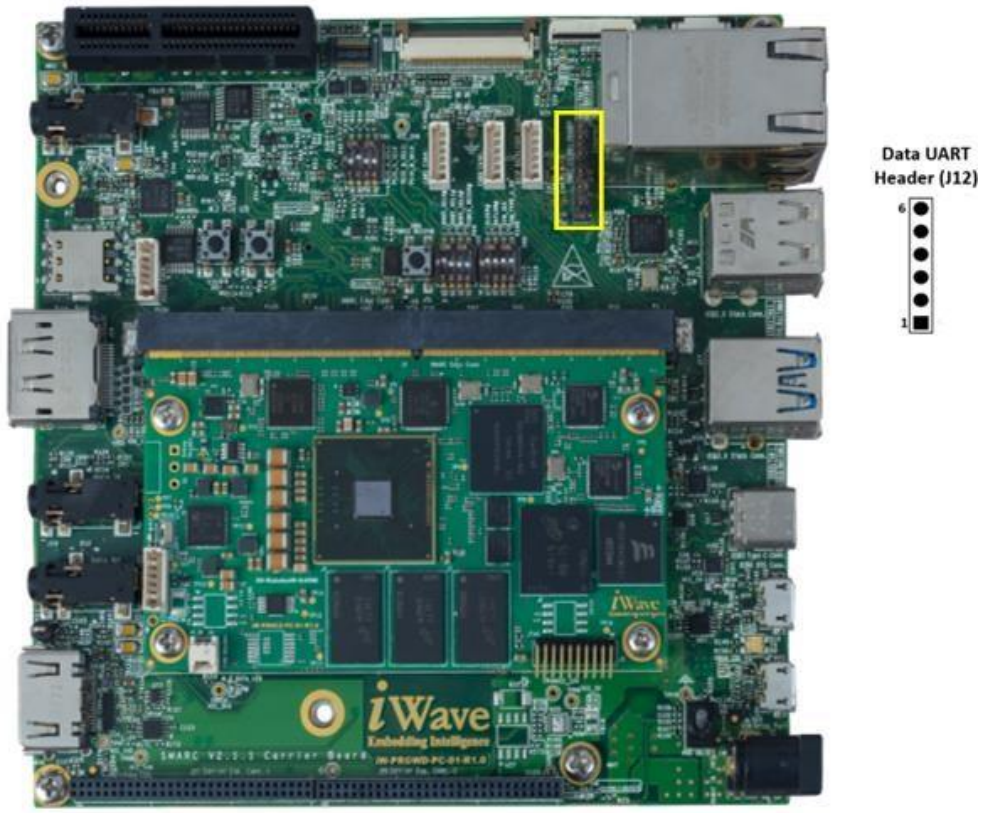


Figure 4: Data UART Header

Table 4: Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_RTS#	UART1_RTS_B	I, 3.3V CMOS	UART1 interface Ready to Send signal.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART_RXD	UART1_RX	I, 3.3V CMOS	UART1 interface Receive signal.
5	UART_TXD	UART1_TX	O, 3.3V CMOS	UART1 interface Transmit signal.
6	UART_CTS#	UART1_CTS_B	O, 3.3V CMOS	UART1 interface Clear to Send signal.

2.4.3 RS232 UART Interface (Optional)

The Layerscape LS1021A SMARC carrier board optionally supports full functional RS232 UART interface through i.MX8 CPU's UART1 interface. This UART1 signals from SMARC MXM connector Connected UART to RS232 Convertor "MAX3232EIPWR" via 1.8V to 3.3V level Translator and MAX3232EIPWR is connected to 6pin Header (J15). This Data RS232 UART header is physically located at the top of the board as shown below.

Number of Pins 6

Connector Part number : 53047-0610 from Molex

Mating Connector Hosuing : 0510210600 from Molex

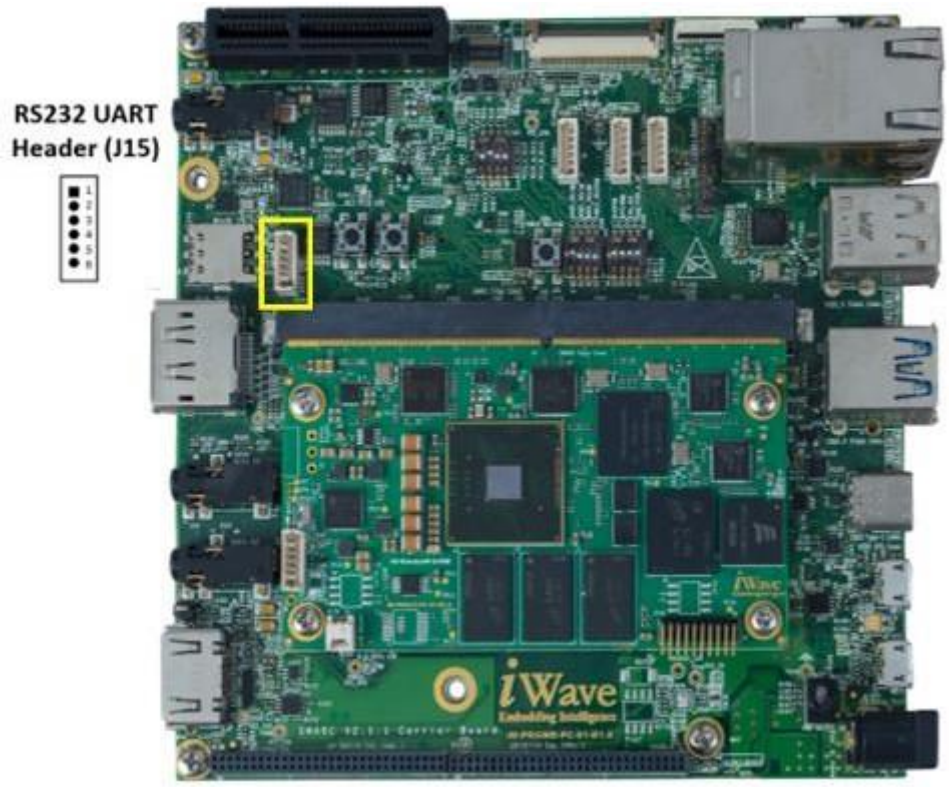


Figure 5: RS232 UART Header

2.5 High Speed Interface Features

2.5.1 PCIe Interface

The Layerscape LS1021A SMARC Development platform by default supports four PCIe Lanes PCIe_A, PCIe_B, PCIe_C and PCIe_D. PCIe_A, PCIe_B, PCIe_C and PCIe_D lane supported through Layerscape LS1021A CPU's Serdes1 Interface.

Both PCIe A & B signals of SMARC MXM connector are connected to separate 1:3 Multiplexer/Demultiplexer switch and the output of both the Multiplexer/Demultiplexer switch are connected to PCIex4 connector and M.2 connector. The PCIe C & D signals of SMARC MXM connector are connected to PCIex4 connector. The selection between the connector can be done by setting the 4th bit of Board configuration switch (SW1) to appropriate position. PCIe A reference clock from SMARC MXM connector is connected to 1:2 output clock buffer and then connected to PCIex4 connector and PCIe M.2 connector for clock reference. Whereas PCIe B reference clock is Optionally connected to PCIe M.2 Connector.

Refer Dip Switch (SW1) Settings in "Table 14: Board Configuration Switch" for more details on selecting PCIe connector.

PCIex4 Connector: PCIeX4 connector (J5) is physically located at the top of the board as shown below

Figure 6: PCIex4 Connector

Table 5: PCIex4 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSNT1#	PRSNT1#	O, 3.3V CMOS	Default Grounded.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A4	GND	GND	Power	Ground.
B4	GND	GND	Power	Ground.
A5	TCK	NC	-	NC.
B5	SMCLK	II2C1_SCL	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.
B6	SMDAT	II2C1_SDA	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND	GND	Power	Ground.
A8	TMS	NC	-	NC.
B8	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
A9	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VAUX_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	GPIO3_05_3V3	O, 3.3V CMOS	PCIe PERST#.
B11	WAKE#	GPIO3_04_3V3	O, 3.3V CMOS	PCIe WAKE#.
A12	GND	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	PCIe0_CLK+	PCIE_A_REFCLK_P	O, PCIe	PCIe Clock positive.
B13	GND	GND	Power	Ground.
A14	PCIe0_CLK-	PCIE_A_REFCLK_N	O, PCIe	PCIe Clock negative.
B14	PCIE0_TX+	LS_SD_TX0_P	O, PCIe	PCIe Port 0 Transmit pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE0_TX.*
A15	GND	GND	Power	Ground.
B15	PCIE0_TX-	LS_SD_TX0_P	O, PCIe	PCIe Port 0 Transmit pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE0_TX.*
A16	PCIE0_RX+	LS_SD_RX0_P	I, PCIe	PCIe Port 0 Receive pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE0_RX.*
B16	GND	GND	Power	Ground.
A17	PCIE0_RX-	LS_SD_RX0_P	I, PCIe	PCIe Port 0 Receive pair negative.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Note: Refer SW1 setting from table to support PCIE0_RX.
B17	PRSNT2#	NC	-	NC.
A18	GND	GND	Power	Ground.
B18	GND	GND	Power	Ground.
A19	RSVD	NC	-	NC, Reserved Pin.
B19	PCIE1_TX+	LS_SD1_TX1_P	O, PCIe	PCIe Port 1 Transmit pair positive. *Note: Refer SW1 setting from Table 10 for support PCIE1_TX.*
A20	GND	GND	Power	Ground.
B20	PCIE1_TX-	LS_SD1_TX1_N	O, PCIe	PCIe Port 1 Transmit pair negative. *Note: Refer SW1 setting from Table 10 for support PCIE1_TX.*
A21	PCIE1_RX+	LS_SD1_RX1_P	I, PCIe	PCIe Port 1 Receive pair positive. *Note: Refer SW1 setting from Table 10 for support PCIE1_RX.*
B21	GND	GND	Power	Ground.
A22	PCIE1_RX-	LS_SD1_RX1_N	I, PCIe	PCIe Port 1 Receive pair negative. *Note: Refer SW1 setting from Table 10 for support PCIE1_RX.*
B22	GND	GND	Power	Ground.
A23	GND	GND	Power	Ground.
B23	PCIE2_TX+	LS_SD1_TX2_P	-	PCIe Port 2 Transmit pair positive. *Note: Refer SW1 setting from Table 10 for support PCIE2_TX.*
A24	GND	GND	Power	Ground.
B24	PCIE2_TX-	LS_SD1_TX2_N	-	PCIe Port 2 Transmit pair negative. *Note: Refer SW1 setting from Table 10 for support PCIE2_TX.*
A25	PCIE2_RX+	LS_SD1_RX2_P	-	PCIe Port 1 Receive pair positive. *Note: Refer SW1 setting from Table 10 for support PCIE2_RX.*
B25	GND	GND	Power	Ground.
A26	PCIE2_RX-	LS_SD1_RX2_N	-	PCIe Port 1 Receive pair negative. *Note: Refer SW1 setting from Table 10 for support PCIE2_RX.*
B26	GND	GND	Power	Ground.
A27	GND	GND	Power	Ground.
B27	PCIE3_TX+	LS_SD1_TX3_P	-	PCIe Port 3 Transmit pair positive.
A28	GND	GND	Power	Ground.
B28	PCIE3_TX-	LS_SD1_TX3_N	-	PCIe Port 3 Transmit pair negative.
A29	PCIE3_RX+	LS_SD1_RX3_P	-	PCIe Port 3 Receive pair positive.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
B29	GND	GND	Power	Ground.
A30	PCIE3_RX-	LS_SD1_RX3_N	-	PCIe Port 3 Receive pair negative.
B30	RSVD	NC	-	NC, Reserved Pin.
A31	GND	GND	Power	Ground.
B31	PRSNT3#	NC	-	NC.
A32	RSVD	NC	-	NC, Reserved Pin.
B32	GND	GND	Power	Ground.

PCIe M.2 Connector: The Layerscape LS1021A SMARC carrier board supports M.2 Key-B Connector (J32) and is placed at the bottom side of the board.+

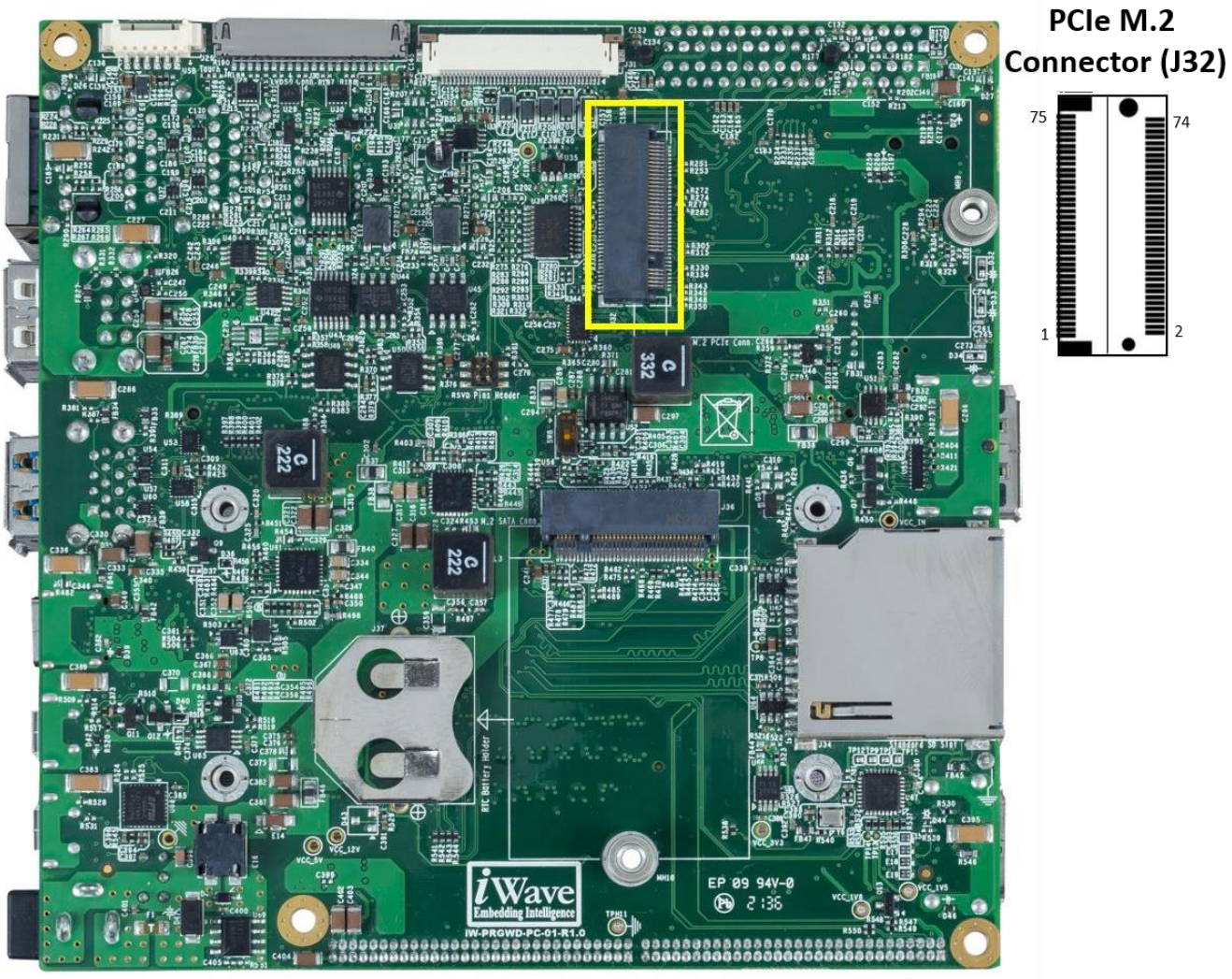


Figure 7: M.2 Connector

Refer below table for M.2 connector pinout details.

Table 6: M.2 PCIe Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB5+	IO, USB	USB2.0 Port5 Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	GPIO2_13	O, 3.3V CMOS 10K PU	M.2 Wireless Disable Signal
9	USB_D-	USB5-	IO, USB	USB2.0 Port5 Data Minus.
10	GPIO9(LED1#/DAS_DSS#)(I/0)(0/3.3V)	GPIO2_27_3V3	O, 3.3V CMOS	Provide status indicators via LED. *Note: GPIO2_27 Connected Optionally.*
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	SAI4_TX_BCLK	IO, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel1 Clock
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	SAI4_RX_DATA	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	NC	NC	NC.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	SAI4_TX_DATA	O, 1.8V CMOS	Serial Audio Interface Channel1 Data Output
25	DPR (O) (0/1.8V)	NC	NC	NC.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NC	NC.
27	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	SAI4_TX_SYNC	IO, 1.8V CMOS	Serial Audio Interface Channel1 Left Right Clock
29	PERN1/USB30_RX-/SSIC_RX-	LS_SD1_RX0_N	O, PCIe	PCIe Channel-A/B Receive Negative. *Note: To select PCIe Chanel Refer Table 10*
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	LS_SD1_RX0_P	O, PCIe	PCIe Channel-A/B Receive Positive. *Note: To select PCIe Chanel Refer Table 10*
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	LS_SD1_TX0_N	I, PCIe	PCIe Channel-A/B Transmit Negative. *Note: To select PCIe Chanel Refer Table 10*
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	LS_SD1_TX0_P	I, PCIe	PCIe Channel-A/B Transmit Positive. *Note: To select PCIe Chanel Refer Table 10*
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	IIC2_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	LS_SD1_RX0_N	O, PCIe	PCIe Channel-A/B Receive Negative. *Note: To select PCIe Chanel Refer Table 10*
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	IIC2_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	LS_SD1_RX0_P	O, PCIe	PCIe Channel-A/B Receive Positive. *Note: To select PCIe Chanel Refer Table 10*
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	NC	NA	NC.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2)(I/O)(0/1.8V)	NC	NA	NC.
47	PETN0/SATA_A-	LS_SD1_TX0_N	I, PCIe	PCIe Channel-A/B Transmit Negative. *Note: To select PCIe Chanel Refer Table 10*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NA	NC.
49	PETP0/SATA_A+	LS_SD1_TX0_P	I, PCIe	PCIe Channel-A/B Transmit Positive. *Note: To select PCIe Chanel Refer Table 10*
50	PERST# (O)(0/3.3V)	GPIO3_05_3V3	O, 3.3V CMOS 10K PU	PCIe Resets Signal.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	GPIO2_15_3V3	IO, 3.3V CMOS 10K PU	M.2 Clock Request Signal.
53	REFCLKN	PCIE_A_REFCLK_N	O,PCIe	PCIe Channel Clock Positive.
54	PEWAKE# (I/O)(0/3.3V)	GPIO3_04	O, 3.3V CMOS 10K PU	PCIe Wake Signal
55	REFCLKP	PCIE_A_REFCLK_P	O,PCIe	PCIe Channel Clock Negative.
56	MFG_DATA	NC	NA	NC.
57	GND	GND	Power	Ground.
58	MFG_CLOCK	NC	NA	NC.
59	ANTCTL0 (I)(0/1.8 V)	NC	NA	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NA	NC.
61	ANTCTL1 (I)(0/1.8 V)	NC	NA	NC.
62	COEX_TXD (O)(0/1.8V)	UART4_SOUT	I, 1.8V CMOS	NC. *Note: UART3_TX Connected Optionally*
63	ANTCTL2 (I)(0/1.8 V)	NC	NA	NC.
64	COEX_RXD (I)(0/1.8V)	UART4_SIN	O, 1.8V CMOS	NC. *Note: UART3_RX Connected Optionally*
65	ANTCTL3 (I)(0/1.8 V)	NC	NA	NC.
66	SIM_DETECT (I)	NC	NA	NC
67	RESET# (O)(0/1.8V)	GPIO2_24	I, 1.8V CMOS 10K PU	M.2 Reset Signal. *Note: GPIO0_19 Connected Optionally.*
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 3.3V CMOS 33E Series	M.2 Clock *Note: Optionally connected 32.768kHz Clock Oscillator.*
69	CONFIG_1	M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 1.8V CMOS	M.2 Configuration Pin 2.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
			10K PU	

2.5.2 SATA M.2 Interface (Optional)

The Layerscape LS1021A SMARC SMARC carrier board supports SATA interface from SERDES1 of Layerscape LS1021A processor using M.2 SATA connector (J36). The SMARC carrier board also supports SATA activity LED (D21) on Top side of the board for SATA activity indication. This M.2 SATA connector is physically located at the bottom of the board.

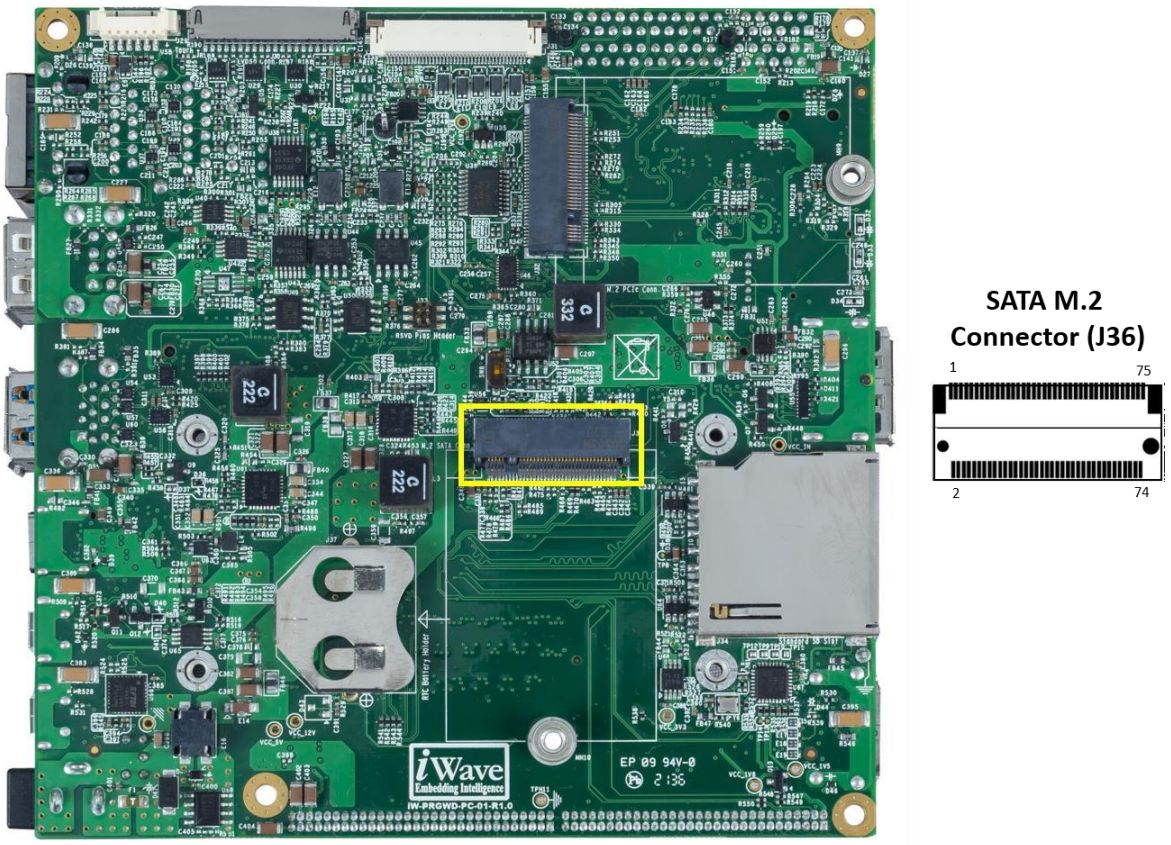


Figure 8: SATA Connector

Refer below table for the pinout is listed of SATA connector.

Table 7: SATA M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_CONFIG_3	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB_HUB3OUT_DP	IO, USB	USB2.0 Data Plus.
8	W_DISABLE1# (O)(0/3.3V)	GPIO2_13	O, 3.3V CMOS 10K PU	M.2 Wireless Disable Signal *Note: GPIO1_04 Connected Optionally.*
9	USB_D-	USB_HUB3OUT_DM	IO, USB	USB2.0 Data Minus.
10	GPIO9(LED1#/DAS_DSS#)(I/0)(0/3.3V)	GPIO2_27_3V3	O, 3.3V CMOS	Provide status indicators via LED.
11	GND	GND	Power	Ground.
12	B1	NC	NA	NC.
13	B2	NC	NA	NC.
14	B3	NC	NA	NC.
15	B4	NC	NA	NC.
16	B5	NC	NA	NC.
17	B6	NC	NA	NC.
18	B7	NC	NA	NC.
19	B8	NC	NA	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	NC	NA	NC.
21	CONFIG_0	M.2_CONFIG_0	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	NC	NA	NC.
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	NC	NA	NC.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	NC	NA	NC.
25	DPR (O) (0/1.8V)	NC	NA	NC.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NA	10K PU Mounted
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NA	NC.
29	PERN1/USB30_RX-/SSIC_RX-	NC	NA	NC.
30	UIM-RESET (I)	M2_UIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NA	NC.
32	UIM-CLK (I)	M2_UIM_CLK	I, SIM	SIM Card Clock Signal.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	M2_UIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NA	NC.
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NA	NC.
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	IIC2_SCL	O, 1.8V CMOS	I2C CLK.
41	PERN0/SATA_B+	LS_SD1_RX0_N	O, SATA	SATA Channel Receive Negative.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	IIC2_SDA	IO, 1.8V CMOS	I2C Data.
43	PERP0/SATA_B-	LS_SD1_RX0_P	O, SATA	SATA Channel Receive Positive.
44	GPIO2_(ALERT#/GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	GPIO_SMBUS_ALERT(GPIO0_16)	IO, 1.8V CMOS 10K PU	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/UIM_RST2) (I/O)(0/1.8V)	NC	NA	NC.
47	PETN0/SATA_A-	LS_SD1_TX0_N	I, SATA	SATA Channel Transmit Negative.
48	GPIO4(TX_BLK/GNSS_1/UIM_PWR2)(I/O)(0/1.8V)	NC	NA	NC.
49	PETP0/SATA_A+	LS_SD1_TX0_P	I, SATA	SATA Channel Transmit Positive.
50	PERST# (O)(0/3.3V)	NC	NA	NC.
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	NC	NA	NC.
53	REFCLKN	NC	NA	NC.
54	PEWAKE# (I/O)(0/3.3V)	NC	NA	NC.
55	REFCLKP	NC	NA	NC.
56	MFG_DATA	NC	NA	NC.
57	GND	GND	Power	Ground.
58	MFG_CLOCK	NC	NA	NC.
59	ANTCTL0 (I)(0/1.8 V)	NC	NA	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NA	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
61	ANTCTL1 (I)(0/1.8 V)	NC	NA	NC.
62	COEX_TXD (O)(0/1.8V)	UART4_SOUT	I, 1.8V CMOS	NC. *Note: UART4_SOUTConnected Optionally*
63	ANTCTL2 (I)(0/1.8 V)	NC	NA	NC.
64	COEX_RXD (I)(0/1.8V)	UART4_SIN	O, 1.8V CMOS	NC. *Note: UART4_SIN Connected Optionally*
65	ANTCTL3 (I)(0/1.8 V)	NC	NA	NC.
66	SIM_DETECT (I)	NC	NA	NC.
67	RESET# (O)(0/1.8V)	GPIO2_24	I, 1.8V CMOS 10K PU	M.2 Reset Signal.
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 3.3V CMOS 33E Series	M.2 Clock *Note: Optionally connected 32.768kHz Clock Oscillator.*
69	CONFIG_1	M.2_CONFIG_1	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_CONFIG_2	I, 1.8V CMOS 10K PU	M.2 Configuration Pin 2.

2.5.3 USB3.0 Host Interface

The Layerscape LS1021A SMARC development board supports Super Speed USB3.0 Host interface through on SOM USB3.0 Hub. This USB3.0 signals of SMARC USB2 and USB3 port from MXM connector is directly connected to bottom and top port of dual stack USB3.0 Type-A connector (J17) respectively. Also, USB2.0 signals of USB2 and USB3 Port of SMARC signals are connected to respective connector from 3.0 USB Hub used on SOM. The top port of J17 connector is shared with USB Type-C connector (J20).

The selection between USB Type C connector and top port of dual stack USB3.0 TypeA connector can be done by setting the 4th bit of Board configuration switch (SW6) to appropriate position. If the 4th bit of Board configuration switch (SW6) is set to OFF position, then USB3 port of SMARC MXM connector is connected to USB Type C connector. If the 4th bit of Board configuration switch (SW6) is set to ON position, then USB3 port of SMARC MXM connector is connected to top port of dual stack USB3.0 TypeA connector. Also, USB2.0 signals of USB3 Port of SMARC MXM connector is connected to both these connectors.

To support double-way plug in on USB TypeC connector, USB3 signals are connected to FUSB340TMX USB3.0 switch and then connected to USB Type C connector. This USB3.0 switch port connection to Type C connector top or bottom is controlled through GPIO4 (P112nd pin) of the SMARC MXM connector.

The VBUS power of this USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of SMARC MXM connector USB2 and USB3 ports. This USB3.0 connector is physically located at the top of the board as shown below.

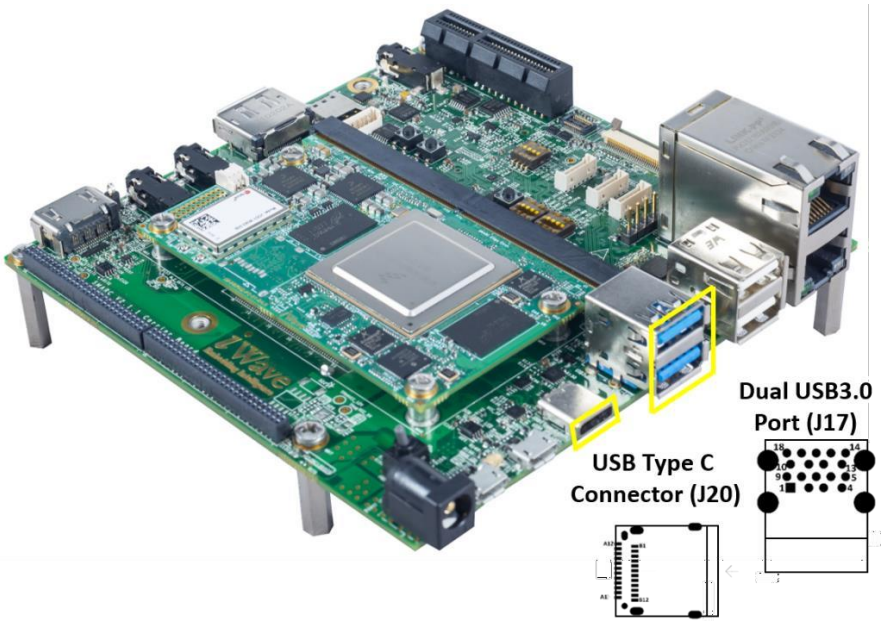


Figure 9: USB3.0 Host

2.6 Communication Interface Features

2.6.1 Gigabit Ethernet Interface

The Layerscape LS1021A SMARC development board supports Dual Ethernet Port interface through on SOM Ethernet PHY which supports 10/100/1000Mbps Ethernet. The Ethernet PHY output signals from SMARC MXM connector GBE0 and GBE1 are directly connected to RJ45 Magjack (J8), Bottom & Top connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

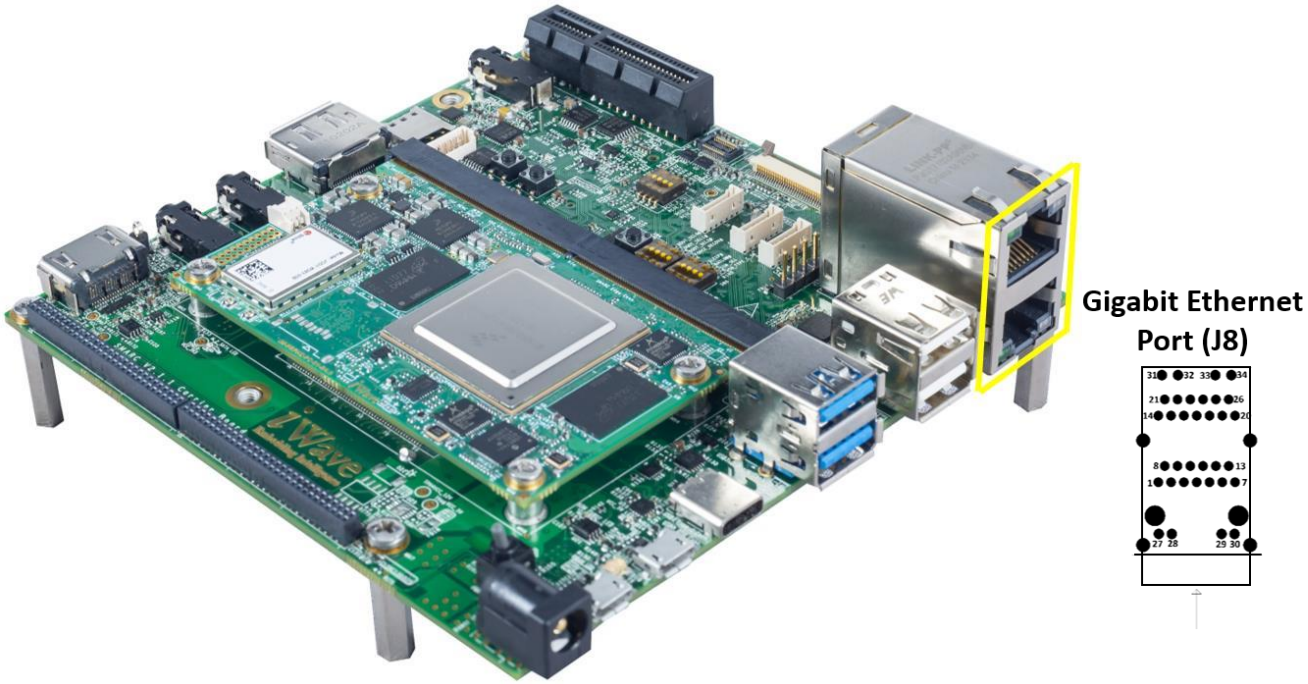


Figure 10: RJ45 Magjack

2.6.2 USB2.0 Host Interface

The Layerscape LS1021A SMARC carrier board supports additional two USB2.0 Host interface through on SOM USB3.0 Hub via SMARC USB1 and USB4 ports. USB1 signals from the edge connector is connected to on board 1:4 USB hub. The primary port is directly connected to J13 TOP and secondary port is connected to SATA M.2 connector; 4th Port of the USB2.0 HUB are connected to PCIe M.2 Module (Optional) respectively. Whereas USB4 port from the SMARC edge connector is directly connected to BOTTOM side of J13 connector.

The VBUS power of this USB2.0 connector is connected through current limit power switch and limit is set as 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of SMARC MXM connector USB1 and USB4 ports. This USB2.0 connector is physically located at the top of the board as shown below.

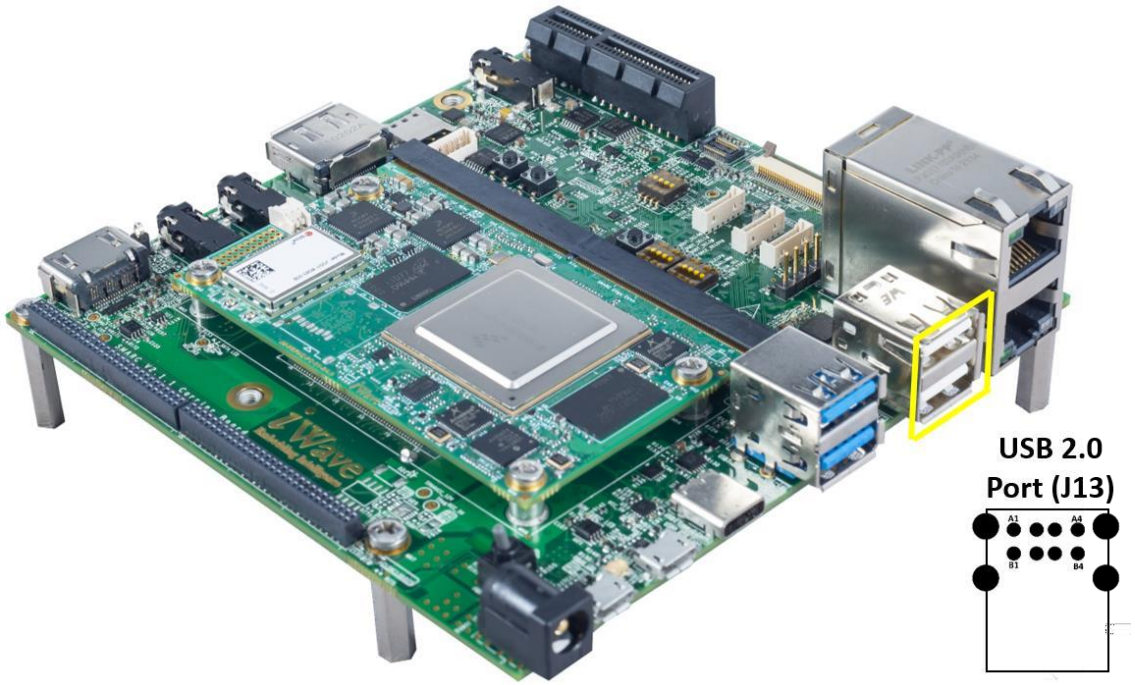


Figure 11: USB2.0 Host

2.6.3 USB2.0 OTG Interface

The SMARC carrier Board supports USB2.0 High Speed OTG interface through Layerscape LS1021A CPU's USB0 interface. This USB2.0 Port0 signals of SMARC MXM connector is directly connected to USB2.0 MicroAB connector (J22). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The connected SMARC SOM detects the USB functionality through USB ID pin and controls the power using the USB0_EN_OC# pin of SMARC MXM connector. In Host mode, USB0_EN_OC# should drive high to enable the power to the connector and in device mode, USB0_EN_OC# should drive low to disable the power to the connector. This USB2.0 OTG connector is physically located at the top of the board as shown below.

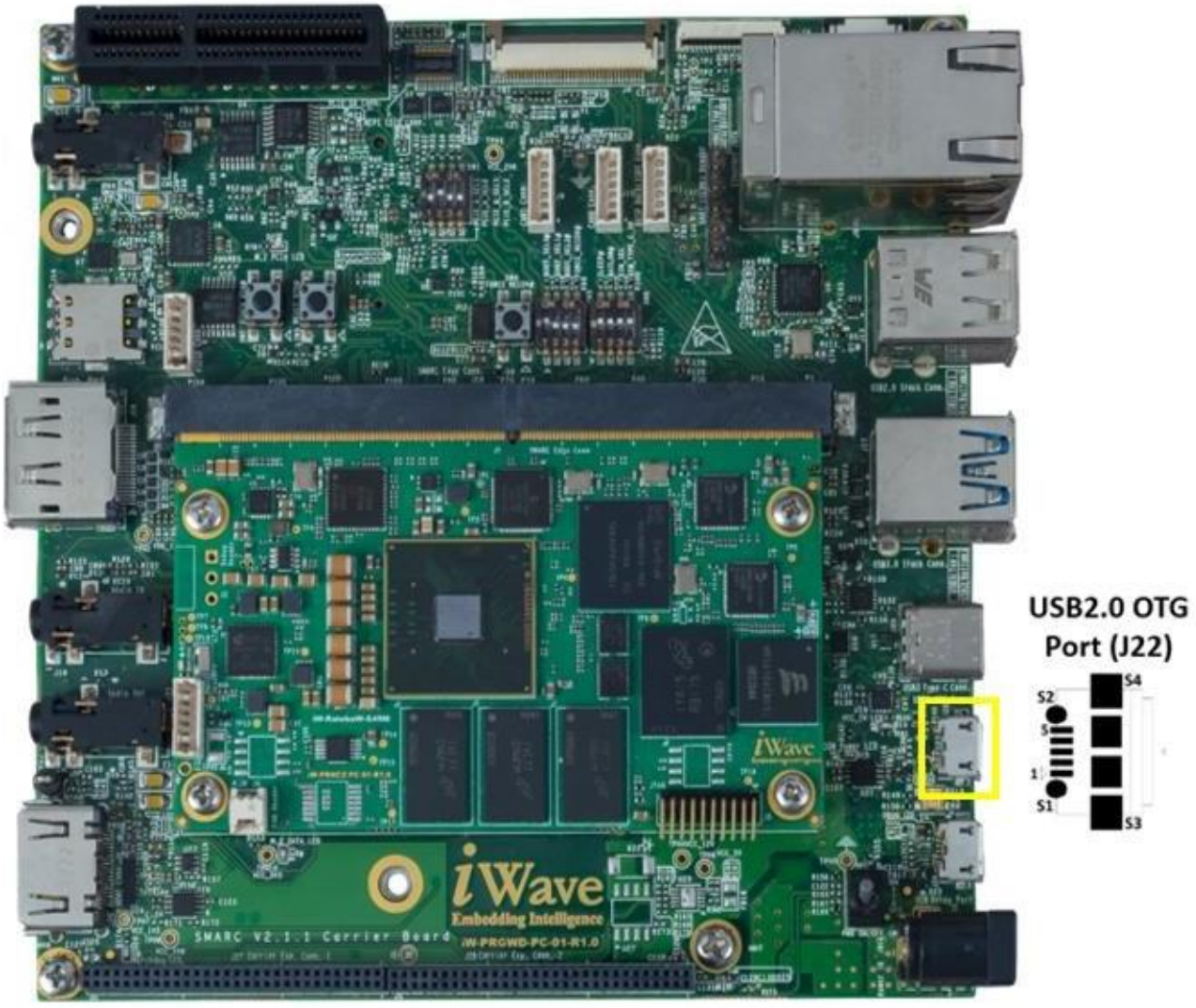


Figure 12: USB2.0 OTG

2.6.4 SDIO Interface (Optional)

The Layerscape LS1021A SMARC Carrier Board supports SDIO interface through CPU's eSDHC interface. This eSDHC signals from SMARC MXM connector is connected to SD connector (J34) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR_EN pin of SMARC MXM connector. The SD connector (J34) is physically located at the bottom of the board.

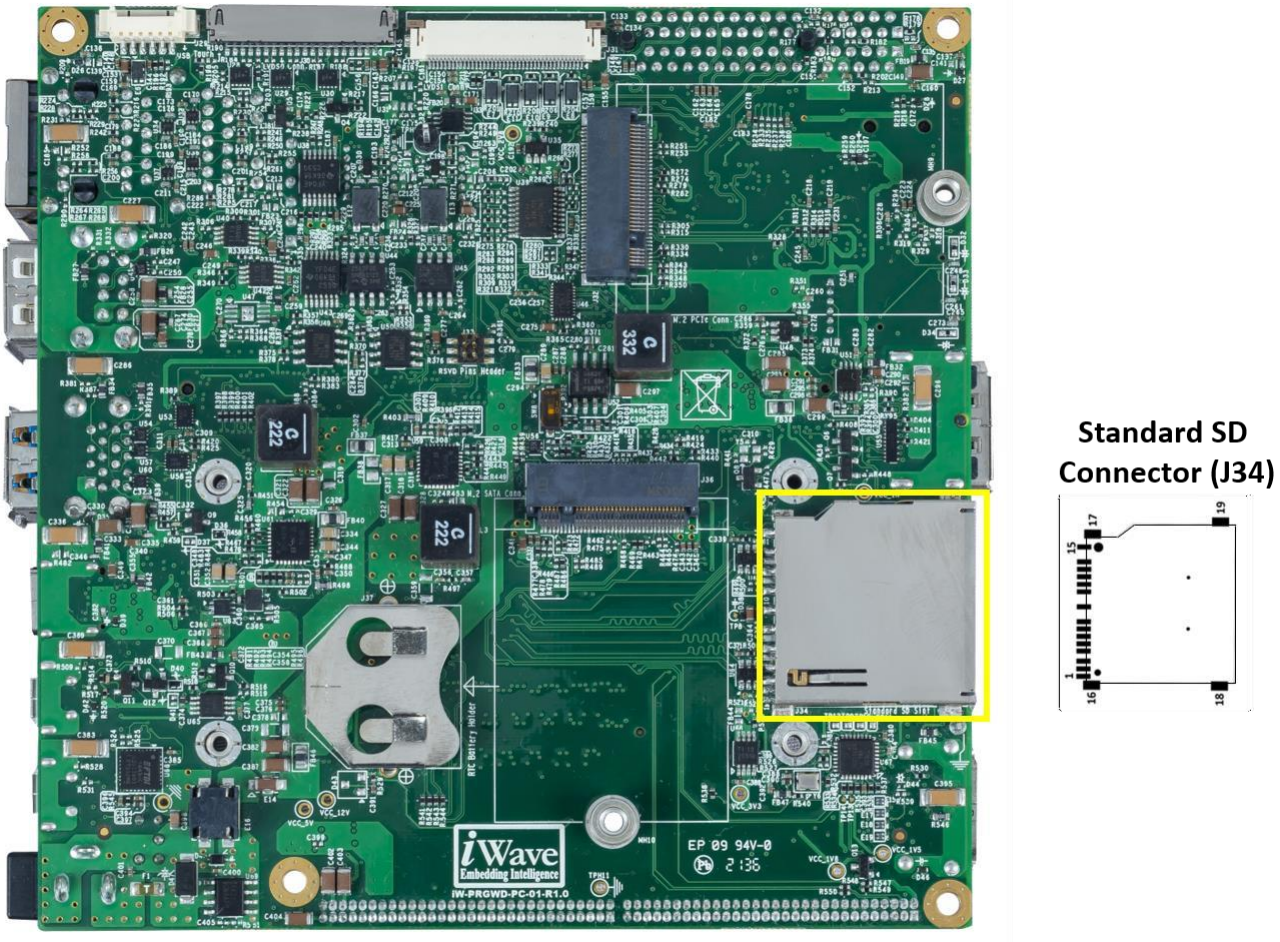


Figure 13:Standard SD Connector

2.6.5 CAN Interface

The SMARC Carrier Board supports two Control Area Network (CAN) Ports. Both CAN0 and CAN1 from the SMARC Edge connector are connected to MCP2562FD-E/SN CAN Transceiver and CANL & CANH of the transceiver are connected to J9 (CAN1) and J10 (CAN0) connectors. Both Connectors are placed on Top Side of the Board.

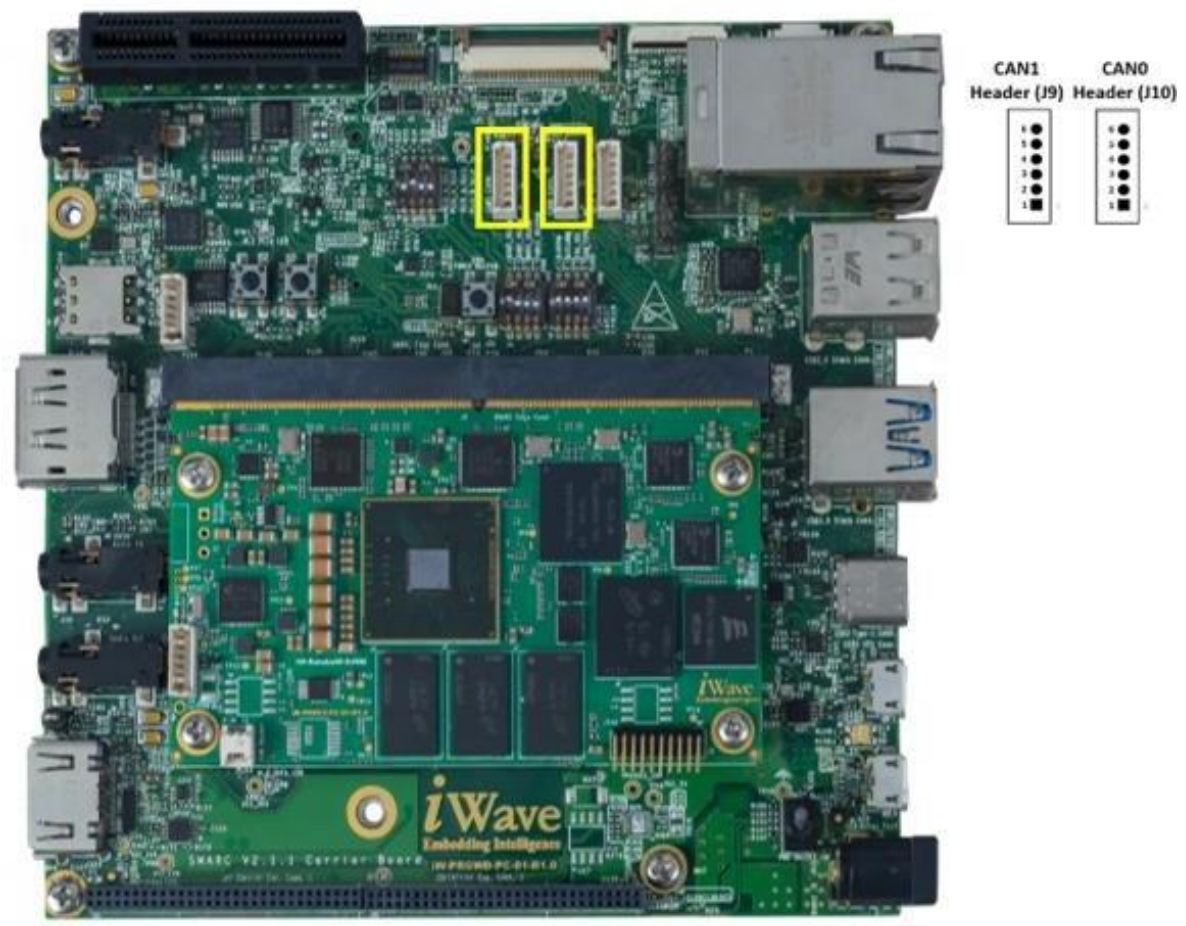


Figure 14: CAN Header

Table 8: CAN0 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Volatge.*
3	CANL	CAN0_LOW	IO, DIFF	CAN0 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_HIGH	IO, DIFF	CAN0 High-Level Voltage I/O
6	GND	GND	Power	Ground.

Table 9: CAN1 Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Volatge.*
3	CANL	CAN1_LOW	IO, DIFF	CAN1 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN1_HIGH	IO, DIFF	CAN1 High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.7 Audio Feature

2.7.1 I2S Audio Interface

The Layerscape LS1021A SMARC carrier board supports First Audio IN and OUT through CPU's SAI3 interface which can support I2S format. These four wire I2S signals from SMARC MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input through 3.5mm double audio Jack J21 and J19 correspondingly. Also, Headphone detect and Mic detect is supported through GPIO8 (P116th) & GPIO11 (P119th) pin of SMARC MXM connector correspondingly.

The Layerscape LS1021A SMARC carrier board supports Second Audio IN and OUT through CPU's SAI4 interface which can support I2S format and also SAI1 interface optionally connected to the PCIe M.2 Connector. These four wire I2S signals from SMARC MXM connector is direct connected to I2S Audio Codec "WM8960CGEFL/RV" to support Headphone Stereo output and Mono Mic input through 3.5mm single audio Jack J7. Second Codec is not supported in default BSP, contact iWave support team for enabling second I2S Audio Codec "WM8960CGEFL/RV".

These Audio Jacks are physically located at the top of the board as shown below.

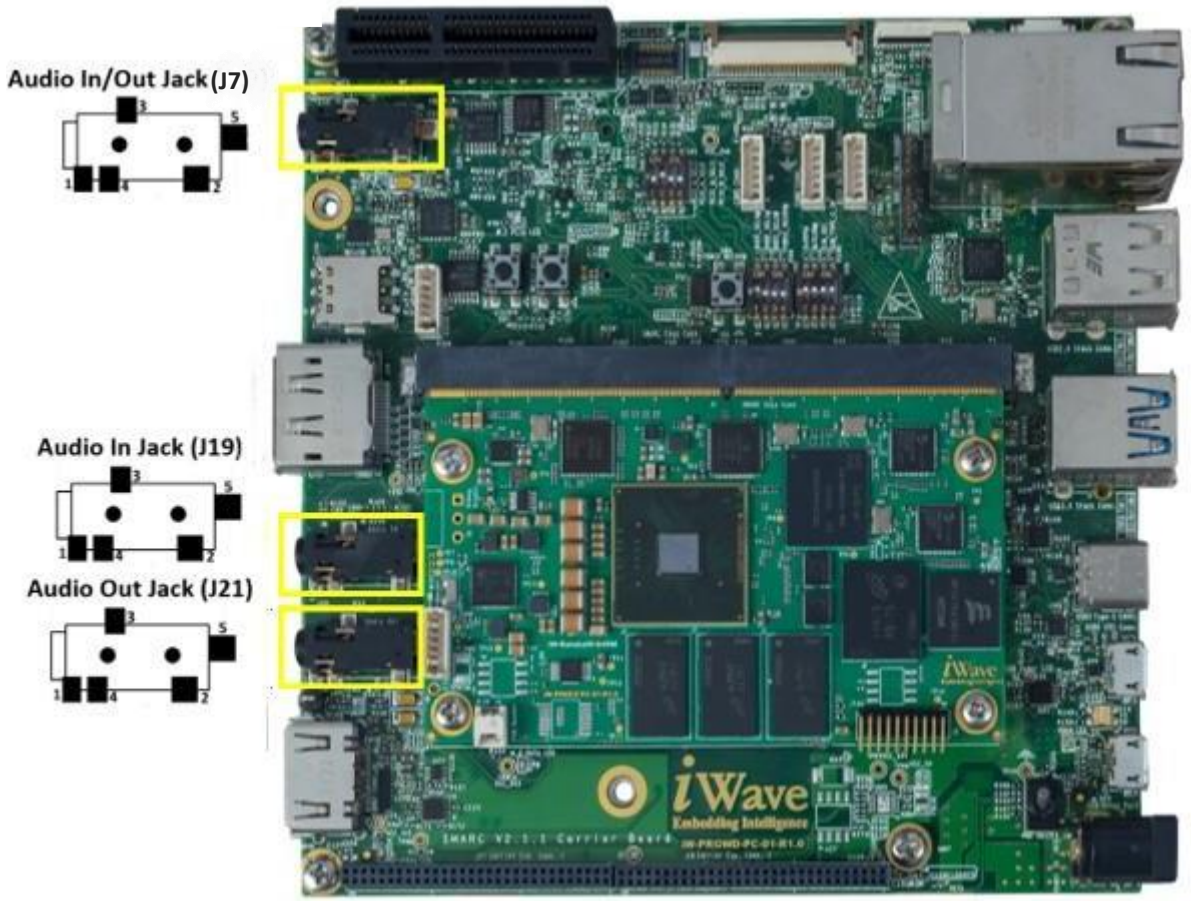


Figure 15: Audio Jack

2.8 Additional Features

2.8.1 SPI Flash

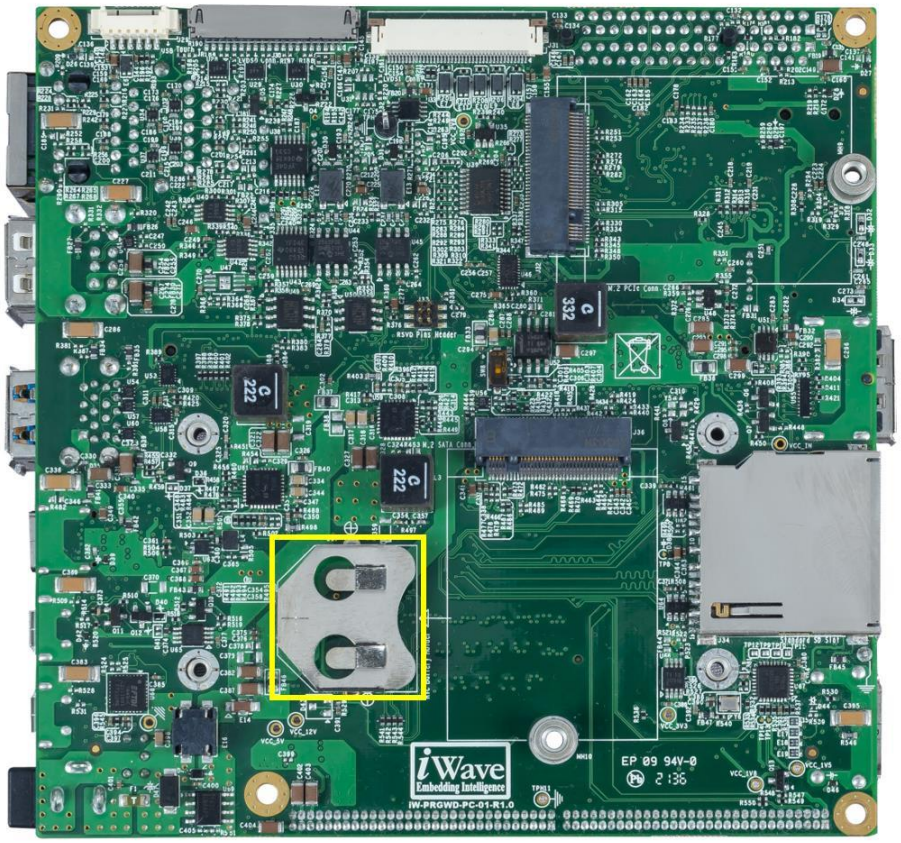
The Layerscape LS1021A SMARC development board supports SPI Flash(U49) through Layerscape LS1021A CPU's SPI1 interface. This SPI interface signals from SMARC MXM connector are connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

2.8.2 QSPI Flash

The Layerscape LS1021A SMARC development board by default supports 2nd SPI Flash(U50) through Layerscape LS1021A CPU's QSPI interface and optionally same IC Can support as QSPI. This SPI interface signals from SMARC MXM connector are connected to SPI Flash "IS25WP016D-JNLE" and operating at 1.8V Level.

2.8.3 RTC Coin Cell Holder

The Layerscape LS1021A SMARC development board supports Coin Cell Holder to connect "2032" series coin cell. This coin cell voltage is connected to SMARC MXM connector VDD_RTC pin (S147th) for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J37) is physically located on bottom of the board as shown below.



RTC Battery Holder (J37)

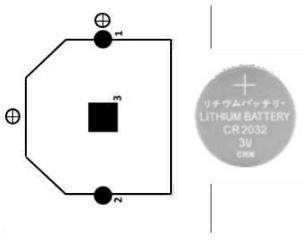


Figure 16: RTC Battery Holder

2.9 On Board Switches

SMARC development board has seven Switches on Top side of carrier card to support generic SMARC features. All the seven switches location is highlight in below image and the switch description is given in the following table.

Figure 17: SMARC On Board Switches

Table 10: Board Configuration Switch

<table>
<tr><th>SW Identifier/ (SW Type)</th><th>No. of Bits</th><th>Bit Name</th><th colspan="3">Description</th><th>Remark</th></tr>
<tr><th></th><th></th><th></th><th colspan="2">ON/Push</th><th>OFF/Release</th><th></th></tr>
<tr><td rowspan="4">SW1 (DIP SW)</td><td>1</td><td>PCIe_A_SEL1</td><td colspan="3"><u>PCIe Channel 0 Connection:</u></td><td rowspan="4">1-Switch OFF (Pulled High) 0 -Switch ON (GND)

Note: At a time, do not set Both the PCIe Channel</td></tr>
<tr><td>2</td><td>PCIe_A_SEL2</td><td>State [SEL2,SEL1]</td><td>Select</td><td>Reference image</td></tr>
<tr><td></td><td></td><td>00</td><td>Hi-Z</td><td>  </td></tr>
<tr><td></td><td></td><td>01</td><td>M.2 Lane0</td><td>  </td></tr>
</table>

<table>
<tr><th>SW Identifier/ (SW Type)</th><th>No. of Bits</th><th>Bit Name</th><th colspan="2">Description</th><th>Remark</th></tr>
<tr><th></th><th></th><th></th><th>ON/Push</th><th>OFF/Release</th><th></th></tr>
<tr><td rowspan="4"></td><td></td><td></td><td colspan="2"><table><tr><td>10</td><td>M.2 Lane1</td><td>  </td></tr><tr><td>11</td><td>PCIe x4(Lane0)</td><td>  </td></tr></table></td><td rowspan="4">A & B neither to PCIe x4 nor to M.2 connector.</td></tr>
<tr><td>3</td><td>PCIe_B_SEL1</td><td colspan="2"><u>PCIe Channel 1 Connection:</u></td></tr>
<tr><td>4</td><td>PCIe_B_SEL2</td><td colspan="2"><table><tr><th>State [SEL2,SEL1]</th><th>Select</th><th>Reference image</th></tr><tr><td>00</td><td>Hi-Z</td><td>  </td></tr><tr><td>01</td><td>M.2 Lane0</td><td>  </td></tr><tr><td>10</td><td>M.2 Lane1</td><td>  </td></tr><tr><td>11</td><td>PCIe x4(Lane1)</td><td>  </td></tr></table></td></tr>
<tr><td>SW2 (Push button)</td><td>1</td><td>POWER_BTN#</td><td colspan="2">SOM Power ON - One Press and release
SOM Power OFF - Long Press (above 5sec)</td><td>SOM Power ON/OFF Switch</td></tr>
<tr><td>SW3 (Push button)</td><td>1</td><td>RESET_IN#</td><td colspan="2">SOM Reset – While Pressing
SOM Out of reset – When release</td><td>SOM Reset Switch</td></tr>
<tr><td>SW4 (Push button)</td><td>1</td><td>FORCE_RECOV#</td><td>-</td><td>-</td><td>Not Supported
Note: Same signal is also connected to SW5 4th bit</td></tr>
<tr><td rowspan="3">SW5 (DIP SW)</td><td>1</td><td>BOOT_SEL0#</td><td colspan="2" rowspan="3"><u>BOOT_SEL[2:0]#</u>
000- Boot from SOM FlexSPI (Optional)
001- Boot from SOM eMMC (Default)
011- Boot from SOM microSD (Optional)
110- Boot from Carrier Board SD</td><td rowspan="3">0-Switch OFF (Floating)

1 -Switch ON (GND)</td></tr>
<tr><td>2</td><td>BOOT_SEL1#</td></tr>
<tr><td>3</td><td>BOOT_SEL2#</td></tr>
</table>

SW Identifier/ (SW Type)	No. of Bits	Bit Name	Description		Remark
			ON/Push	OFF/Release	
	4	FORCE_RECOV#	CPU USB Serial Mode (For programming the SOM boot media)	CPU Normal Boot Mode	*Note: Same signal is also connected to SW4*
SW6 (DIP SW)	**1**	LID#/SLEEP#*	-	-	Not Supported
	2	BATLOW#/CHARGING#*	-	-	Not Supported
	3	TEST#/CHARGER_PRSNT#/SIM_SEL	-	-	By default, SIM Select function is supported
	4	USB_TYPE_C_SW	USB3 port is connected to USB Type A (J17, Top) connector.	USB3 port is connected to USB Type C (J20) connector.	
SW7 (Toggle SW)	**1**	Carrier Power ON/ OFF Switch	Carrier Board Power is ON	Carrier board Power is OFF	Carrier Board Main 12V Power On/Off Switch.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Layerscape LS1021A SMARC Development Platform technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The Layerscape LS1021A SMARC Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the SMARC Carrier Board through Power Jack (J26). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed at the top of the board as shown below.

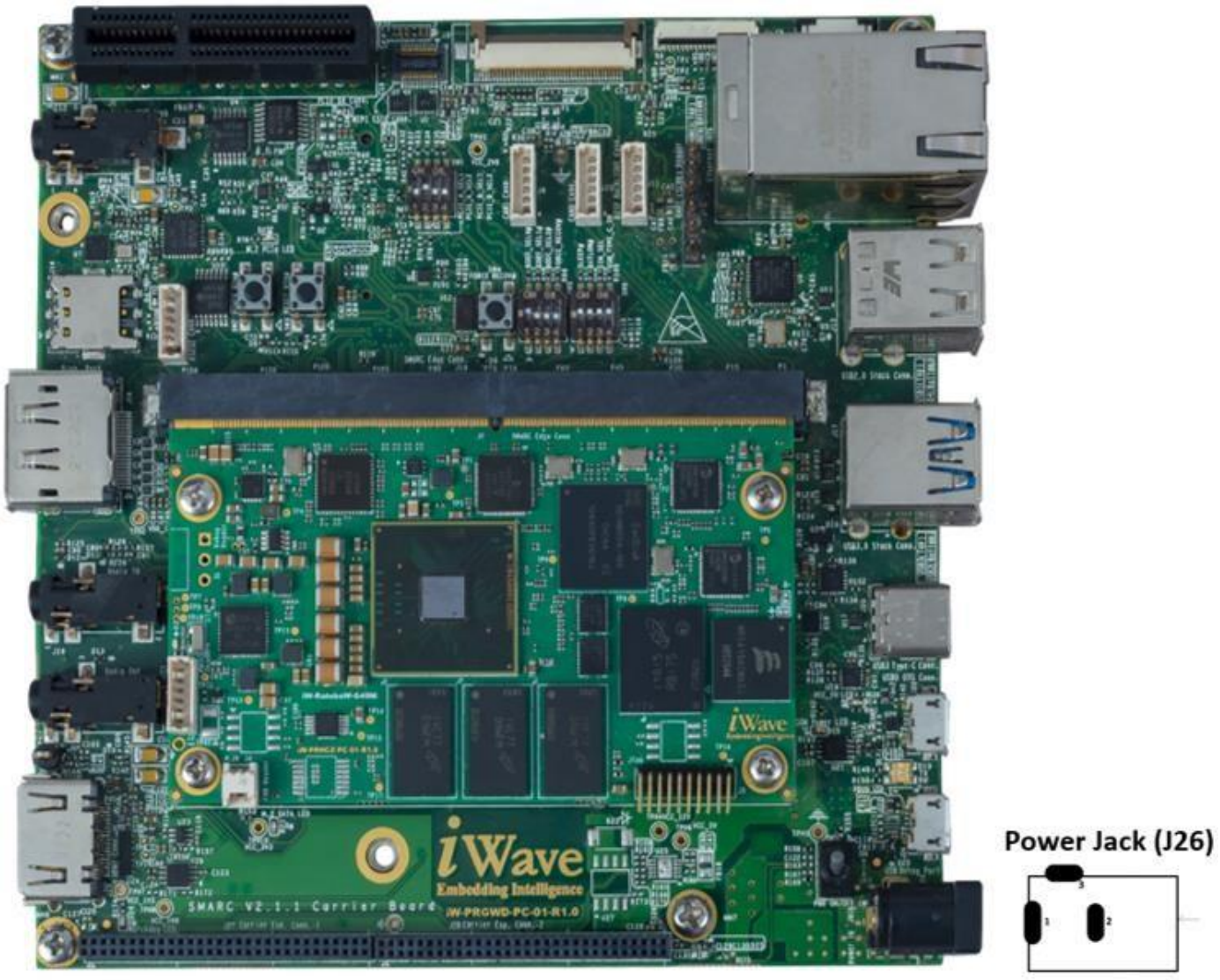


Figure 18: Power Jack

Table 11: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] SMARC Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of Layerscape LS1021A SMARC SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

3.2 Power Output Specification

The Layerscape LS1021A SMARC Carrier Board has dedicated power regulator to provide +5V power to SMARC SOM for VIN power supply. Also +3V RTC power from coin cell holder is provided to SMARC SOM for Real time clock support.

The Layerscape LS1021A SMARC carrier board also shares different on-board power to Audio & Video connector and Carrier Expansion connector2 for its Add-On Module power.

Table 12: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to SMARC SOM (through SMARC MXM connector)					
1	VIN_5V	4.85V	5V	5.15V	5000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Expansion Connector1)					
1	VCC_5V	4.85V	5V	5.15V	1000mA
2	VCC_3V3	3.15	3.3	3.45	1000mA
3	VCC_1V8	1.7	1.8	1.9	1000mA
Power to Add-On Module (through Expansion Connector2)					
1	VCC_5V	4.85V	5V	5.15V	1000mA
2	VCC_3V3	3.15	3.3	3.45	1000mA
3	VCC_1V8	1.7	1.8	1.9	1000mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of Layerscape LS1021A SMARC Development Platform.

Table 13: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	60°C

[1] *iWave guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's Layerscape LS1021A SMARC Development Platform is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's Layerscape LS1021A SMARC Development Platform is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the Development Platform except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 Layerscape LS1021A SMARC Carrier Board Mechanical Dimensions

Layerscape LS1021A SMARC Development Platform PCB size is 120 mm x 120 mm x 1.6mm. SMARC carrier card mechanical dimensions is shown below. (All dimensions are shown in mm)

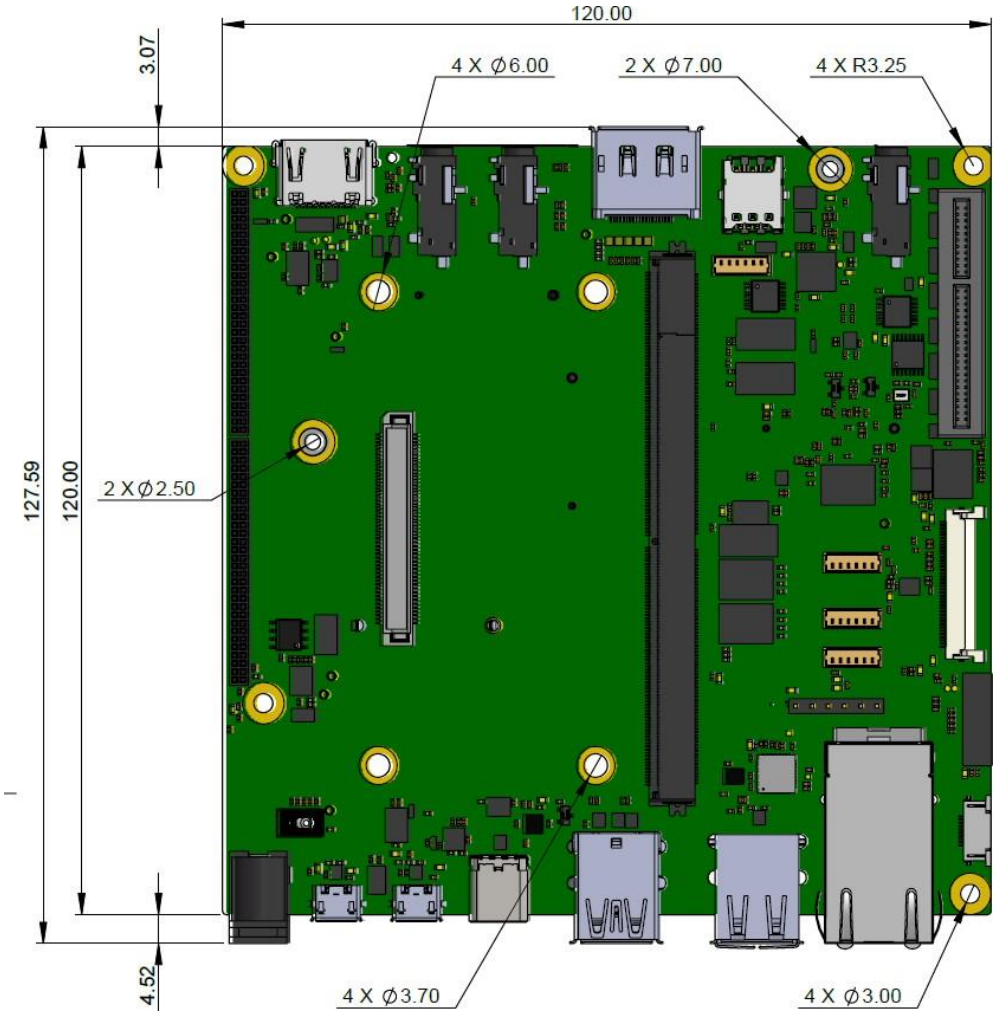


Figure 19: Mechanical dimensions of Layerscape LS1021A SMARC Carrier Board- Top View

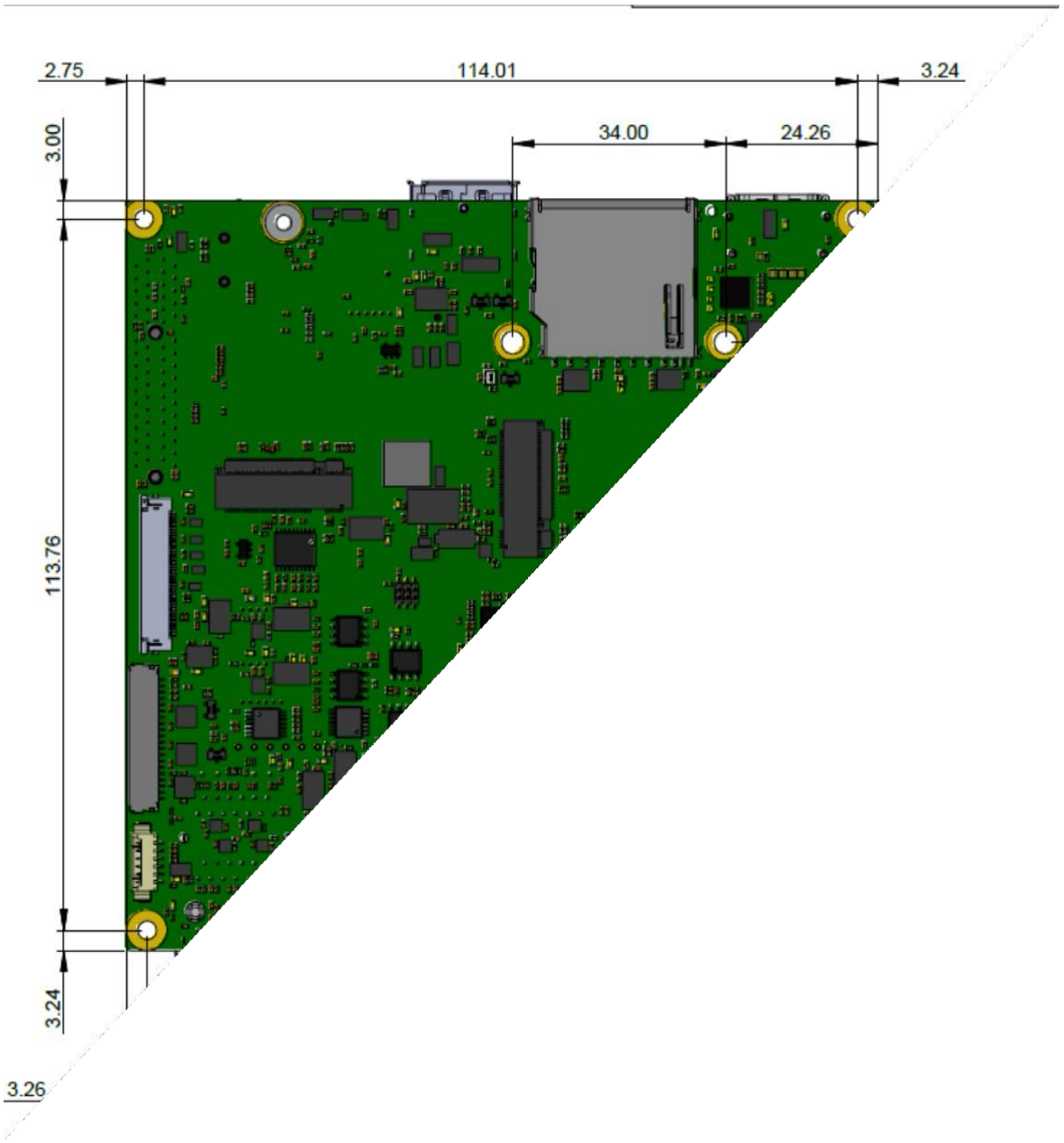


Figure 20: Mechanical dimensions of Layerscape LS1021A SMARC Carrier Board- Bottom View

Layerscape LS1021A SMARC Development Platform PCB thickness is 1.6mm±0.16mm, top side maximum height component is connector dual Ethernet Jack J8 (28.58mm) followed by USB3.0 Stack slot J17(15.6mm) and bottom side maximum height component is inductor (7.3mm). Please refer the below figure which gives height details of the i.MX8 SMARC Development kit.

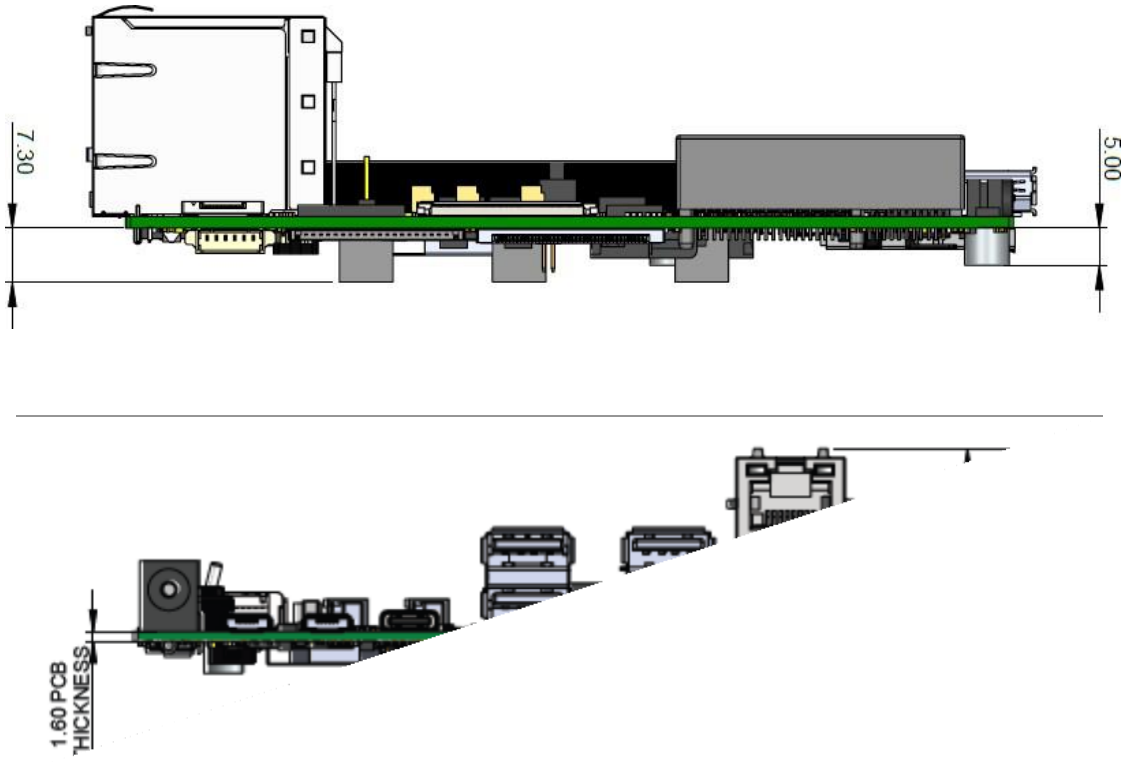


Figure 21: Mechanical dimensions of Layerscape LS1021A SMARC Carrier Board - Side View

3.4.2 Guidelines to insert the SMARC SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the SMARC module in to the MXM connector at an angle of 30° as shown in below image.
- Check the Notch position of SMARC module is proper while inserting.
- Once the SMARC module is inserted to the MXM connector properly, press the board vertically down as shown below, such that the board is fixed firmly into the expansion connectors and fix the board by screwing.

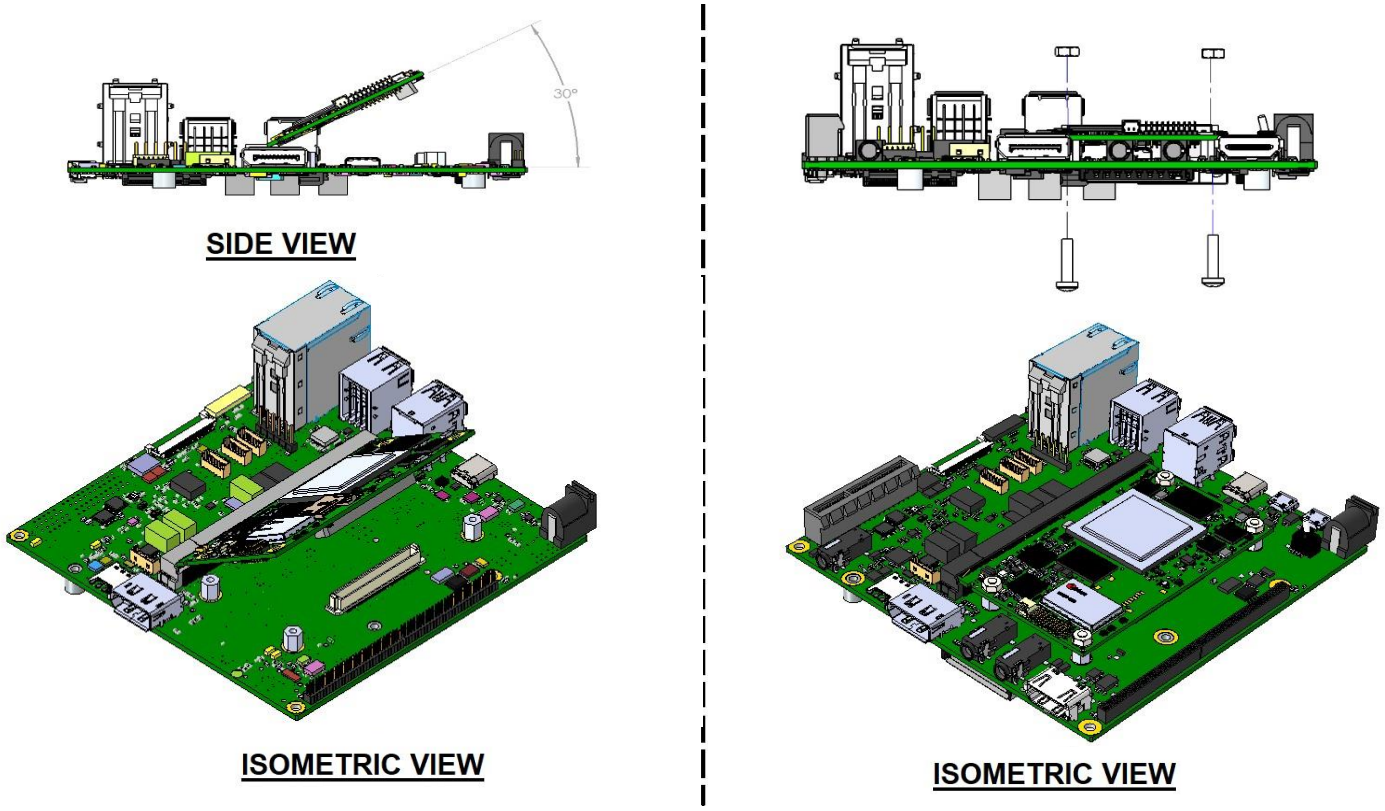


Figure 22: SOM Insertion Guideline

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Layerscape LS1021A SMARC Development Platform which includes SMARC SOM and SMARC carrier board.

Table 14: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G49D-SC02-4L002G-E016G-LCA	LS1021A, Dual Cortex A7, 1.2 GHz CPU, 2GB DDR4 with ECC, 16GB eMMC, TPM	0°C to 60°C

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.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