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## MAX14919/MAX14919A

## Industrial-Protected, Quad-Channel, Low-Side Switch

### General Description

The MAX14919/MAX14919A industrial-protected quad-channel low-side switch features 140mΩ (typ) on-resistance ( $R_{ON}$ ) per channel with integrated  $\pm 1\text{kV}/42\Omega$  surge protection for robust operation.

Resistor-settable accurate current limiting provides guaranteed operating currents in the range of 100mA to 800mA. Loads that draw large activation or inrush currents are supported using the 2x inrush load-current option. The outputs can be connected in parallel to achieve higher load currents. The four switches are pin-controlled to allow for simple and fast switching of up to 200kHz.

The MAX14919/MAX14919A feature reverse current detection. The MAX14919 implements reverse-current protection by driving an external FET for non-capacitive loads. The MAX14919A has reverse current indication.

Inductive loads are turned off rapidly using the internal high-voltage clamps. The switches are short-circuit and overload protected.

The MAX14919/MAX14919A quad low-side switch is available in a 6.5mm x 6.4mm footprint 20-TSSOP package and a 4mm x 5mm footprint 20-TQFN package specified over the  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range.

### Applications

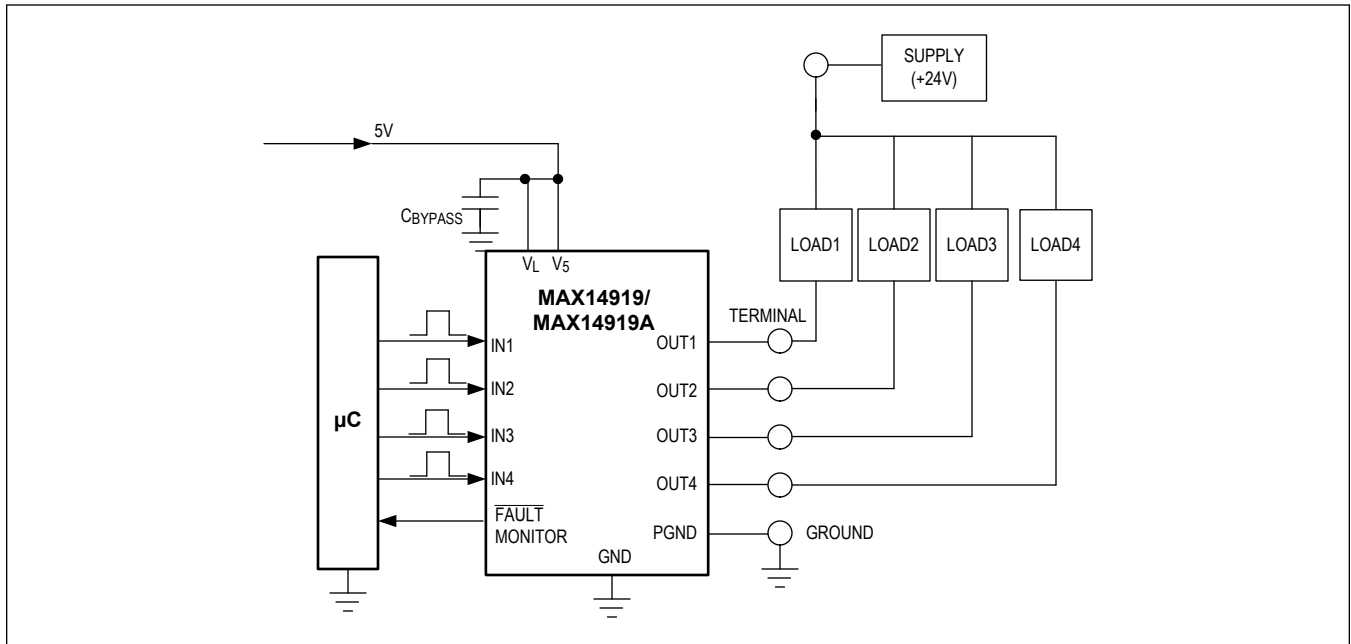
- Industrial Digital Outputs
- Relay and Solenoid Drivers
- PLC and DCS Systems
- Motor Control

### Benefits and Features

- 5V or 7V to 60V Supply Voltage
- 800mA Load Current per OUT
- Integrated 5V/30mA Linear Regulator
- Logic Supply Input from 1.62V(min) to 5.5V(max)
- 5V to 48V Load Voltage Range
- Up to 200kHz (min) Switching Rates
- 2x Inrush Load Current Option for 10ms
- Reduces Power and Heat Dissipation
  - 140mΩ (typ) On-Resistance per channel
  - 1.7mA (typ) Supply Current
  - Settable Load Current Limit
- Robust Design Features
  - Internal inductive Energy Clamp at 55V(typ)
  - Short-Circuit Protection
  - Reverse Current Detection against Load-Supply Miswiring
  - $\pm 1\text{kV}/42\Omega$ , 8μs/20μs Surge Protection
  - $\pm 8\text{kV}$  Contact and  $\pm 25\text{kV}$  Airgap ESD Protection
  - $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Operating Ambient Temperature
- $\overline{\text{FAULT}}$  Indication for:
  - Thermal Overload
  - Reverse Load Current Detection
  - Undervoltage Lockout on  $V_5$  Supply
- Compact 20-pin, 6.5mm x 6.4mm TSSOP Package
- Compact 20-pin, 4mm x 5mm TQFN Package

Ordering Information appears at end of data sheet.

## Simplified Low-Side Switch Application



## Absolute Maximum Ratings

V <sub>DD</sub> .....	-0.3V to 65V
V <sub>5</sub> .....	-0.3V to +6V
V <sub>L</sub> , FAULT.....	-0.3V to +6V
REV, RCLIM.....	-0.3V to (V <sub>5</sub> + 0.3V)
IN.....	-0.3V to +6V
OUT1, OUT2, OUT3, OUT4.....	-0.3V to V <sub>CLAMP</sub>
OUT_ Load Current (Current limit defined by R <sub>LIM</sub> resistor).....	Internally Limited
Continuous Current (any other terminal).....	±100mA

Continuous Power Dissipation (Single-Layer Board) (20-TSSOP) (T <sub>A</sub> = +70°C, derate 65mW/°C above +70°C).....	1739mW
Continuous Power Dissipation (Multilayer Board) (20-TSSOP) (T <sub>A</sub> = +70°C, derate 55mW/°C above +70°C).....	2122mW
Continuous Power Dissipation (Multilayer Board) (20-TQFN) (T <sub>A</sub> = +70°C, derate 32.96mW/°C above +70°C).....	2636.78mW
Operating Temperature Range.....	-40°C to 125°C
Junction Temperature.....	Internally Limited
Storage Temperature Range.....	-65°C to +150°C
Soldering Temperature (reflow).....	260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### 20 TSSOP

Package Code	U20E+3C
Outline Number	<a href="#">21-100132</a>
Land Pattern Number	<a href="#">90-100049</a>
<b>THERMAL RESISTANCE, SINGLE-LAYER BOARD</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	46°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	2°C/W
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	37°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	2°C/W

### 20 TQFN

Package Code	T2045+1C
Outline Number	<a href="#">21-0726</a>
Land Pattern Number	<a href="#">90-100091</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction-to-Ambient (θ <sub>JA</sub> )	30.34°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> )	1.98°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{DD} = 7V$  to  $60V$ ,  $V_5 = 4.5$  to  $5.5V$ ,  $V_L = 1.62V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$  and  $V_{DD} = +24.0V$ ,  $V_L = V_5$ ) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY (V <sub>5</sub> , V <sub>L</sub> )							
V <sub>5</sub> Supply Voltage	V <sub>5</sub>	V <sub>DD</sub> = GND or unconnected		4.5	5.0	5.5	V
V <sub>5</sub> Supply Current	I <sub>V5_ON</sub>	V <sub>DD</sub> = GND or unconnected	All OUT_ turned on or off		1.6	3	mA
V <sub>5</sub> Undervoltage-Lockout Threshold	V <sub>5_UVLO</sub>	V <sub>DD</sub> = GND or unconnected	OUT_ are three-state in UVLO, V <sub>5</sub> falling	3.6		4.2	V
V <sub>5</sub> Undervoltage-Lockout Hysteresis	V <sub>5_UVLO_HYS</sub>	V <sub>DD</sub> = GND or unconnected			0.2		V
V <sub>L</sub> Supply Voltage	V <sub>L</sub>			1.62		5.5	V
V <sub>L</sub> Supply Current	I <sub>VL</sub>	Logic inputs at GND or V <sub>L</sub>				20	μA
V <sub>L</sub> Undervoltage-Lockout Threshold	V <sub>L_UVLO</sub>	V <sub>L</sub> falling		0.7		1.4	V
V <sub>L</sub> Undervoltage-Lockout Hysteresis	V <sub>L_UVLO_HYS</sub>				50		mV
LINEAR REGULATOR (V <sub>DD</sub> , V <sub>5</sub> )							
V <sub>DD</sub> Supply-Voltage Range	V <sub>DD</sub>			7		60	V
V <sub>DD</sub> Supply Current	I <sub>DD</sub>	V <sub>5</sub> = No Load			1.7	3	mA
V <sub>5</sub> Regulator Output Voltage	V <sub>5</sub>	0mA to 30mA external load current		4.75	5.00	5.25	V
V <sub>5</sub> Regulator Current Limit	I <sub>CL_V5</sub>			35			mA
V <sub>5</sub> Line Regulation		7V ≤ V <sub>DD</sub> ≤ 60V, I <sub>V5</sub> = 5mA			0.002		mV/V
V <sub>5</sub> Load Regulation		0 ≤ I <sub>V5</sub> ≤ 20mA			0.175		%
SWITCH OUTPUTS (OUT_)							
On-Resistance	R <sub>ON</sub>	I <sub>OUT_</sub> = 600mA			140	300	mΩ
Current Limit	I <sub>LIM</sub>	INRUSH = 0, or INRUSH = 1 and t <sub>LIM</sub> > 15ms	R <sub>LIM</sub> = 100kΩ	140		270	mA
			R <sub>LIM</sub> = 27kΩ	700	800	900	
			R <sub>LIM</sub> = open	650		950	
Inrush Current Limit	I <sub>LIM</sub>	INRUSH = 1 or high, for 10ms after switch turn-on		2 x I <sub>LIM</sub>			mA
Inductive Clamp Voltage	V <sub>CLAMP</sub>	OUT_ is OFF, I <sub>OUT_</sub> = 500mA		49	55		V
Off-State Leakage Current at OUT_	I <sub>LEAK</sub>	IN_ = low, V <sub>OUT_</sub> = 0V to 45V. (Note 2)		-15		+15	μA
CLIM Voltage	V <sub>CLIM</sub>				1.2		V
CLIM Short Resistance-Threshold Value	R <sub>LIM_SHORT</sub>			4.5	6.5	9	kΩ
CLIM Open Resistance-Threshold Value	R <sub>LIM_OPEN</sub>			400	650	1000	kΩ
Switch Turn-Off Propagation Delay (Low-to-High)	t <sub>OFF</sub>	Delay from IN_ switching low to OUT_ rising by 0.5V, R <sub>L</sub> = 48Ω, C <sub>L</sub> = 0.1nF, V <sub>LOAD</sub> = 24V (see Figure 1)			105	300	ns

**Electrical Characteristics (continued)**

( $V_{DD} = 7V$  to  $60V$ ,  $V_5 = 4.5$  to  $5.5V$ ,  $V_L = 1.62V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$  and  $V_{DD} = +24.0V$ ,  $V_L = V_5$ ) ([Note 1](#))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch Turn-On Propagation Delay (High-to-Low)	t <sub>ON</sub>	Delay between IN_ switching high to OUT_ falling by 0.5V, R <sub>L</sub> = 48Ω, V <sub>LOAD</sub> = 24V (see <a href="#">Figure 1</a> )		70	300	ns
Output Fall-Time	t <sub>F</sub>	Output falling 80% to 20% of final value, V <sub>LOAD</sub> = 24V, R <sub>L</sub> = 48Ω C <sub>L</sub> = 0.1nF (see <a href="#">Figure 2</a> )		160	250	ns
LOAD SUPPLY REVERSE POLARITY DETECT (REV)						
Reverse Current-Detect Threshold	I <sub>TH_OUT_REV_ON</sub>	V <sub>5</sub> > V <sub>5_UVLO</sub> , IN_ = high, current flow out of any OUT_	-190	-150	-115	mA
		V <sub>5</sub> > V <sub>5_UVLO</sub> , IN_ = low, current flow out of any OUT_	-185	-150	-95	
REV Output-Pullup Current	I <sub>REV_ON</sub>	(MAX14919 only) V <sub>5</sub> > V <sub>5_UVLO</sub> , I <sub>OUT_</sub> > I <sub>TH_OUT_REV</sub> , V <sub>REV</sub> = V <sub>5</sub> - 1V	25	45		μA
REV Output-Pulldown Resistance	R <sub>REV_OFF</sub>	V <sub>5</sub> > V <sub>5_UVLO</sub> , I <sub>OUT_</sub> < I <sub>TH_OUT_REV</sub>		10		Ω
Auto-Retry Delay	t <sub>REV_AR</sub>	Delay until REV output is turned back on after reverse-detection turn-off. MAX14919 only		2		s
Three-State Leakage	I <sub>REV_LKG</sub>	MAX14919A only		10		nA
LOGIC INPUTS (IN_, INRUSH)						
Input-Voltage High	V <sub>IH</sub>		0.8 x V <sub>L</sub>			V
Input-Voltage Low	V <sub>IL</sub>		0.2 x V <sub>L</sub>			V
Input-Threshold Hysteresis	V <sub>I_TH</sub>		0.1			V
Input-Pulldown Resistor	R <sub>PULLDOWN</sub>	All logic input pins	200			kΩ
LOGIC OUTPUT (FAULT)						
Output Logic Low	V <sub>OL</sub>	I <sub>LOAD</sub> = 5mA	0.33			V
Three-State Leakage	I <sub>LKG</sub>	Open-drain output off, V <sub>PULLUP</sub> = 5V ( <a href="#">Note 2</a> )	-1		+1	μA
THERMAL PROTECTION						
Channel Thermal-Shutdown Temperature	T <sub>JSHDN</sub>	Junction temperature rising, per channel	160			°C
Channel Thermal-Shutdown Hysteresis	T <sub>JSHDN_HYST</sub>		15			°C
Chip Thermal Shutdown	T <sub>CSHDN</sub>	Temperature rising	150			°C
Chip Thermal-Shutdown Hysteresis	T <sub>CSHDN_HYS_T</sub>		10			°C
LDO Shutdown Temperature	T <sub>DSHDN</sub>	Temperature rising	160			°C
EMC						
Surge Tolerance	V <sub>SURGE</sub>	OUT_ to GND, IEC 61000-4-5 with 42Ω	±1			kV
ESD IEC Contact Discharge	V <sub>ESD_C</sub>	OUT_ to GND, IEC 61000-4-2	±8			kV

Electrical Characteristics (continued)

( $V_{DD}$  = 7V to 60V,  $V_5$  = 4.5 to 5.5V,  $V_L$  = 1.62V to 5.5V,  $T_A$  = -40°C to +125°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C and  $V_{DD}$  = +24.0V,  $V_L$  =  $V_5$ ) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD IEC Air Discharge	$V_{ESD\_A}$	OUT_ to GND, IEC 61000-4-2		±25		kV
ESD	$V_{ESD}$	All other pins. Human Body Model		±2		kV

**Note 1:** All units are production tested at  $T_A$  = +25C. Specifications over temperature are guaranteed by design.

**Note 2:** Current into the device is positive and current out of the device is negative.

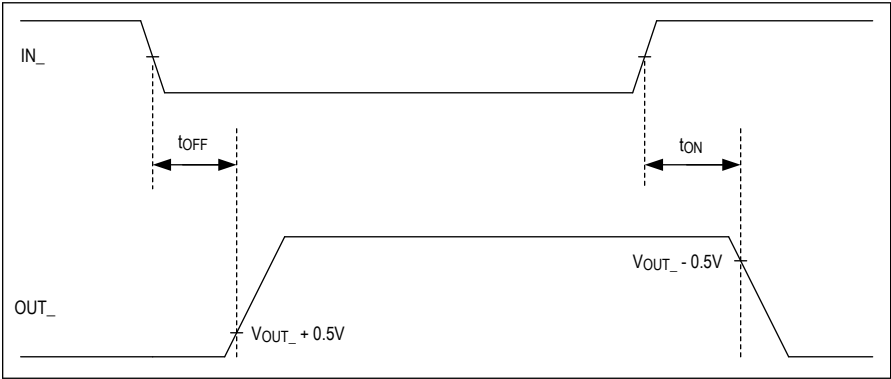


Figure 1. IN\_ to OUT\_ Propagation Times

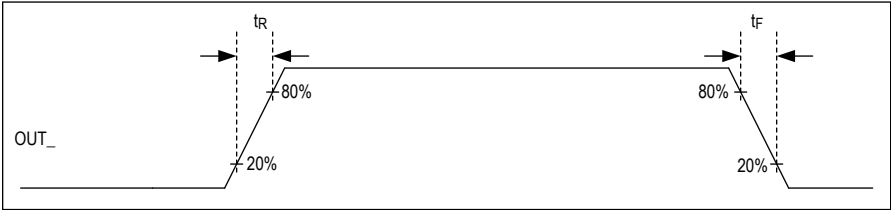
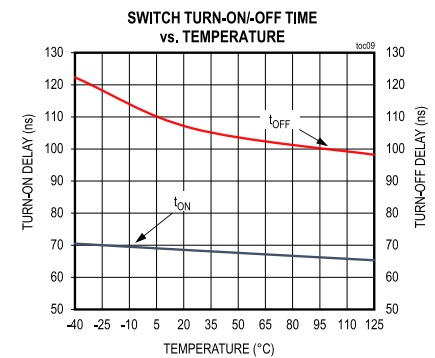
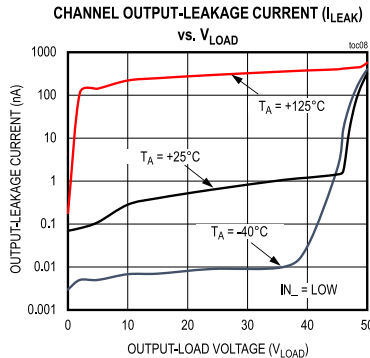
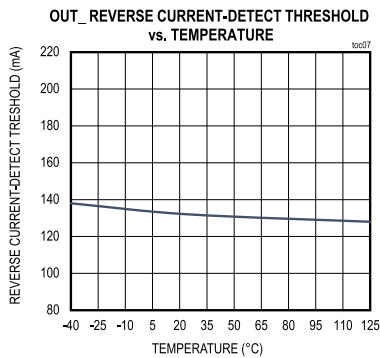
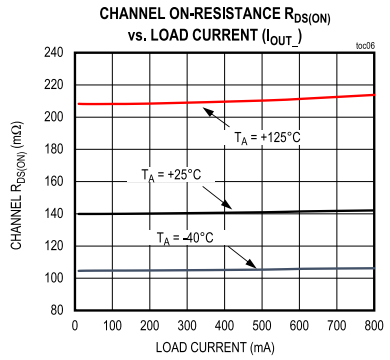
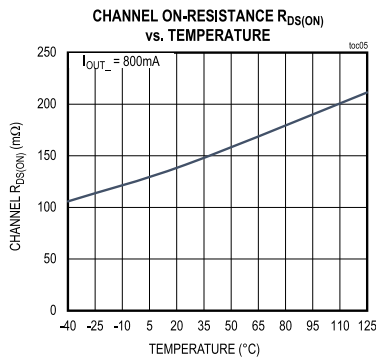
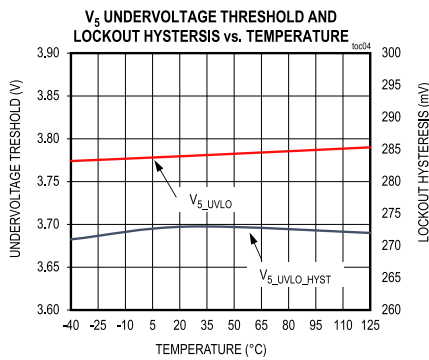
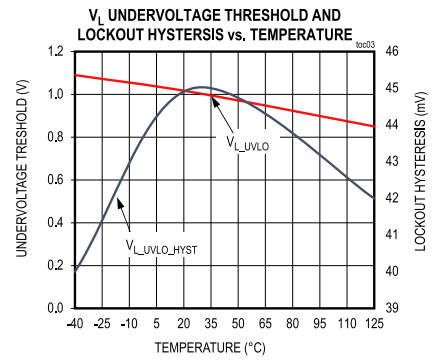
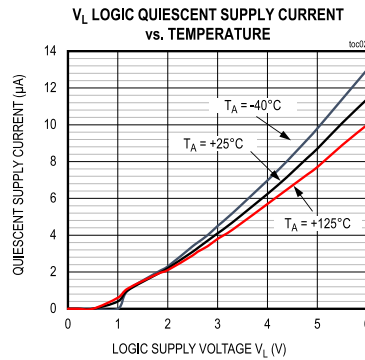
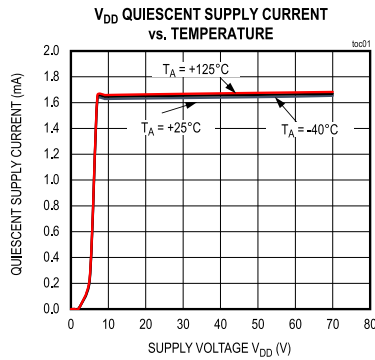
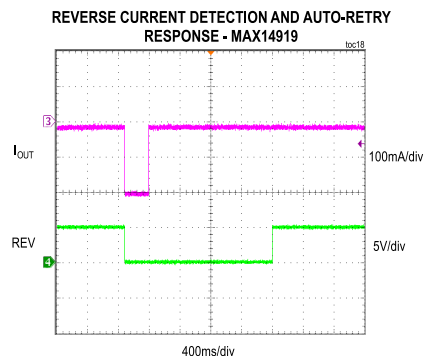
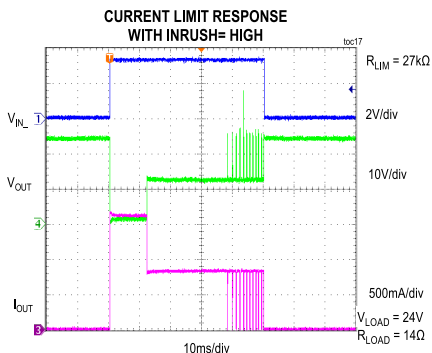
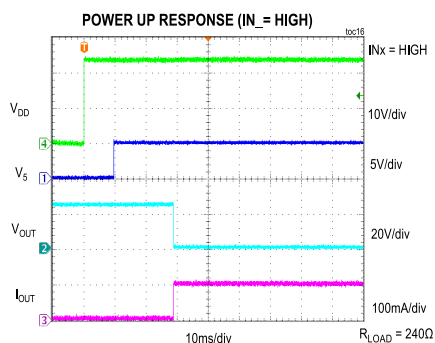
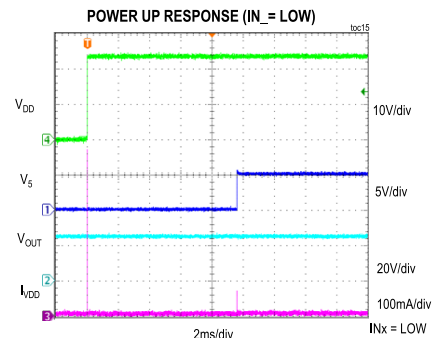
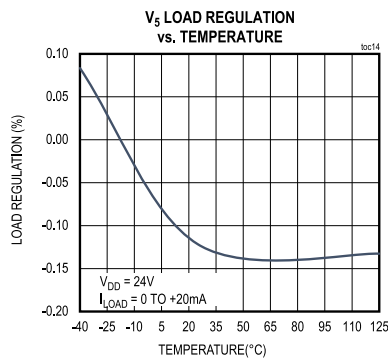
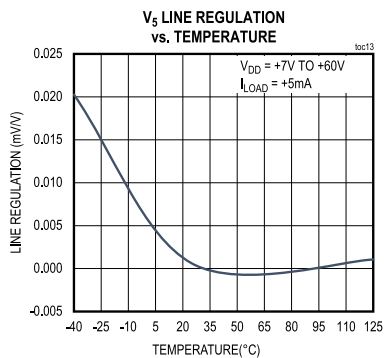
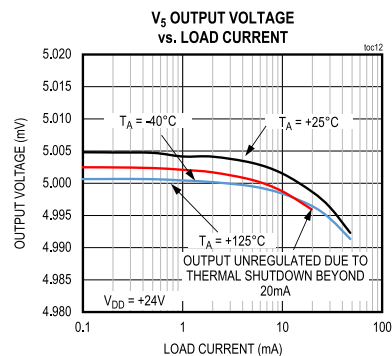
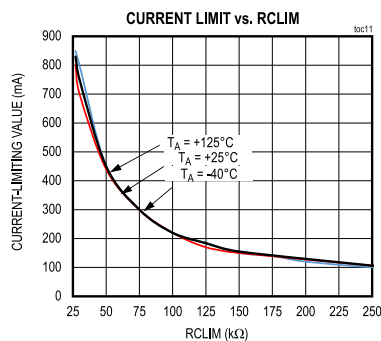
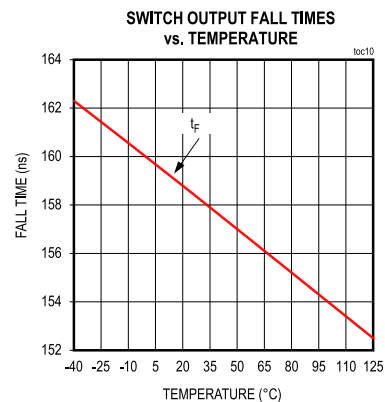


Figure 2. Output Channel Rise and Fall Times

## Typical Operating Characteristics

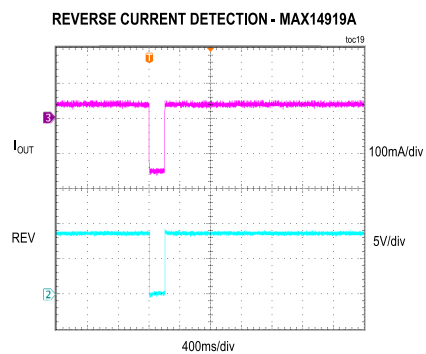
(V<sub>DD</sub> = +24V, V<sub>L</sub> = +3.3V, INRUSH = LOW, T<sub>A</sub> = 25°C unless otherwise noted.)

## Typical Operating Characteristics (continued)

(V<sub>DD</sub> = +24V, V<sub>L</sub> = +3.3V, INRUSH = LOW, T<sub>A</sub> = 25°C unless otherwise noted.)

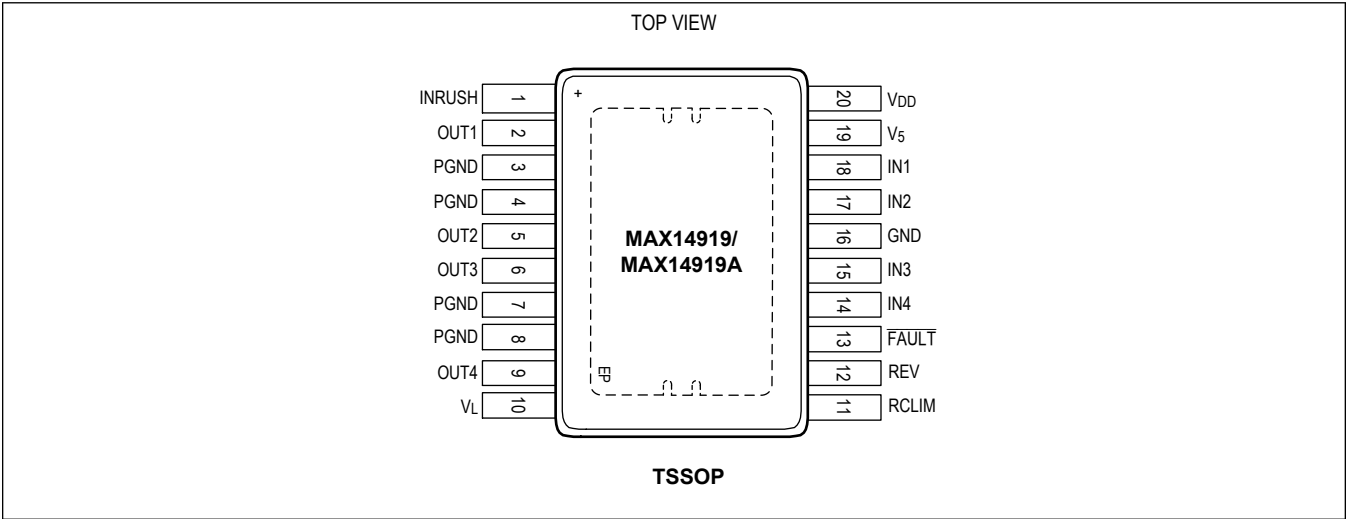
**Typical Operating Characteristics (continued)**

( $V_{DD} = +24V$ ,  $V_L = +3.3V$ , INRUSH = LOW,  $T_A = 25^\circ C$  unless otherwise noted.)

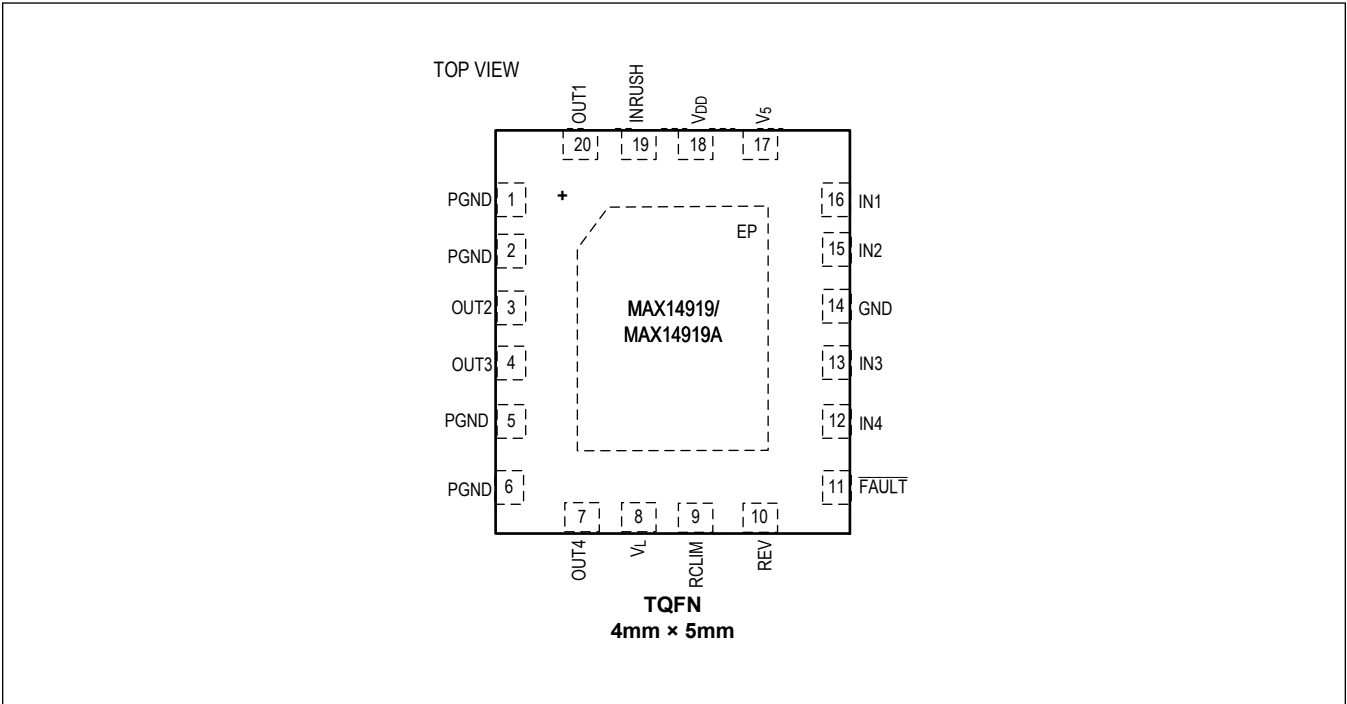


Pin Configurations

20 TSSOP



20 TQFN

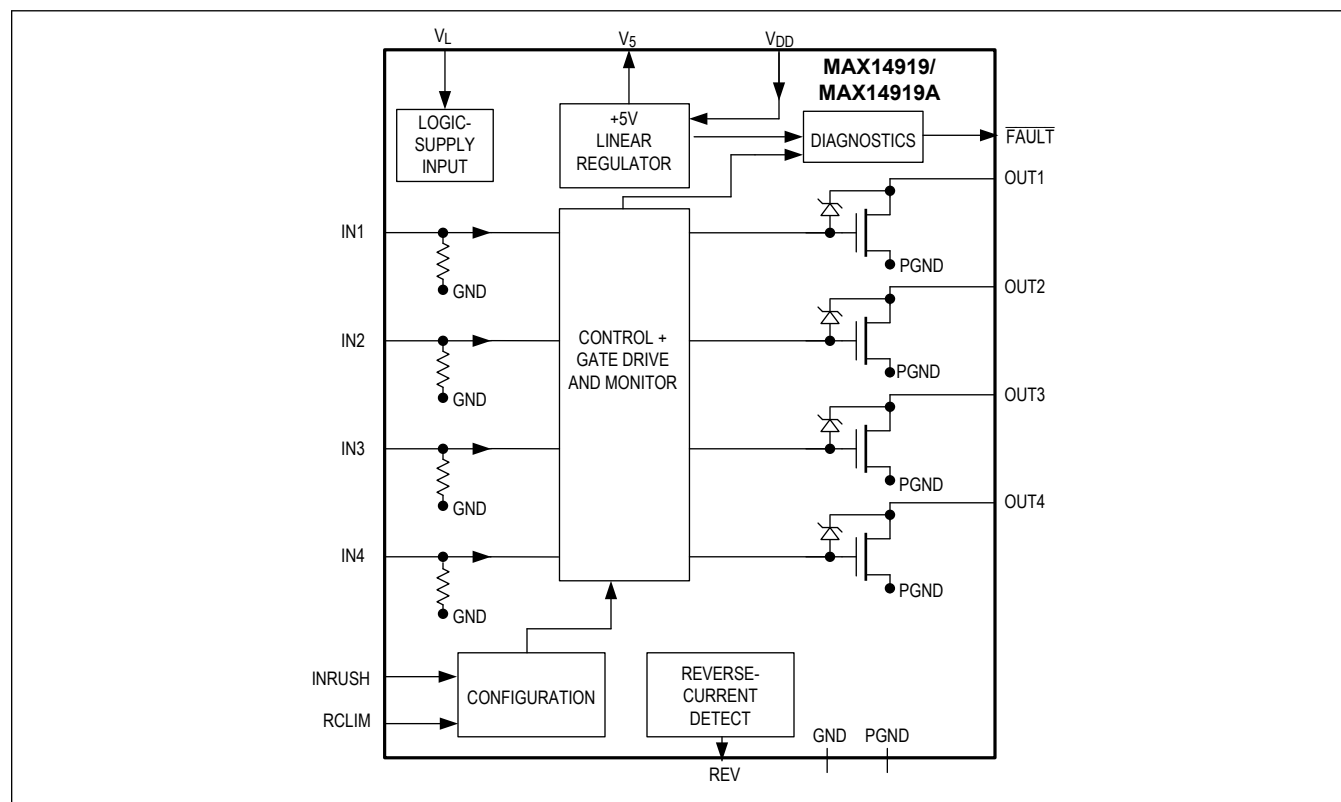


## Pin Description

PIN		NAME	FUNCTION
20 TSSOP	20 TQFN		
POWER SUPPLY			
20	18	V <sub>DD</sub>	24V Supply Input to Linear Regulator. Bypass V <sub>DD</sub> to GND using a 1μF ceramic capacitor. If the MAX14919/ MAX14919A is powered by an external V <sub>5</sub> supply and not V <sub>DD</sub> , the V <sub>DD</sub> input must either be connected to GND or left unconnected.
3, 4, 7, 8	1,2,5,6	PGND	Power Ground. Connect to Exposed Pad (EP).
16	14	GND	Analog Ground. Connect to Exposed Pad (EP).
19	17	V <sub>5</sub>	5V Supply Input or 5V Linear Regulator Output. Bypass V <sub>5</sub> to GND using a 1μF ceramic capacitor. V <sub>5</sub> is the primary chip supply and is required for normal operation
10	8	V <sub>L</sub>	Logic Supply. Connect a supply voltage between 1.6V and 5.5V to V <sub>L</sub> . Connect a 100nF bypass cap to V <sub>L</sub>
SWITCH CONTROL			
18	16	IN1	Switch 1 Control Logic Input. IN1 has a weak pulldown to GND. Drive IN1 high to close the OUT1 switch.
17	15	IN2	Switch 2 Control Logic Input. IN2 has a weak pulldown to GND. Drive IN2 high to close the OUT2 switch.
15	13	IN3	Switch 3 Control Logic Input. IN3 has a weak pulldown to GND. Drive IN3 high to close the OUT3 switch.
14	12	IN4	Switch 4 Control Logic Input. IN4 has a weak pulldown to GND. Drive IN4 high to close the OUT4 switch.
SWITCH OUTPUTS			
2	20	OUT1	Low-Side Switch 1 Output
5	3	OUT2	Low-Side Switch 2 Output
6	4	OUT3	Low-Side Switch 3 Output
9	7	OUT4	Low-Side Switch 4 Output
Configuration			
1	19	INRUSH	Inrush-Enable Logic Input. Drive INRUSH high to enable 2x current limiting for 100mA (min) after any switch is turned on (using IN <sub>_</sub> ). Drive INRUSH low to disable inrush current.
11	9	RCLIM	Load Current-Limit Control Resistor. Connect a resistor between RCLIM and GND to define the maximum load current through each switch. See the <a href="#">Current Limiting</a> section for details.
DIAGNOSTICS SIGNALLING			
12	10	REV	REV Logic Output. Open-drain output with a 45μA internal pullup to V <sub>5</sub> (MAX14919), open-drain output (MAX14919A). On the MAX14919, connect REV to the gate of an external nMOS transistor for supply-load reverse-polarity protection.
13	11	$\overline{\text{FAULT}}$	Global Overload Open-Drain Output. The $\overline{\text{FAULT}}$ transistor turns on low when any of the OUT <sub>_</sub> switches are in thermal overload or the chip is in thermal shutdown. Connect a pullup resistor to V <sub>L</sub> .
EXPOSED PAD			
—	—	EP	Exposed Pad. Connect EP to GND, PGND1, or PGND2.

## Functional Diagrams

## MAX14919/ MAX14919A



## Detailed Description

The MAX14919/MAX14919A is a quad industrial low-side switch. Each low-side switch has 140mΩ (typ) on-resistance at up to 800mA load current. The four switches are pin-controlled, allowing parallel interface and high switching rates of over 200kHz on each channel. The maximum load current allowed through the switches can be set to fit different system needs. The switch outputs are protected against short circuits to voltages in the range of 0V to 49V and are protected against thermal overload. Integrated line-to-GND surge protection of up to ±1kV/42Ω makes external TVS protection unnecessary.

The device offers additional control for protection and diagnostics indicating thermal overload, reverse-load detect,  $V_5$  supply undervoltage, and faults on the RCLIM current-limit setting pin.

The internal active clamps limit the OUT\_ voltage to +55V (typ) enabling fast turn-off of inductive loads.

## Supply Inputs

### Supply Powering Options with $V_{DD}$ and $V_5$

The MAX14919/MAX14919A offers flexible powering options. It can either be powered by  $V_{DD}$  or by  $V_5$ . The  $V_{DD}$  power-supply input is able to support a wide supply-voltage range from +7V to +60V with a typical case of +24V industrial power. The internal low-dropout regulator (LDO) handles the wide input to provide a stable +5V output. Applications with limited available system power or unregulated supplies are able to power MAX14919/MAX14919A without the need of external power converters.

In the presence of a stable +5V external supply, the internal LDO can be bypassed and the MAX14919/MAX14919A only powered by 5V. The  $V_5$  power pin acts as a supply input when  $V_{DD}$  is grounded/unconnected and handles input with +4.5V to +5.5V supplies.  $V_5$  is the primary power supply for the MAX14919/MAX14919A powering the internal control and analog blocks. The internal LDO can be bypassed by either connecting  $V_{DD}$  to GND or by leaving  $V_{DD}$  unconnected.

### 5V Linear Regulator

The integrated 5V linear regulator ( $V_5$ ) can supply up to 30mA load current. Note that linear regulators have high power dissipation when high load currents are drawn while powered from high supply voltage. Calculate the power dissipation in the regulator as  $P_{DIS} (W) = (V_{DD} - V_5) \times I_{V_5}$ . The power dissipation might be excessive for high  $V_5$  load currents in combination with high  $V_{DD}$  supply voltage resulting in self-heating of the device. Verify that the MAX14919/MAX14919A maximum thermal ratings are not exceeded at the highest operating temperatures.

When the device enters thermal shutdown, the  $V_5$  linear regulator is automatically turned off at 160°C. The regulator turns on automatically when the chip temperature drops by 15°C (typ).

### Logic Supply Input $V_L$

The  $V_L$  logic-supply input supports a wide logic-voltage range of +1.62V to +5.5V.  $V_L$  can either be powered by  $V_5$  or externally supplied by +1.8V (typ) or +3.3V (typ) to enable interface with microcontrollers, FPGAs, or digital isolators. This supply input powers internal interface and logic blocks of MAX14919/MAX14919A.

### Undervoltage Lockout

When the  $V_{DD}$ ,  $V_5$ , or  $V_L$  supply voltages are under their respective UVLO thresholds, all OUT\_ switches are off.

### Logic Interface

The logic interface requires a  $V_L$  supply in the range of +1.62V to +5.5V. This ensures that the logic levels on logic I/O pins are CMOS-compliant. If used, connect pullup resistors to the open-drain logic outputs. If not used, connect the open-drain logic outputs to GND.

## FAULT Signaling

$\overline{\text{FAULT}}$  is a global fault indication that is an open drain logic output that transitions active low when the MAX14919/MAX14919A detects a fault condition. When the device exits fault status and all switches are in normal operation, the  $\overline{\text{FAULT}}$  pin transitions passive high.  $\overline{\text{FAULT}}$  is asserted for any of these conditions:

- Chip thermal shutdown
- Any of the OUT switches are in thermal overloads; thus, are turned off.
- Reverse current detected at OUT\_
- $V_5$  UVLO
- Short-circuit detected on the RCLIM pin.

During power-up of the device,  $\overline{\text{FAULT}}$  is asserted until  $V_5$  goes above its undervoltage-lockout condition ( $V_{5\_UVLO}$ ).  $\overline{\text{FAULT}}$  is indicated if any one of the switch output has thermal overload or reverse-load connection, while the other channels are operating normally. The  $\overline{\text{FAULT}}$  output is independent of the IN\_ pin logic.

## Chip Thermal Protection

All switches are constantly monitored while the MAX14919/MAX14919A is powered with  $V_5 > V_{5\_UVLO}$ . When the device chip temperature rises above the thermal shutdown threshold of 150°C ( $T_{CSHDN}$ ), the chip enters thermal shutdown protection and all OUT switches are turned off until the chip temperature drops below 140°C ( $T_{CSHDN} - T_{CSHDN\_HYS}$ ). In this condition, the  $\overline{\text{FAULT}}$  output is set.

If an output switch temperature rises above 160°C (channel thermal-shutdown temperature  $T_{JSHDN}$ ), that switch output (OUTx) is shut off. When the chip temperature falls by the hysteresis amount ( $T_{JSHDN\_HYS}$ ), the OUT\_ switch is restored to normal operation.

The integrated low dropout regulator features a separate temperature sensor that monitors the internal temperature due to the LDO power dissipation. If the internal LDO temperature rises above 160°C ( $T_{DSHDN}$ ) the LDO is turned off. The LDO wakes up after cooling down by ( $T_{CSHDN\_HYST}$ ).

## Current Limiting

The MAX14919/MAX14919A has a settable current limiting common to all four output switches (OUT1 to OUT4). The load current limiting can be set to between 100mA and 800mA depending on the value of the resistor applied at the RCLIM pin.

Connect a resistor ( $R_{LIM}$ ) from RCLIM to GND to set the required current limit. The equation to determine  $R_{LIM}$  for a known current to be limited ( $I_{LIM}$ ) is given by:

$$R_{LIM}(k\Omega) = \frac{V_{CLIM} \times K1}{(I_{LIM} - K2)(mA)}$$

where,

$$V_{CLIM} = 1.2V$$

$$K1 = 17260 \text{ (min), } 18000 \text{ (typ), } 19418 \text{ (max)}$$

$$K2 \text{ (mA)} = -67.1 \text{ (min), } 0 \text{ (typ), } 36.98 \text{ (max)}$$

For example, the  $R_{LIM}$  resistor to ensure the current limit is always higher than 600mA, which is the maximum operating load current of system is:

$$R_{LIM}(k\Omega) = \frac{V_{CLIM} \times K1(\text{min})}{(I_{LIM} - K2(\text{min}))(\text{mA})} = \frac{1.2 \times 17260}{(600 - (-67.1))(\text{mA})} = 31.05k\Omega$$

If no resistor is connected to the RCLIM input (i.e., RCLIM is unconnected) or  $R_{LIM}$  is more than 650k $\Omega$ , the  $I_{LIM}$  is internally set to 800mA. If the  $R_{LIM}$  resistor is less than 6.5k $\Omega$  (typ), all OUT\_ switches are turned off. RCLIM is short-circuit protected.

When the load current is higher than the set  $I_{LIM}$  current in any of the outputs, the device forces the associated switch to limit the current to the  $I_{LIM}$  (mA) value. In current-limit operation, the OUT\_ voltage rises and the OUT\_ switch consequentially heats up proportionally to the  $V_{OUT} \times I_{LIM}$  power dissipation. The limiting is done indefinitely until the

channel is turned-off or the fault condition is removed.

### Inrush Current Mode

The MAX14919/ MAX14919A offers inrush mode that supports loads that draw higher currents during turn-on. In INRUSH mode, each switch provides at least double of the current set by the  $R_{LIM}$  resistor for the INRUSH duration of 10ms (min). Setting the INRUSH logic-input high enables the inrush mode allowing  $2 \times I_{LIM}$  for up to 10ms. After the INRUSH period, the switch current limiting reverts to the value set by  $I_{LIM}$ .

### System Protection

#### Reverse-Current Detection

The MAX14919 and MAX14919A feature reverse current detection which is signaled by the REV logic output. A reverse current on any OUT\_ can arise when the field PSU that powers the load is miswired via a reverse polarity. Reverse currents are drawn out of outputs (OUT\_) when a negative voltage is applied across any OUT\_ and GND/PGND with the OUT\_ switch either in an on or off state. If the reverse current flowing out of any of the OUT\_ exceeds 150mA(typ) ( $I_{TH\_OUT\_REV\_ON}$ ), the REV output immediately transitions low to signal a reverse current condition. The MAX14919 and MAX14919A react differently to a reverse current condition as explained in the following.

The MAX14919 drives REV low and automatically turns off all four OUT\_ switches when it detects a reverse current condition ( $I_{OUT\_} < I_{TH\_OUT\_REV\_ON}$ ). The REV output is held low and all four OUT\_ switches remain off for the autoretry duration ( $t_{REV\_AR}$ ) of 2 seconds (typ). After this delay, the OUT\_ are turned back to the state defined by the IN\_ inputs and REV is pulled high by the 45uA pull-up current. If the cause for reverse current is still present and a reverse current is again detected, the autoretry scheme again turns REV low and forces all OUT\_ off for 2s ( $t_{REV\_AR}$ ). The REV output can drive the gate of an nFET which will open the GND/PGND connection to the field GND/COM connection, thereby stopping the reverse current flow. The on-resistance of the external nFET should be chosen such that it does not contribute significantly to a channel  $R_{ON}$  since all four OUT\_ currents flow through the reverse-protecting nFET. Its  $R_{ON}$  should be significantly less than (1/4)th of the  $R_{ON}$  of the OUT\_ (less than 35m $\Omega$  typ).

The MAX14919A version does not have internal reverse protection and the REV is a real-time open-drain output that signals when a reverse condition is detected. When a reverse current is detected, the open-drain REV output is pulled low but the OUT\_ switches are not turned off – they remain in the state defined by the IN\_. The 2s auto-retry delay ( $t_{REV\_AR}$ ) is not present in MAX14919A, so as soon as the reverse condition disappears, the REV output reverts back to logic high, indicating a return to normal operation. The REV output can be used as an indication for a reverse condition, for example to an LED or to MCU, but is not suitable for driving an nFET in GND/PGND path for protection purposes.

Note the following when using the MAX14919. When the load driven by an OUT\_ is capacitive and if the load is connected via a length of wire that has inductance, turning on the OUT\_ will result in brief current and voltage oscillations on the wire due to LC oscillation. If the currents during oscillation exceeds the reverse trigger level of 150mA(typ) ( $I_{TH\_OUT\_REV\_ON}$ ), then this is detected as a reverse current. The MAX14919 will force all the channels off for autoretry time ( $t_{REV\_AR}$ ) for protection. In the same scenario, the MAX14919A will indicate a reverse detection fault (REV will be forced low) for the time until reverse current is present and will not change the state of output channels OUT\_.

#### Transient Energy Protection

The MAX14919/ MAX14919A features an integrated clamp at each of its four channel outputs. In typical applications, the integrated clamp avoids an external clamp on each of its outputs reducing component cost and board space. In case of an overvoltage event caused by surge, ESD, or inductive load turn-off, the clamp turns on at +55V (typ) to dissipate the energy.

#### Short-Circuit and Overcurrent Protection

The device outputs are designed to handle hard short-circuits as well as overcurrents. In case of a short-circuit at OUT\_ to field supply with the switch turned on, the device actively regulates the current to  $I_{LIM}$ . The shorted switch channel temperature increases at a rate determined by the power dissipation: OUT\_ voltage  $\times I_{LIM}$ . The switch enters thermal shutdown when its temperature is greater than 160°C. After the device cools down by  $T_{JSHDN\_HYS}$  (°C), the switch is automatically turned on if its associated IN\_ input is high. The MAX14919/ MAX14919A switch outputs indefinitely cycle into and out of thermal shutdown until the switch is turned off or the short-circuit is removed.

## Applications Information

### Paralleling the Outputs

The MAX14919/MAX14919A device supports paralleling of channels in applications with a higher load-current requirement. The channels that are paralleled should be connected together at the output and input, respectively. When multiple outputs are connected in parallel, the resulting current limit is the sum of the each output's current limit. For example, paralleling of two channels doubles the available load current.

When multiple outputs OUT\_ are paralleled, an external zener-diode (ZD) clamp might be required per output for quenching the energy during inductive load turnoff. The external ZD-clamp voltage must be lower than the minimum internal-clamp voltage (49V min).

### Board Layout

High-current, low  $R_{ON}$  switches require proper layout and design procedures for optimum performance. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Ensure that the PGND and GND pins are interconnected to have the least on-board resistance. In this case, a 1 $\mu$ F capacitor should be placed to the ground plane as close to the V<sub>DD</sub> pin as possible.

Connect the exposed pad to a large GND plane to dissipate heat in case of large load currents. Either the top layer or an inner or the bottom PCB layer is used for heat conduction. Use many vias under the exposed pad ("via farm") to efficiently contact the inner and bottom layers.

### Surge Protection

Each OUT\_ (OUT1 to OUT4) of the MAX14919/MAX14919A is protected against IEC 61000-4-5 (1.2 $\mu$ s/ 50 $\mu$ s) surges of up to  $\pm 1\text{kV}/(42\Omega + 0.5\mu\text{F})$  without the need for external protection diodes from OUT\_ to PGND.

### Inductive Demagnetization

During turn-off of inductive loads by an OUT\_ low-side switch, the kickback voltage generated by the inductance is clamped by the internal clamp to a voltage of +55V (typ) relative to PGND allowing fast demagnetization. Large load inductance and higher load currents in the inductive load increase the time until the inductance is demagnetized. This increases the energy in the clamp; hence, the internal temperature of MAX14919/MAX14919A and can result in a thermal overload with FAULT set low. Since large energy is dissipated in the device through the voltage clamp, the user must design the system keeping in mind the inductance of the load and its operating current. Failure to do so results in damage to the device.

Each switch is able to dissipate up to 200mJ of clamp energy during inductive load clamping at +125°C junction temperature (T<sub>J</sub>).

## Isolated Quad-Channel Digital-Output Application with Reverse-Load Polarity Protection

The schematic diagram illustrates a power management system for a video camera, centered around three integrated circuits: the MAX258, MAX14483, and MAX14919.

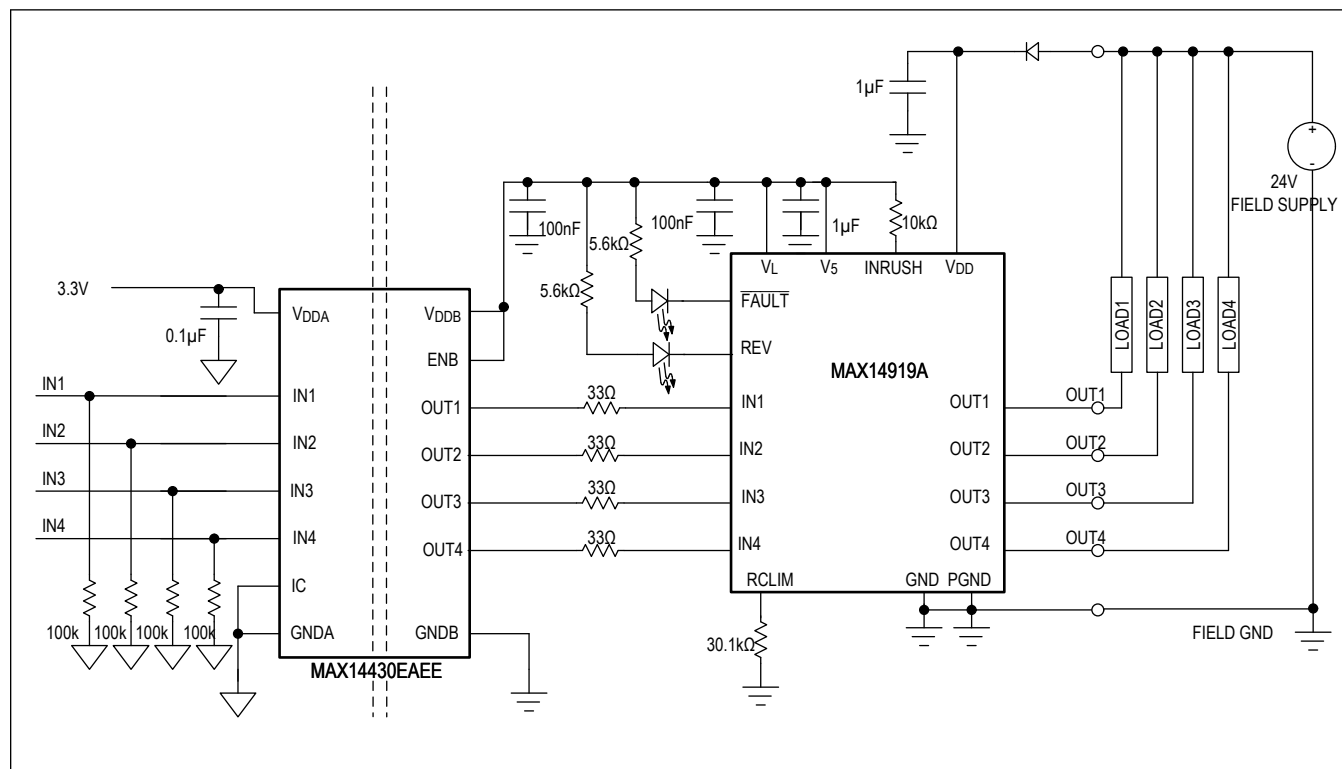
**MAX258 (Top Left):** This IC is responsible for power regulation. It has a  $3.3V_{IN}$  input, a  $1\mu F$  input capacitor, and a  $10\mu F$  output capacitor. It is connected to a transformer with a 1CT:3CT ratio. The output of the transformer is connected to a diode bridge rectifier, which is then connected to a  $1\mu F$  capacitor. The MAX258 is also connected to a  $10k\Omega$  resistor and a  $0.1\mu F$  capacitor.

**MAX14483 (Bottom Left):** This IC is a multi-channel voltage detector. It has four input channels (IN1, IN2, IN3, IN4) and four output channels (OUT1, OUT2, OUT3, OUT4). It is connected to a  $25k\Omega$  resistor and a  $1\mu F$  capacitor. The output of the MAX14483 is connected to a  $10k\Omega$  resistor and a  $0.1\mu F$  capacitor.

**MAX14919 (Right):** This IC is a multi-channel voltage detector. It has four input channels (IN1, IN2, IN3, IN4) and four output channels (OUT1, OUT2, OUT3, OUT4). It is connected to a  $25k\Omega$  resistor and a  $1\mu F$  capacitor. The output of the MAX14919 is connected to a  $10k\Omega$  resistor and a  $0.1\mu F$  capacitor.

**Power Supply and Grounding:** The system is powered by a  $24V$  FIELD SUPPLY. The ground is connected to COM/ FIELD GND. The MAX258 is connected to  $V_{DD}$ ,  $HICLK$ ,  $EN$ , and  $GND/PGND$ . The MAX14483 is connected to  $V_{DDB}$ ,  $SAA$ ,  $IRDY$ ,  $IFAULT$ ,  $ISDO$ ,  $OAUX$ ,  $OSDI$ ,  $OSCLK$ ,  $ICS$ ,  $SDOEN$ ,  $GNDDB$ , and  $GNCDA$ . The MAX14919 is connected to  $V_L$ ,  $V_5$ ,  $V_{DD}$ ,  $FAULT$ ,  $INRUSH$ ,  $IN1$ ,  $IN2$ ,  $IN3$ ,  $IN4$ ,  $OUT1$ ,  $OUT2$ ,  $OUT3$ ,  $OUT4$ ,  $RCLIM$ ,  $REV$ ,  $GND$ , and  $PGND$ .

This [Typical Application Circuit](#) illustrates an isolated quad-channel low-side digital output with 600mA current limit. The MAX14919A is powered from +24V field supply. The internal +5V V<sub>5</sub> output is connected to the VL logic supply input of the MAX14919A and the MAX14430 isolator. The MAX14430 enables a +3.3V to +5V interface while providing 3kV<sub>RMS</sub> isolation.



PART NUMBER	TEMP RANGE	PIN-PACKAGE
<b>MAX14919AUP+</b>	-40°C to +125°C	20 TSSOP-EP*
MAX14919AUP+T	-40°C to +125°C	20 TSSOP-EP*
MAX14919ATP+	-40°C to +125°C	20 TQFN-EP*
MAX14919ATP+T	-40°C to +125°C	20 TQFN-EP*
<b>MAX14919AAUP+**</b>	-40°C to +125°C	20 TSSOP-EP*
MAX14919AAUP+T**	-40°C to +125°C	20 TSSOP-EP*
MAX14919AATP+	-40°C to +125°C	20 TQFN-EP*
MAX14919AATP+T	-40°C to +125°C	20 TQFN-EP*

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Release for Market Intro	—
1	2/21	Updated the <i>General Description, Benefits and Features, Absolute Maximum Ratings, Package Description, Pin Configurations</i> , and <i>Reverse-Current Detection</i> sections; removed future product designation from MAX14919ATP+ and added MAX14919AAUP+ and MAX14919AAUP+T as future parts in the <i>Ordering Information</i>	1–2, 8, 13, 16
2	5/21	Added MAX14919A, updated <i>General Description, Benefits and Features, Simplified Low-Side Switch Application, Electrical Characteristics</i> table, TOCs 15, 16, 17, 18 and added TOC19, <i>Pin Configurations, Pin Description, Functional Diagrams, Detailed Description, Supply Powering Options with <math>V_{DD}</math> and <math>V_S</math>, FAULT Signaling, Chip Thermal Protection, Current Limiting, Inrush Current Mode, Reverse-Current Detection, Transient Energy Protection, Paralleling the Outputs, Surge Protection, Inductive Demagnetization, Isolated Quad-Channel Digital-Output Application with Reverse-Load Polarity Protection, Field Isolated Quad-Channel Digital Output Application with MAX14919A, and Ordering Information</i>	1–19

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