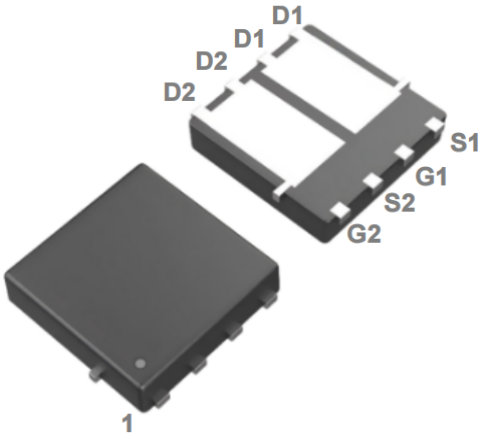
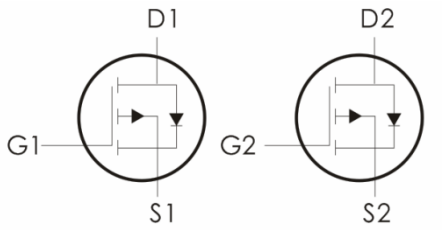
Description：

This Dual P-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.





Features：

1) V_{DS}=-20V,I_D=-12A,$R_{DS(ON)}$<16mΩ @V_{GS}=-4.5V（Typ：12 mΩ）
2) Low gate charge.
3) Green device available.
4) Advanced high cell denity trench technology for ultra low $R_{DS(ON)}$.
5) Excellent package for good heat dissipation.

Package Marking and Ordering Information：

Part NO.	Marking	Package	Packing
DOZ12DP02	12DP02	DFN3*3-8D	5000 pcs/Reel

Absolute Maximum Ratings： (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	±12	V
I_D	Continuous Drain Current	-12	A
	Continuous Drain Current-T_C=100℃[1]	-50	
P_D	Power Dissipation	15	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	℃

Thermal Characteristics：

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance,Junction to Ambient[2]	4.5	℃/W

Electrical Characteristics: (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	-20	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=-12V	---	---	-1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	-0.4	-0.65	-1	V
$R_{DS(ON)}$	Drain-Source On Resistance	V_{GS}=-4.5V,I_D=-6A	---	12	16	mΩ
		V_{GS}=-2.5V,I_D=-5A	---	17	24	mΩ
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=-6V, V_{GS}=0V, f=1MHz	---	1730	---	pF
C_{oss}	Output Capacitance		---	320	--	
C_{rss}	Reverse Transfer Capacitance		---	210	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-6V, I_D=-1A, R_L=6Ω ,V_{GS}=-4.5V， R_g=6Ω	---	20	---	ns
t_r	Rise Time		---	35	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	90	---	ns
t_f	Fall Time[2]		---	70	---	ns
Q_g	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-6V, I_D=-6A	---	19.5	---	nc
Q_{gs}	Gate-Source Charge		---	4.1	---	nc
Q_{gd}	Gate-Drain “Miller” Charge		---	5.2	---	nc
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage[3]	V_{GS}=0V, I_{SD}=-1A	---	---	-1.2	V
I_S	Continuous Drain Curren[2]	V_D=V_G=0V	---	---	-12	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Characteristics: (T_C=25℃ unless otherwise noted)

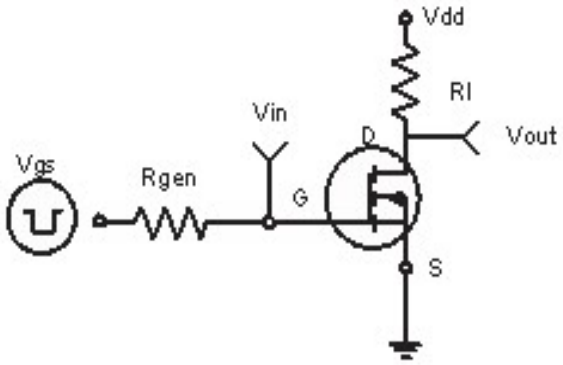


Figure 1:Switching Test Circuit

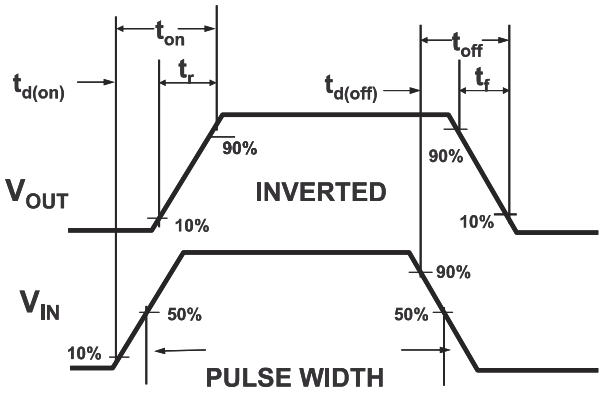
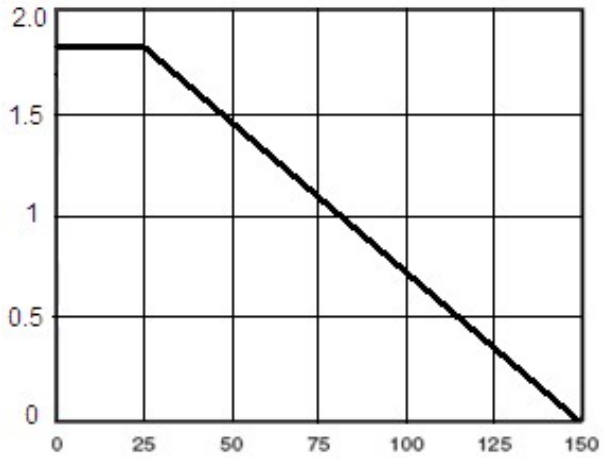
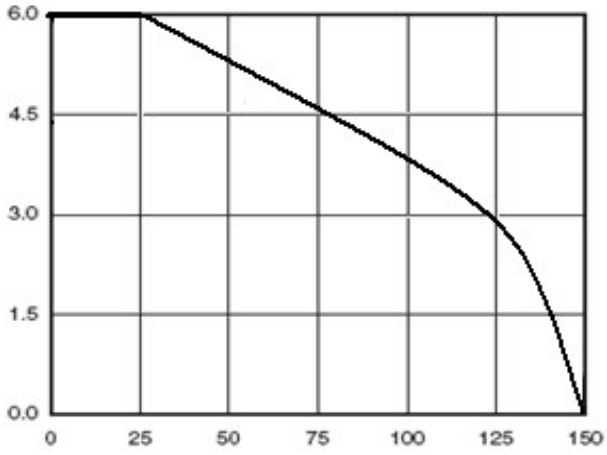


Figure 2:Switching Waveforms



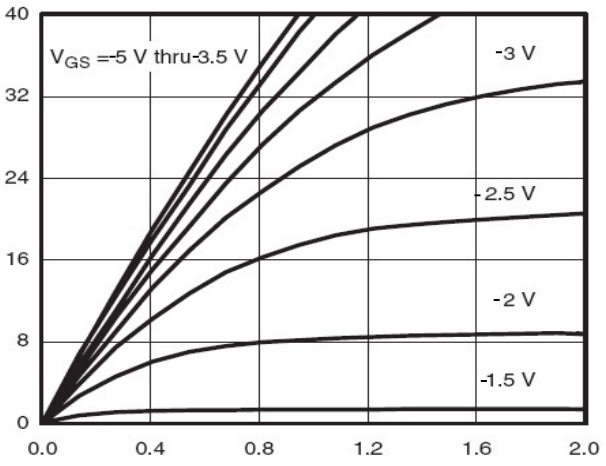
T_J-Junction Temperature(℃)

Fi gure3 P owerDi ssi pati on



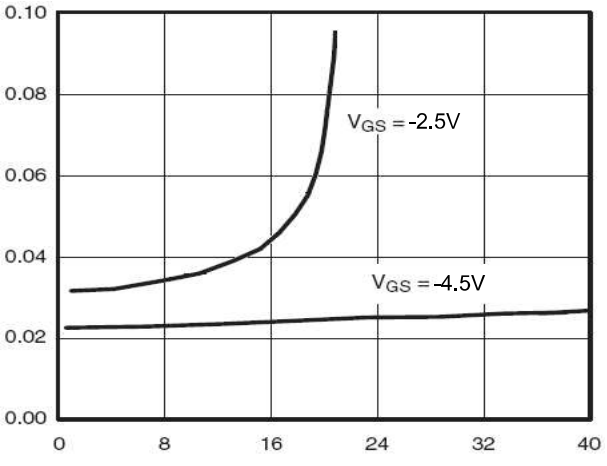
T_J-Junction Temperature(℃)

Figure 4 Drain Current



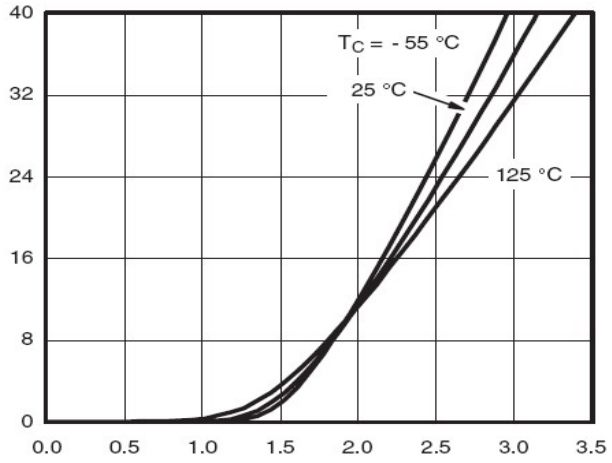
Vds Drain-Source Voltage (V)

Figure 5 Output Characteristics



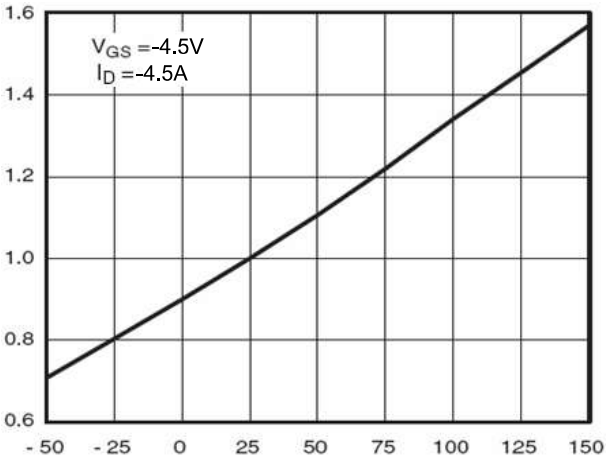
I_D- Drain Current (A)

Figure 6 Drain-Source On-Resistance



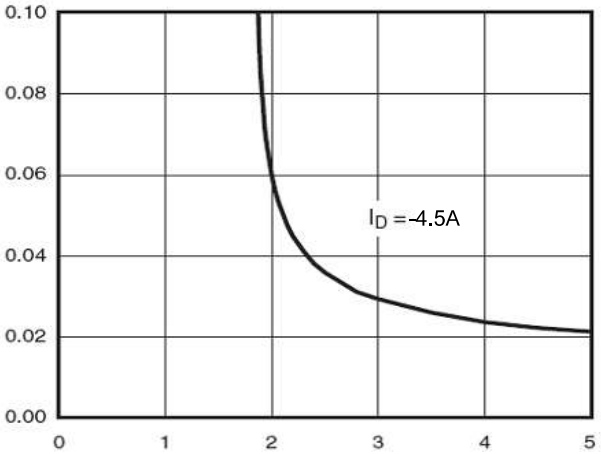
Vgs Gate-Source Voltage (V)

Figure 7 Transfer Characteristics



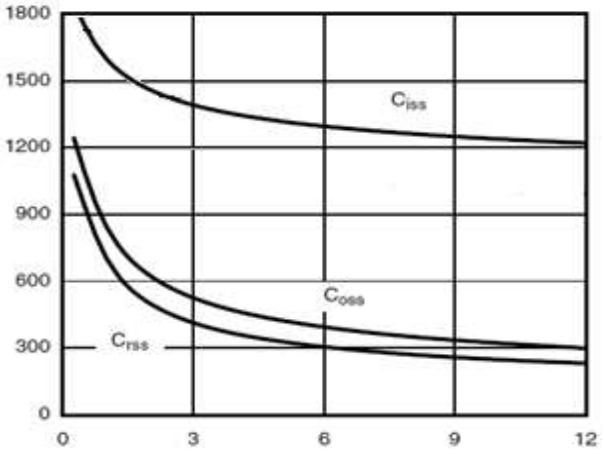
T_J-Junction Temperature(℃)

Figure 8 Drain-Source On-Resistance



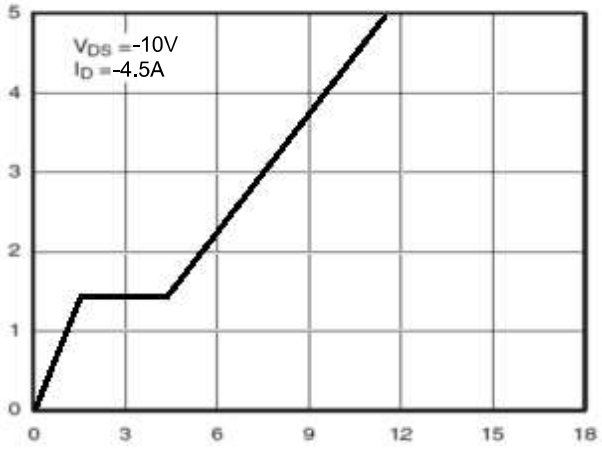
Vgs Gate-Source Voltage (V)

Figure 9 Rdson vs Vgs



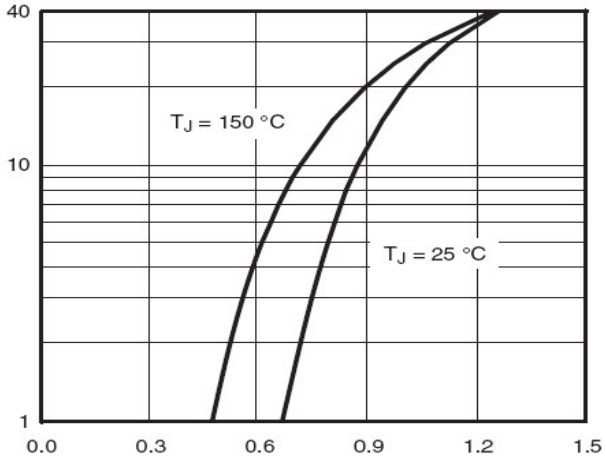
Vds Drain-Source Voltage (V)

Figure 10 Capacitance vs Vds



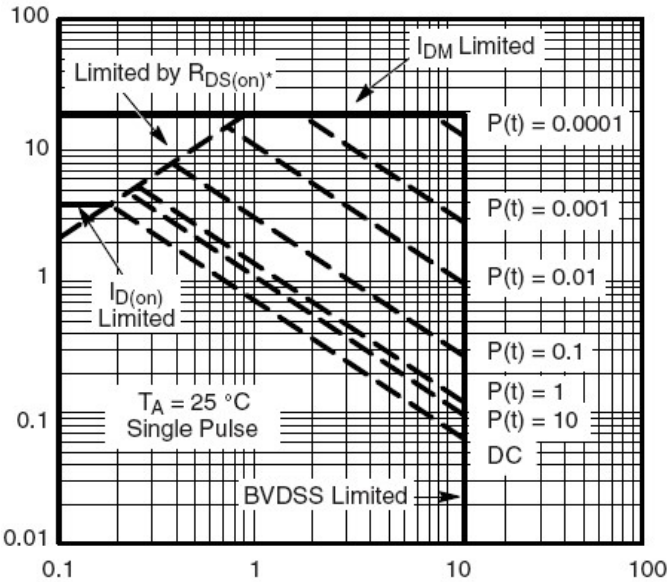
Qg Gate Charge (nC)

Figure 11 Gate Charge



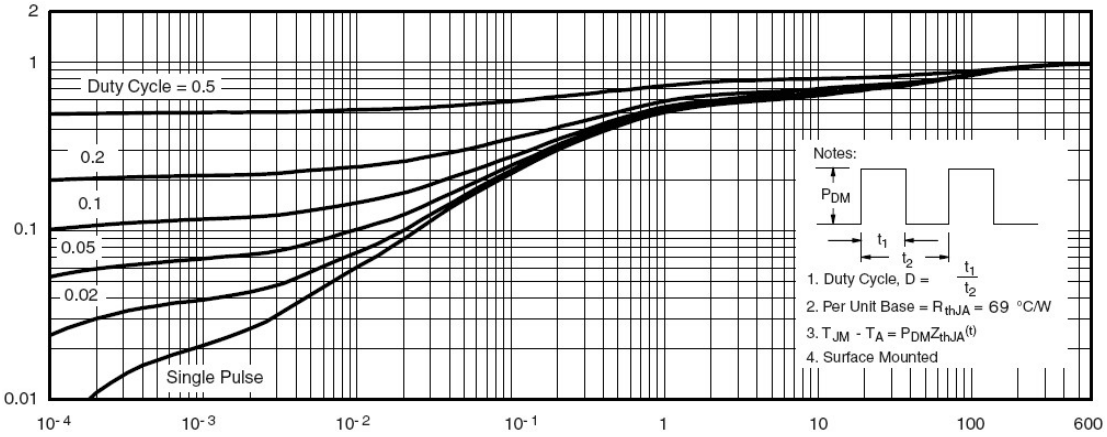
Vsd Source-Drain Voltage (V)

Figure 12 Source- Drain Diode Forward



Vds Drain-Source Voltage (V)

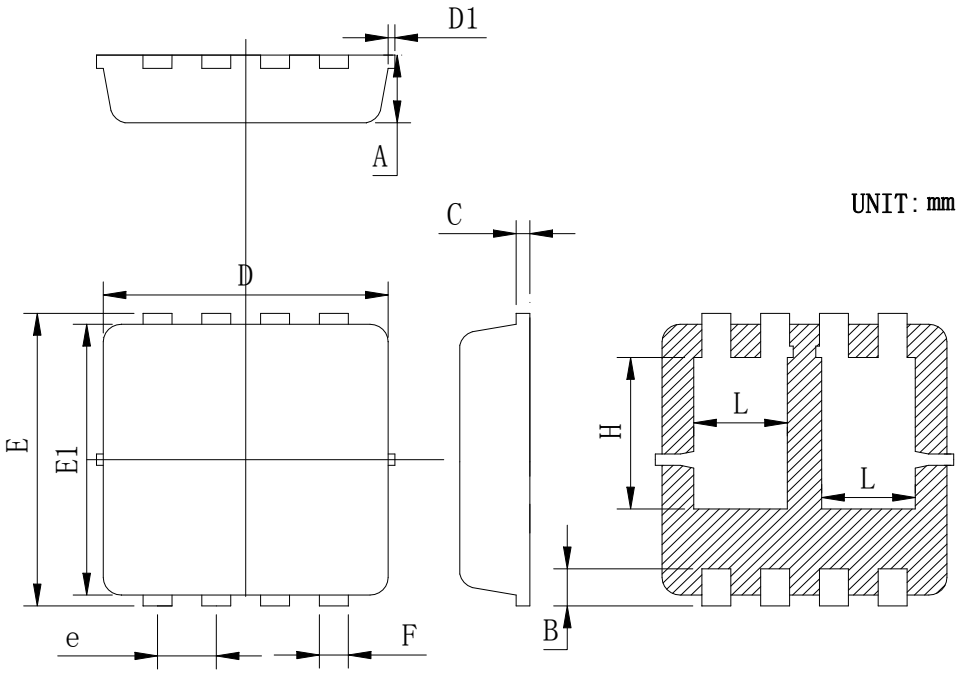
Figure 13 Safe Operation Area



Square Wave Pluse Duration(sec)

Figure 14 Normalized Maximum Transient Thermal Impedance

DFN3X3-8D Package Outline Data



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

Marking Information：

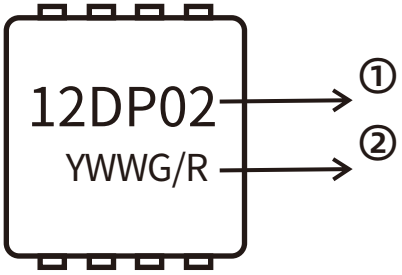
①: Part NO.

②: Date Code (YWWG / R)

Y: Year Code , last digit of the year

WW : Week Code (01-53)

G/R: G(Green) /R(Lead Free)



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2024-06-16	Release of final version

Attention:

Information furnished in this document is believed to be accurate and reliable. However, Shenzhen Doingter Semiconductor Co.,Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Shenzhen Doingter complies with the agreement. Products and information provided in this document have no infringement of patents. Shenzhen Doingter assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied. Is a registered trademark of Shenzhen Doingter Semiconductor Co.,Ltd.