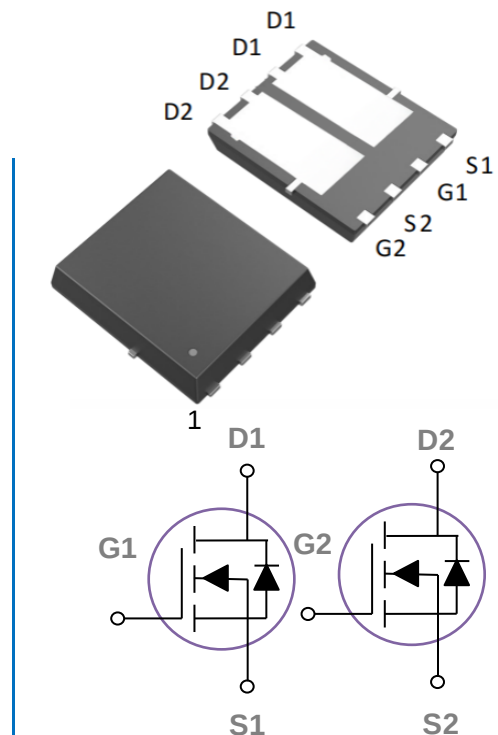


Description:

These Dual N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Features:

- 1) $V_{DS}=60V, I_D=40A, R_{DS(ON)} < 17m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(ON)}$.
- 5) Excellent package for good heat dissipation.



Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current- $T_C=25^\circ C$	40	A
	Continuous Drain Current- $T_C=100^\circ C$	29	A
I_{DM}	Pulsed Drain Current ³	190	A
P_D	Power Dissipation	56	W
E_{AS}	Single pulse avalanche energy ¹	98	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.23	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	$^\circ C/W$

Package Marking and Ordering Information:

Part NO.	Marking	Package
DON40DN06	40DN06	DFN5*6-8D

Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Sourtce Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	60	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	---	---	1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} = ± 20V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	GATE-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	1.2	1.8	2.5	V
R _{DS(ON)}	Drain-Source On Resistanc	V _{GS} =10V, I _D =20A	---	13.5	17	m Ω
		V _{GS} =4.5V, I _D =20A	---	18	23	m Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	---	1899	---	pF
C _{oss}	Output Capacitance		---	113	---	
C _{rss}	Reverse Transfer Capacitance		---	92	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	VDD=30V, V _{GS} =10V R _{GEN} =3 Ω , I _D =20A	---	13	---	ns
t _r	Rise Time		---	25	---	ns
t _{d(off)}	Turn-Off Delay Time		---	60	---	ns
t _f	Fall Time		---	9	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =20A	---	40	---	nC
Q _{gs}	Gate-Source Charge		---	7.8	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	8.3	---	nC
Drain-Source Diode Characteristics						
I _S	Continuous Source Current	VG=VD=0V	---	---	40	A
I _{sm}	Pulsed Source Current	VG=VD=0V	---	---	190	A

V_{SD}	Diode Forward Voltage	V _{GS} =0V , I _D =20A , V _{GS} =0V	---	---	1.2	V
T_{rr}	Reverse Recovery Time	I _F =20A , dI/dt=100A/μs ,	---	29	---	ns
Q_{rr}	Reverse Recovery Charge		---	21	---	nC

Notes:

- 1) L=0.5mH, V_{DD}=30V, Start T_J=25°C.
- 2) Limited by maximum junction temperature.
- 3) Repetitive Rating: Pulse width limited by maximum junction temperature.

Typical Characteristics:

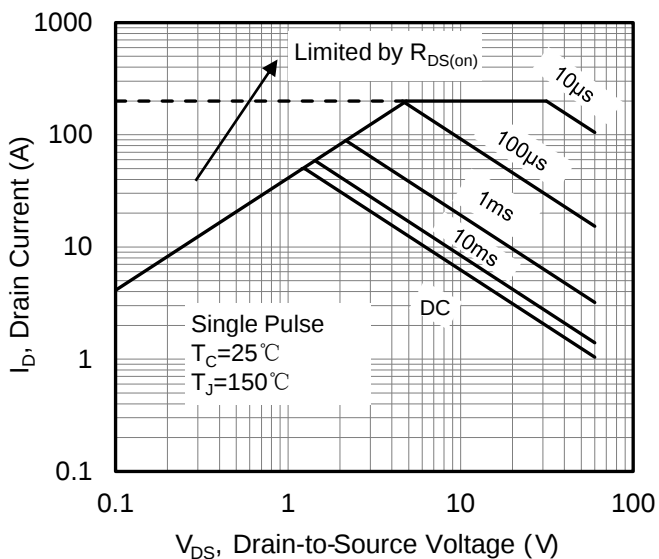


Figure 1. Maximum Safe Operating Area

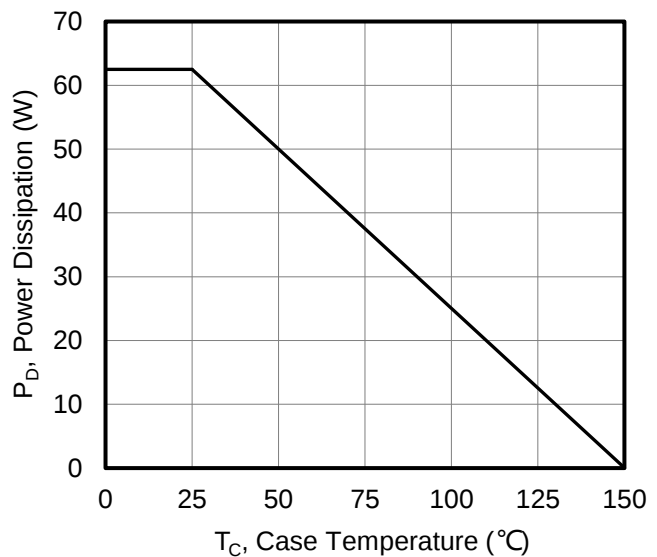


Figure 2. Maximum Power Dissipation vs. Case Temperature

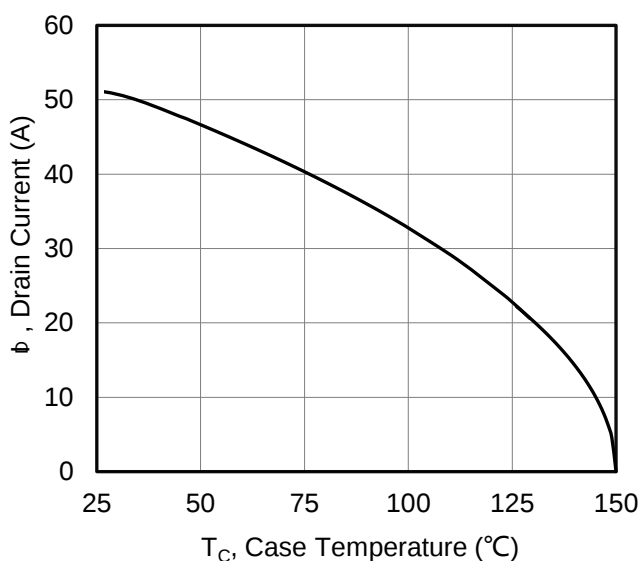


Figure 3. Maximum Continuous Drain Current vs. Case Temperature

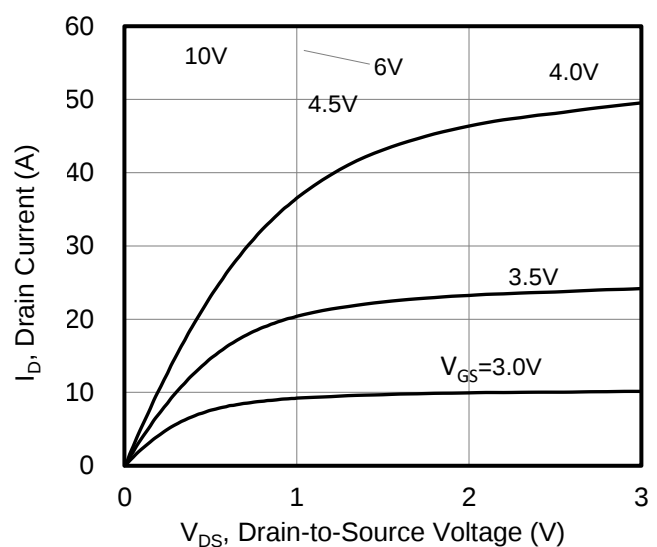


Figure 4. Typical output Characteristics

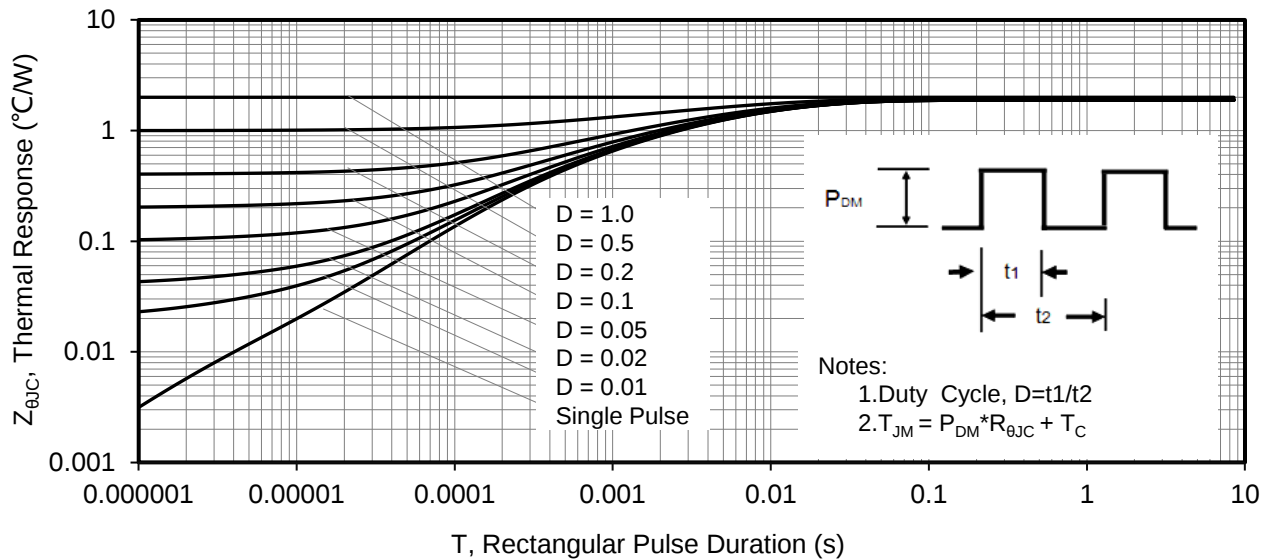


Figure 5. Maximum Effective Thermal Impedance, Junction to Case

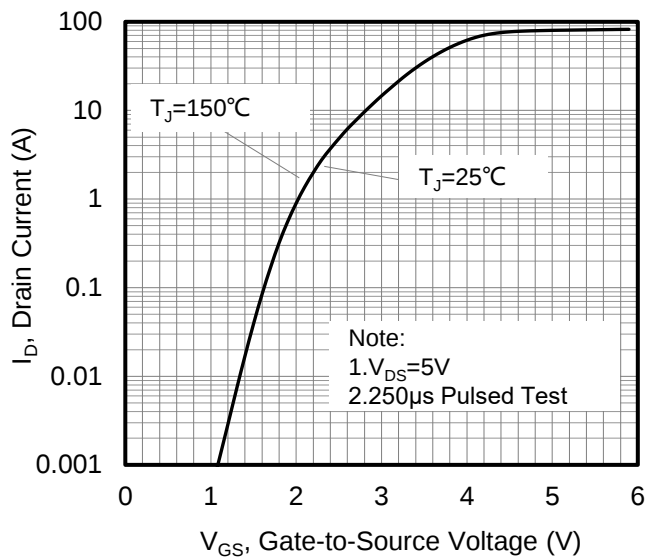


Figure 6. Typical Transfer Characteristics

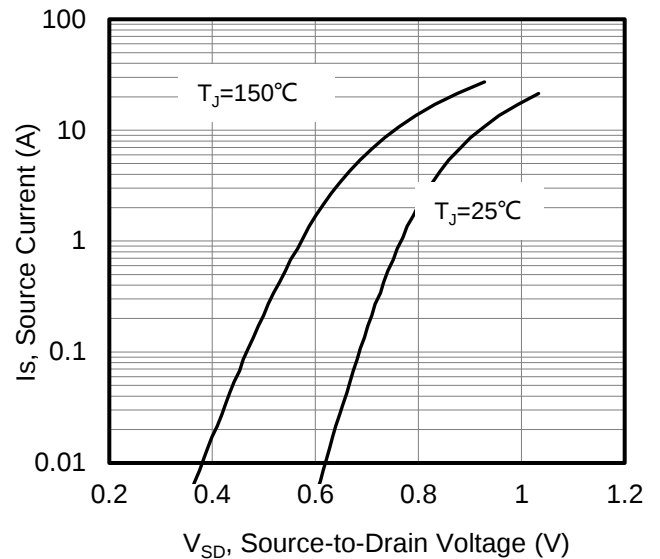


Figure 7. Typical Body Diode Transfer Characteristics

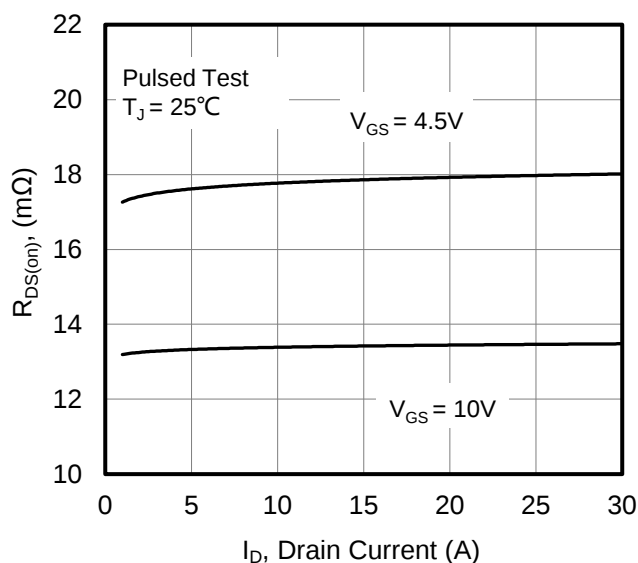


Figure 8. Drain-to-Source On Resistance vs Drain Current

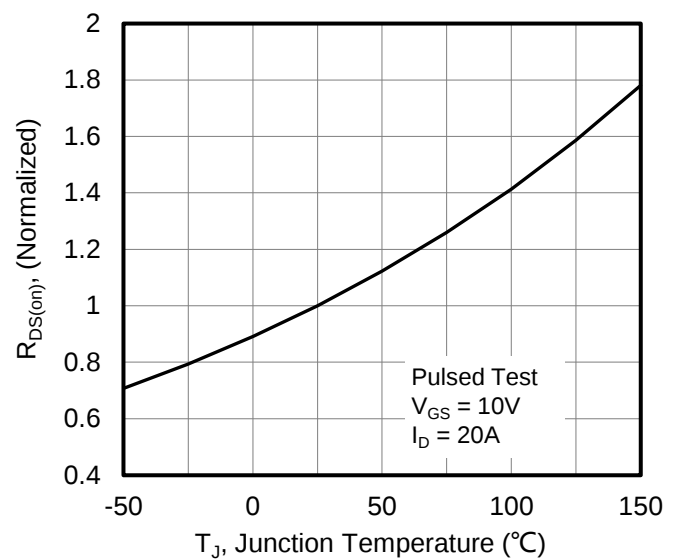


Figure 9. Normalized On Resistance vs Junction Temperature

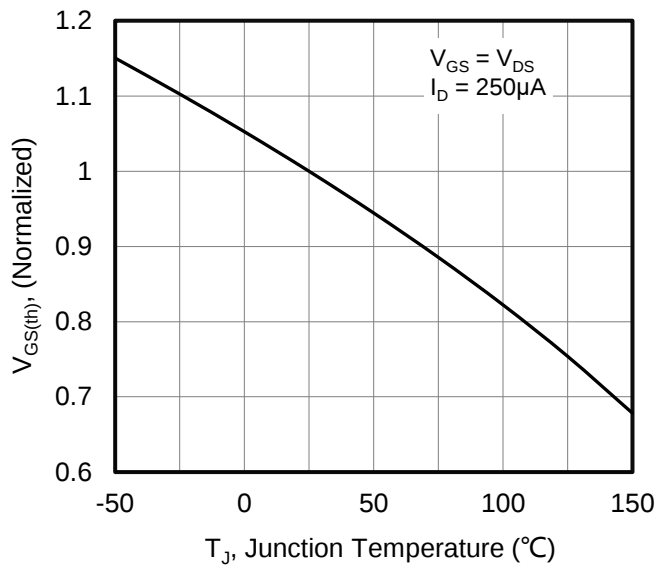


Figure 10. Normalized Threshold Voltage vs Junction Temperature

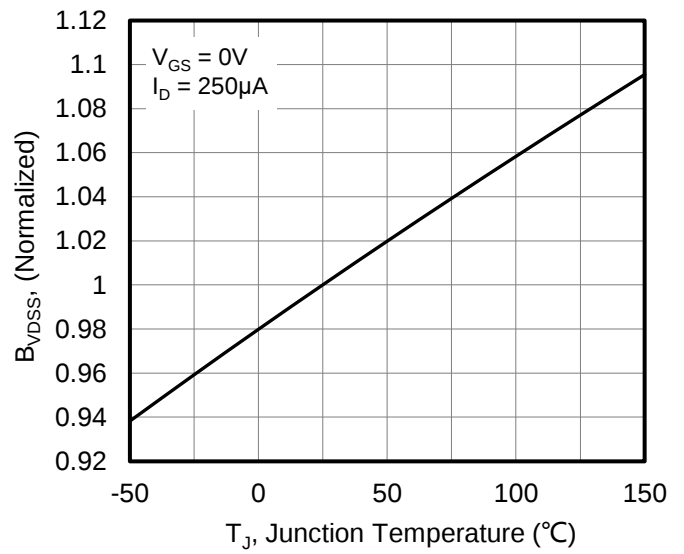


Figure 11. Normalized Breakdown Voltage vs Junction Temperature

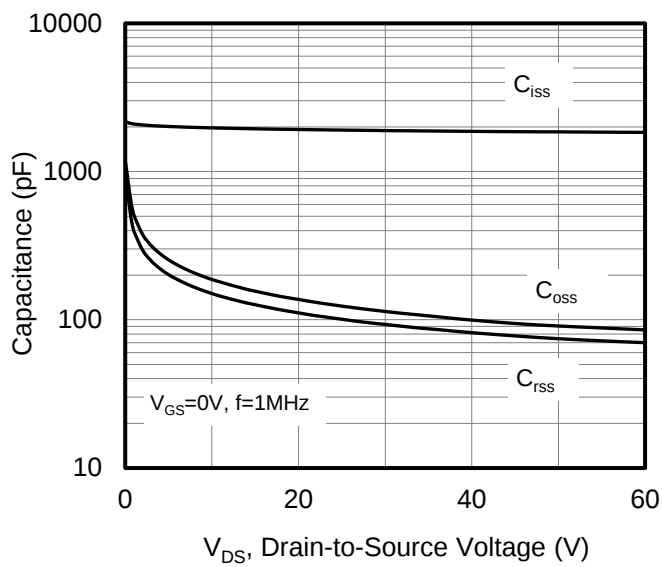


Figure 12. Capacitance Characteristics

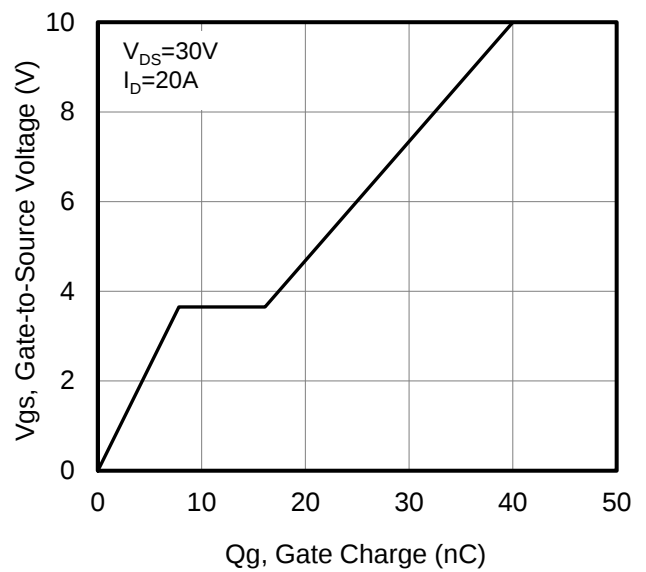


Figure 13. Typical Gate Charge vs Gate to Source Voltage