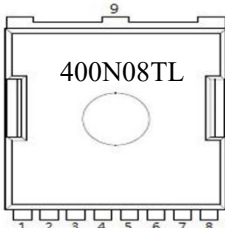
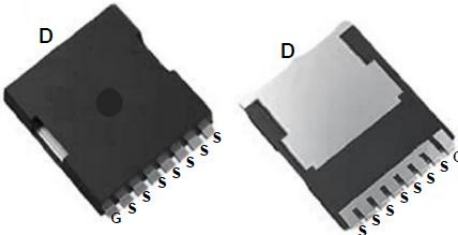
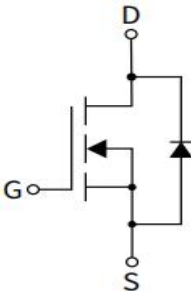


Features	Bvdss	Rdson	ID
	80V	1.05mΩ	400A
➤ Split Gate Trench MOSFET technology ➤ Excellent package for heat dissipation ➤ High density cell design for low RDS(ON)	Application ➤ DC-DC Converters ➤ Power management functions ➤ Synchronous-rectification applications		

Package			
   <tr><td>Marking and pin assignment</td><td>TOLL-8L top view</td><td>Schematic diagram</td></tr>	Marking and pin assignment	TOLL-8L top view	Schematic diagram
Marking and pin assignment	TOLL-8L top view	Schematic diagram	

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
400N08TL	S400N08TL	TOLL-8L	2000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}\text{C}$	I_D	400	A
	$T_C = 100^{\circ}\text{C}$	I_D	253	A
Pulsed Drain Current ¹		I_{DM}	1600	A
Power Dissipation	$T_C = 25^{\circ}\text{C}$	P_D	468.8	W
Single Pulse Avalanche Energy ²		EAS	1280	mJ
Junction Temperature		T_J	-55~+175	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55~+175	$^{\circ}\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient ³	$R_{\theta JA}$	39	$^{\circ}\text{C/W}$
Thermal Resistance Junction-Case	$R_{\theta JC}$	2.5	$^{\circ}\text{C/W}$



Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HLS400N08TL	TOLL-8	1	9	2,3,4,5,6,7,8	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	80	-	-	V
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	$T_C = 25^{\circ}\text{C}$ I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	μA
Zero Gate Voltage Drain Current	$T_C = 100^{\circ}\text{C}$ I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$	-	-	100	μA
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2	3	4	V
Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	1.05	1.35	$m\Omega$
Forward Trans-conductance ⁴	g_{fs}	$V_{GS} = 10V, I_D = 20A$	--	62	-	S
Input Capacitance	C_{ISS}	$V_{DS} = 40V, V_{GS} = 0V,$ $f = 1MHz$	-	13085	-	pF
Output Capacitance	C_{OSS}		-	2615	-	
Reverse Transfer Capacitance	C_{RSS}		-	120	-	
Gate Resistance	R_g	$f = 1MHz$	-	3.1	-	Ω
Total Gate Charge	Q_g	$V_{DS} = 40V, I_D = 20A, V_{GS} = 10V$	-	243.6	-	nC
Gate-Source Charge	Q_{gs}		-	64.2	-	
Gate-Drain Charge	Q_{gd}		-	58.8	-	
Turn-On Delay Time	$T_{d(on)}$	$V_{DD} = 40V, I_D = 20A, R_{GEN} = 3\Omega,$ $V_{GS} = 10V$	-	44.8	-	ns
Rise Time	T_R		-	86.8	-	
Turn-Off Delay Time	$T_{d(off)}$		-	164	-	
Fall Time	T_F		-	94	-	
Continuous Source Current	I_S	$T_C = 25^{\circ}\text{C}$	-	-	400	A
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 20A$	-	-	1.2	V
Reverse Recovery time	T_{rr}	$IF = 20A, dI/dt = 100A/\mu s$	-	128	-	ns
Reverse Recovery Charge	Q_{rr}		-	140.8	-	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 175^{\circ}\text{C}$.
2. The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.4mH, I_{AS} = 80A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, The value in any given application depends on the



user's specific board design.

4. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

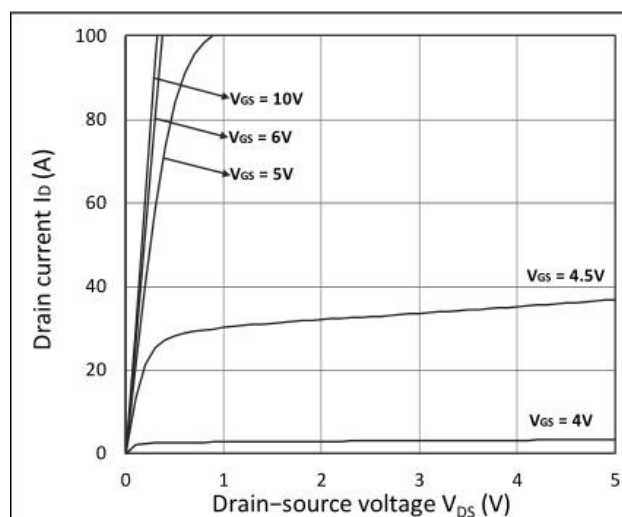


Figure 1. Output Characteristics

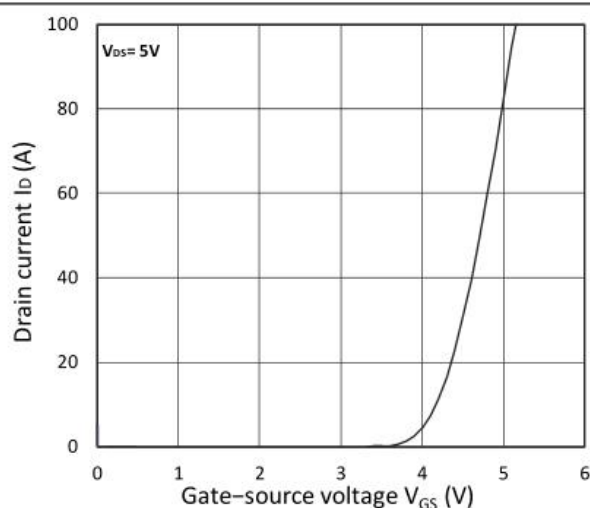


Figure 2. Transfer Characteristics

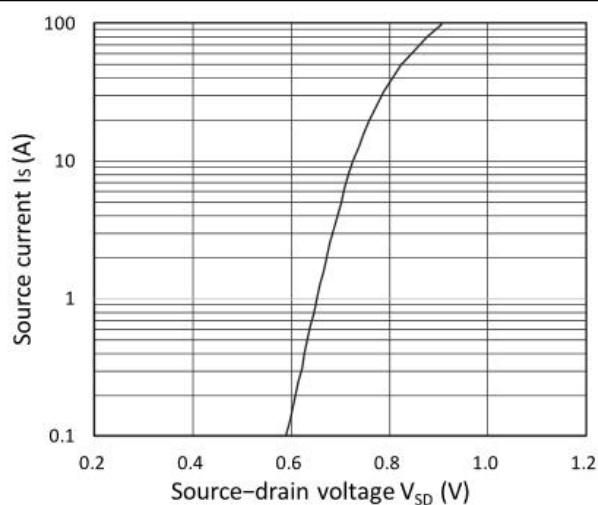


Figure 3. Forward Characteristics of Reverse

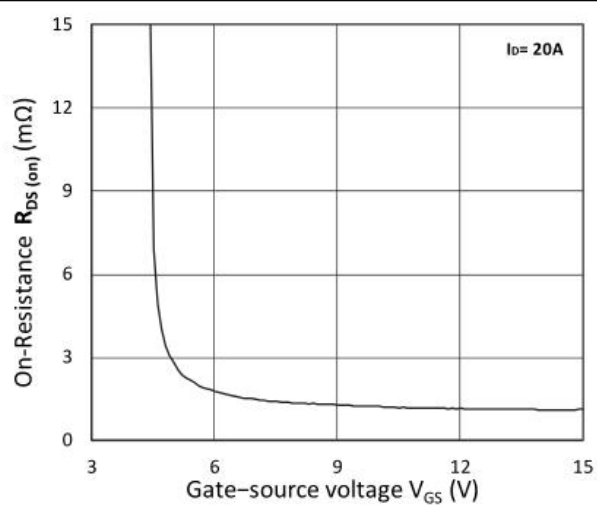


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

Typical Characteristics

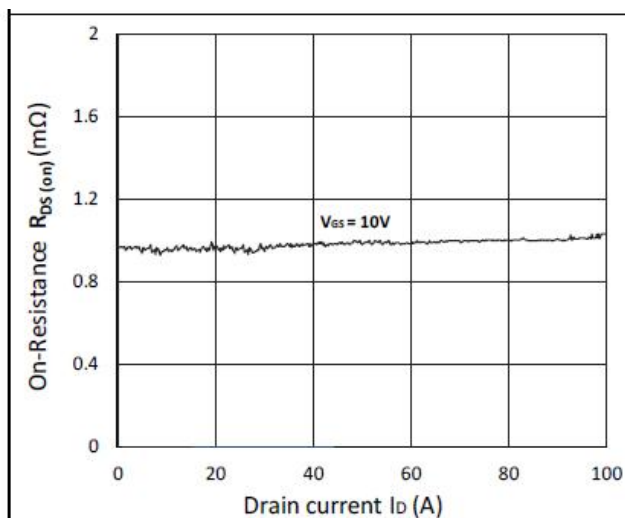


Figure 5. $R_{DS(on)}$ vs. I_D

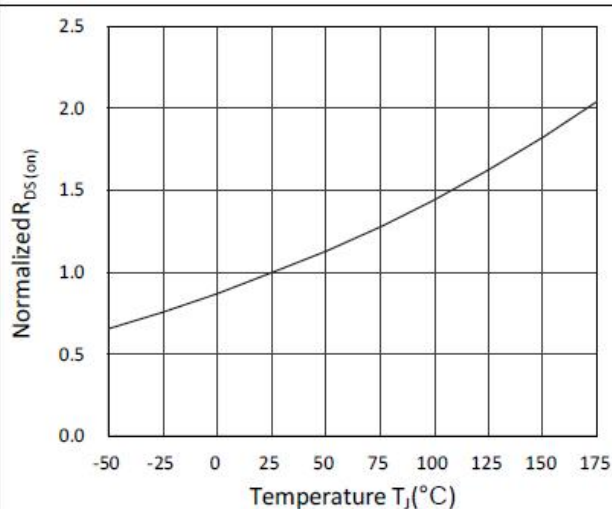


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

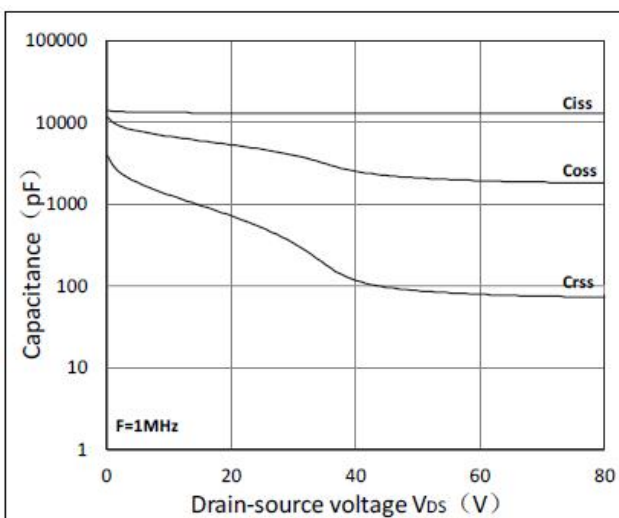


Figure 7. Capacitance Characteristics

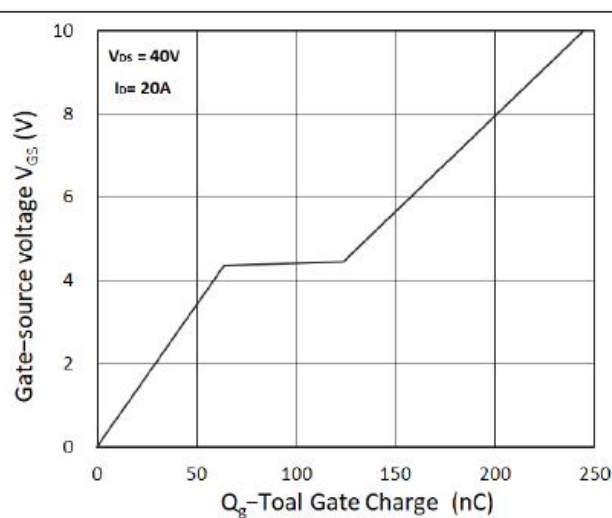


Figure 8. Gate Charge Characteristics

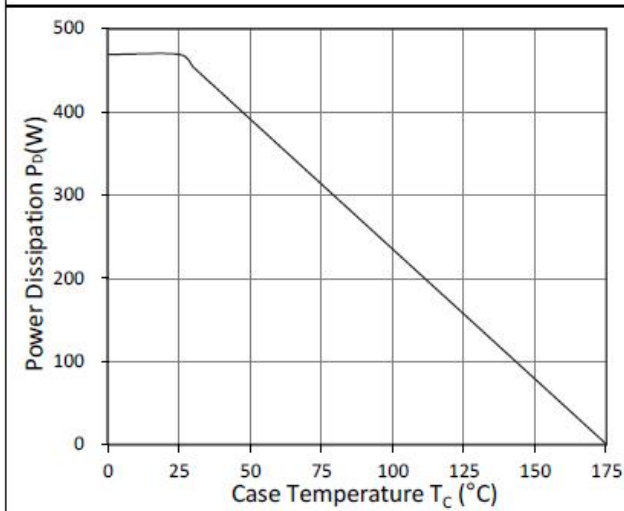


Figure 9. Power Dissipation

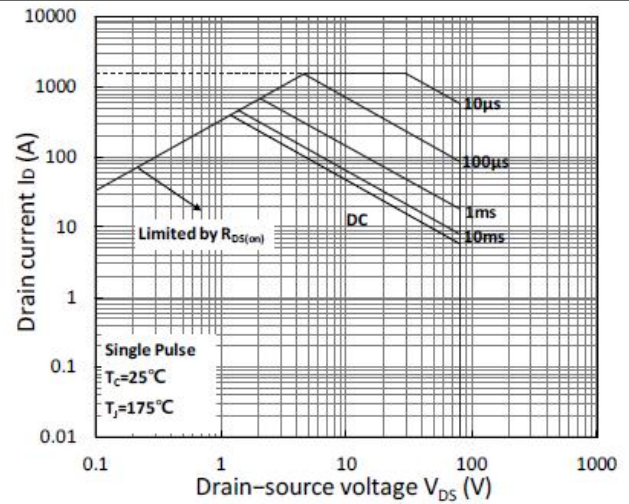


Figure10. Safe Operating Area

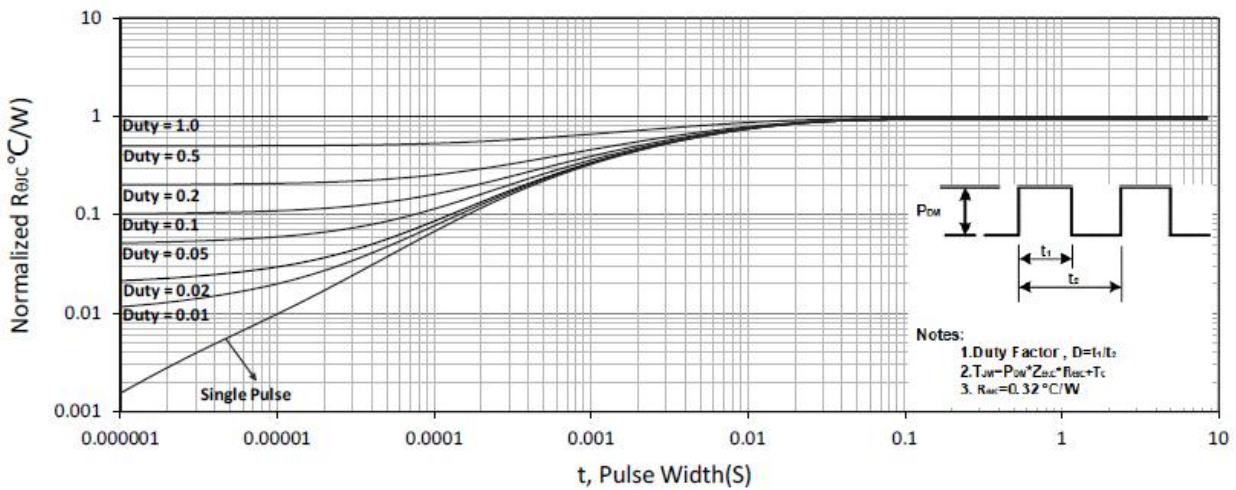


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

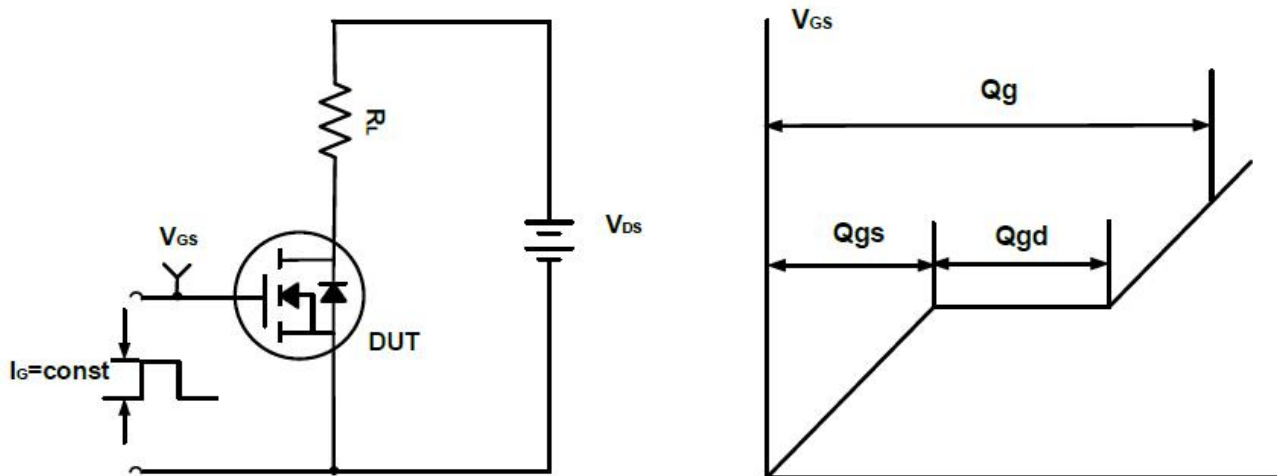


Figure A. Gate Charge Test Circuit & Wave forms

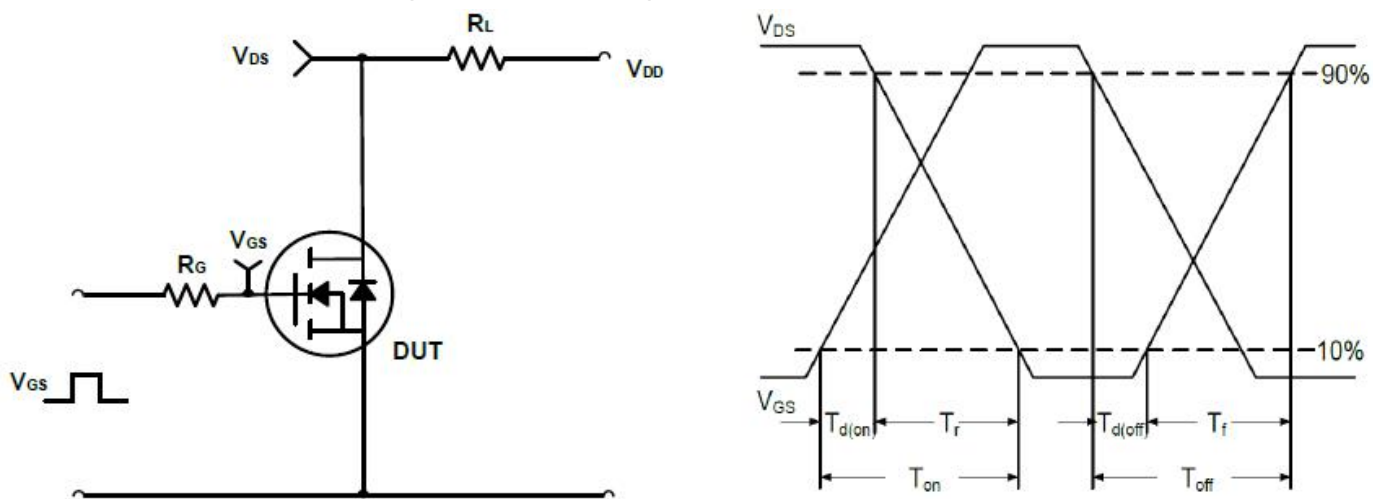


Figure B. Switching Test Circuit & Wave forms

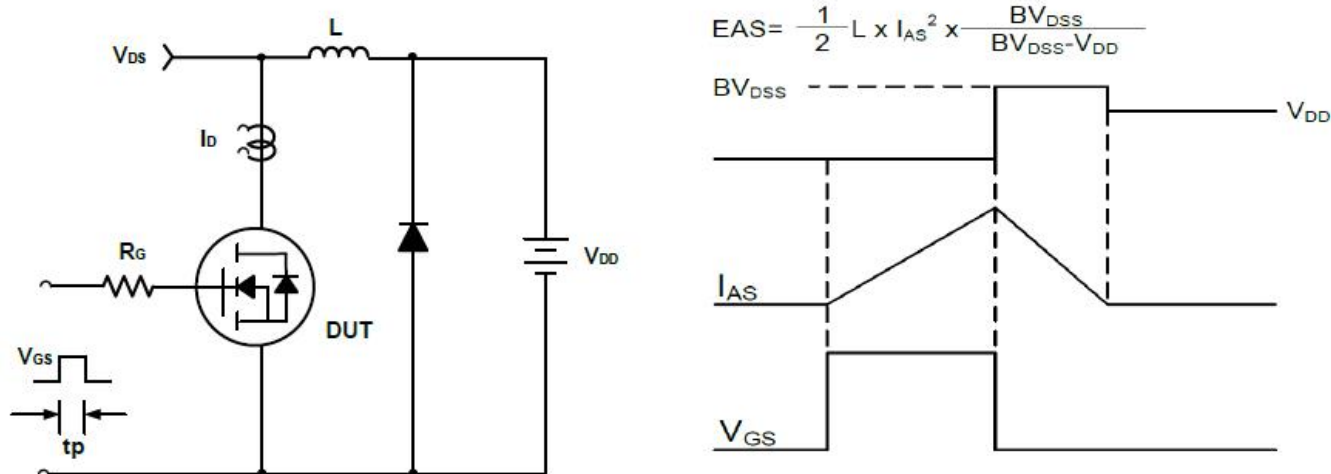
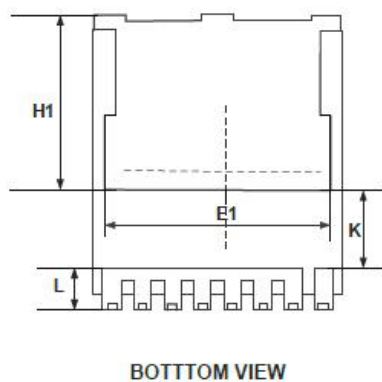
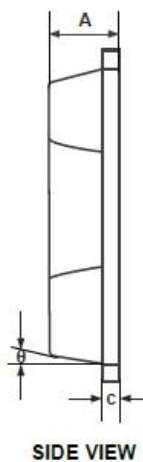
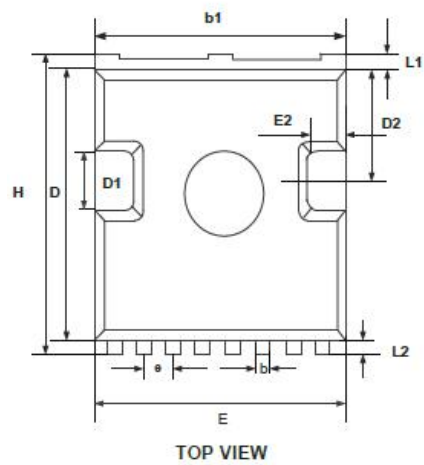


Figure C. Unclamped Inductive Switching Circuit & Wave forms

Package Dimensions TOLL-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	2.20	2.40
b	0.60	0.90
b1	9.70	9.90
c	0.40	0.60
D	10.20	10.60
D1	3.10	3.50
D2	4.45	4.75
E	9.70	10.10
E1	7.80BSC	
E2	0.50	0.70
e	1.200 BSC	
H	11.45	11.90
H1	6.75 BSC	
K	3.10 REF	
L	1.70	2.10
L1	0.60	0.80
L2	0.50	0.70
θ	10° REF	



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