Application Note: SY50213W

Flyback Regulator With Primary Side CV/CC Control

General Description

SY50213W is a single stage Flyback regulator targeting at Constant Current/Constant Voltage (CC/CV) applications. It integrates a 800V bipolar NPN transistor in a compact SO8 package to minimize the size. Both the output current and voltage are sensed on the primary side, eliminating the opto-isolator and the secondary side feedback circuitry, and minimizing the overall system cost.

SY50213W adopts the quasi-resonant operation and the adaptive PWM/PFM control to achieve the highest average efficiency and the best EMI performance. The no-load switching frequency can be as low as 500Hz, minimizing the no-load power loss

SY50213W has programmable cable compensation to provide a better load regulation for the output voltage at the cable terminals.

SY50213W provides reliable protections including VIN Over Voltage Protection, Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP protection (OVP), VSEN/ISEN pin short protection, VSEN pin upper divider resistor disconnect protection.

Features

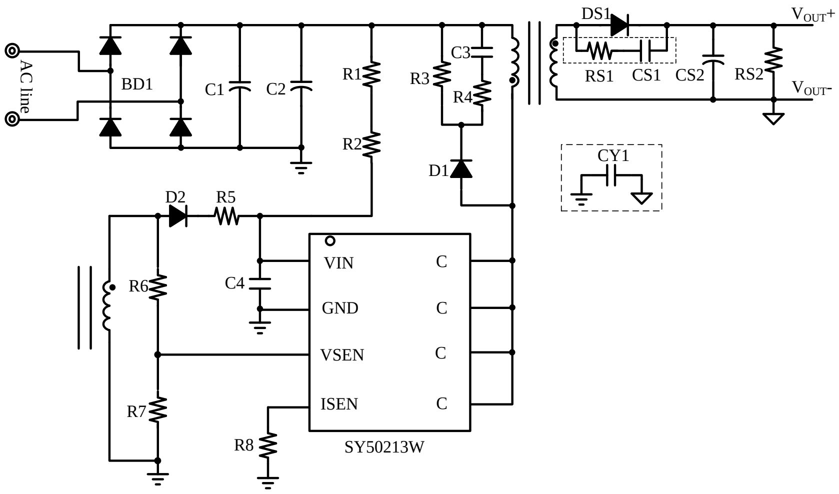
- Tight PSR CC/CV Regulation Over Entire Operating Range
- QR-mode Operation for High Efficiency
- PWM/PFM Control for High Average Efficiency
- Fast dynamic load transient response
- Cable Compensation for Better Load Regulation
- Low Start Up Current: 5μA Max
- Minimum Frequency Limitation 500Hz
- No-load Power is Less than 75mW
- Reliable Protections for OVP, SCP, OTP,OCP
- Reliable Protections for Safety Requirement
- Maximum switching frequency limitation125kHz
- Integrated 800V bipolar NPN transistor
- RoHS Compliant and Halogen Free
- Compact Package: SO8

Applications

- AC/DC Adapters
- Battery Chargers

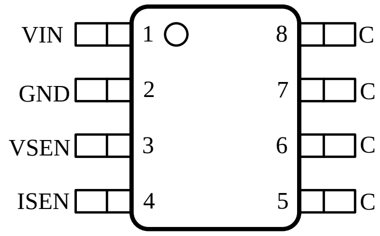
Recommended Operating Output Power		
Products	90~264Vac	176~264Vac
SY50213W	12W	15W

Typical Applications



Ordering Information

SY50213□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code



Pinout (Top view)

Ordering Number	Package	Top Mark
SY50213WFAC	SO8	CQWxyz

x=year code, y=week code, z= lot number code

Pinout

Pin Number	Pin Name	Pin Description
1	VIN	Power supply pin. Bypass this pin to the GND pin with a ceramic capacitor.
2	GND	Ground pin.
3	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. The value of the resistor divider also programs the cable impedance. This pin also senses the winding voltage to provide the QR operation.
4	ISEN	Current sense pin. The current sense resistor is placed between this pin and the GND pin.
5	C	Collector of the internal bipolar NPN transistor.
6	C	Collector of the internal bipolar NPN transistor.
7	C	Collector of the internal bipolar NPN transistor.
8	C	Collector of the internal bipolar NPN transistor.

Absolute Maximum Ratings (Note 1)

VIN-- -0.3V~26V
VSEN --- -0.3V~3.6V
ISEN-- -0.3V~3.6V
Supply Current I_{VIN} -- 20mA
C--- 800V
Power Dissipation, @ T_A = 25°C SO8 -- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} -- 150°C/W
SO8, θ_{JC} -- 60°C/W
Junction Temperature Range -- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range --- -65°C to 150°C

Recommended Operating Conditions

VIN -- 6V~14V
ISEN-- 0V~1V
Junction Temperature Range-- -40°C to 125°C
Ambient Temperature Range-- -40°C to 105°C

Electrical Characteristics

(V_{VIN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

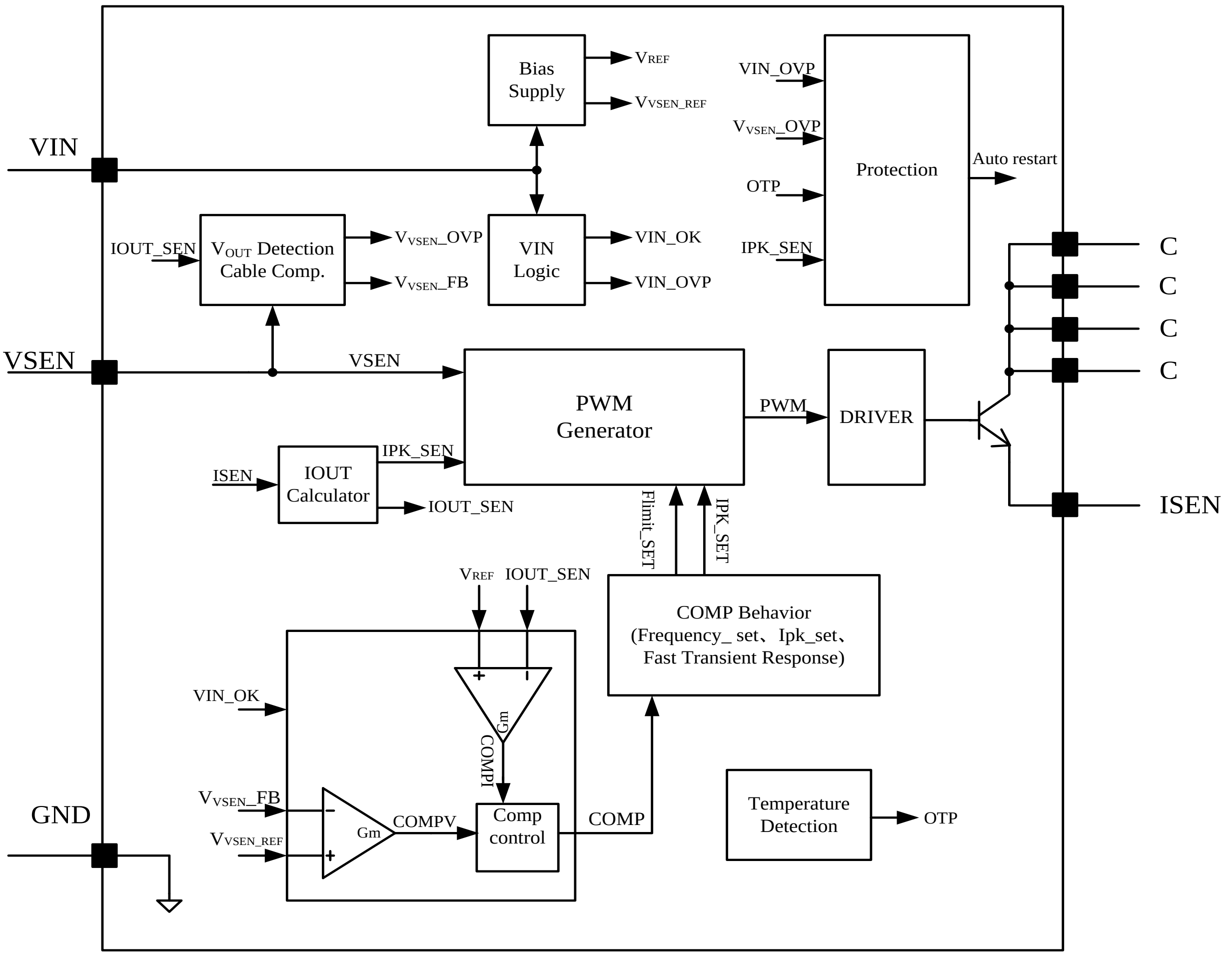
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}		19.6	21.3	23	V
VIN Turn-off Threshold	V_{VIN_OFF}		3.3	4.2	5	V
VIN OVP Voltage	V_{VIN_OVP}			V_{VIN_ON}+3		V
Start Up Current	I_{ST}	V_{VIN}<V_{VIN_OFF}		2.4	5	μA
Operating Current	I_{VIN}	f=100kHz		4.8		mA
Quiescent Current	I_Q	f=500Hz		170		μA
Discharge Current in OVP Mode	I_{VIN_OVP}	V_{VIN}=12V		5.5		mA
Current Feedback Modulator Section						
Internal Reference Voltage	V_{REF}		0.41	0.42	0.43	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}	V_{FBV}<0.4V		0.85		V
		V_{FBV}>0.4V	0.87	1	1.16	V
VSEN Pin Section						
OVP Voltage Threshold	V_{VSEN_OVP}		1.4	1.5	1.6	V
Internal Reference Voltage	V_{VSEN_REF}		1.232	1.25	1.268	V
Cable Compensation Coefficient	K_3		16	25	31	μA/V
Integrated Bipolar NPN Transistor Section						
Collector-Base voltage	$V_{(BR)CBO}$	Ic=1mA,Ie=0	800			V
Switching Section						
Max ON Time	T_{ON_MAX}			26		μs
Min ON Time	T_{ON_MIN}			360		ns
Max OFF Time	T_{OFF_MAX}		1.58	2	2.42	ms
Min OFF Time	T_{OFF_MIN}		1.3	1.8	2.3	μs
Minimum Switching Period	T_{PERIOD_MIN}		6.9	8	9.1	μs
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Temperature Hysteresis	T_{SD_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

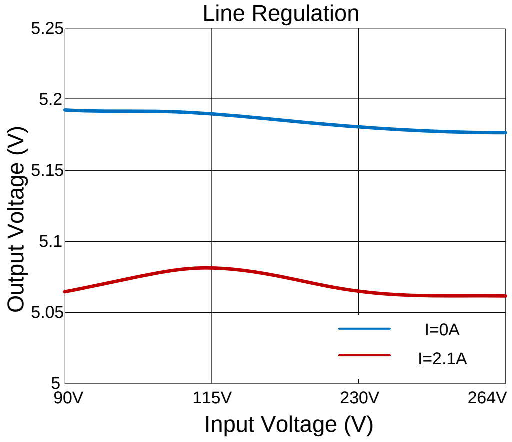
Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage to start the IC first, then set VIN to 12V.

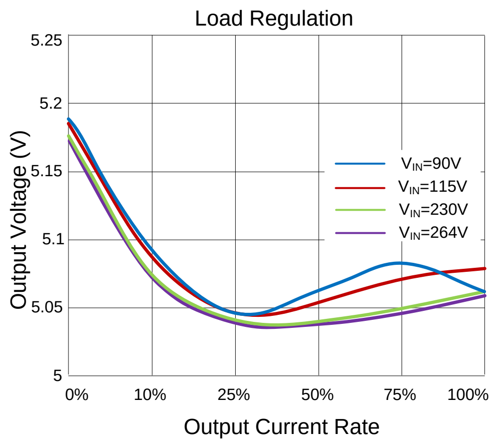
Block Diagram

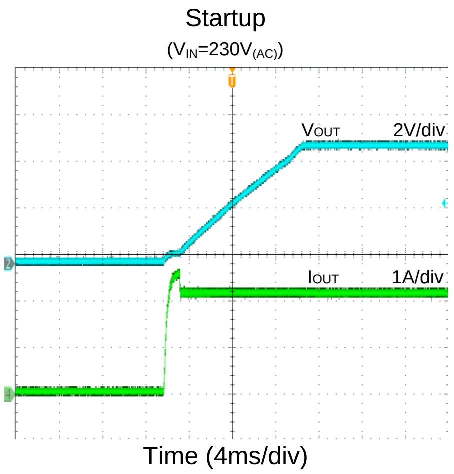


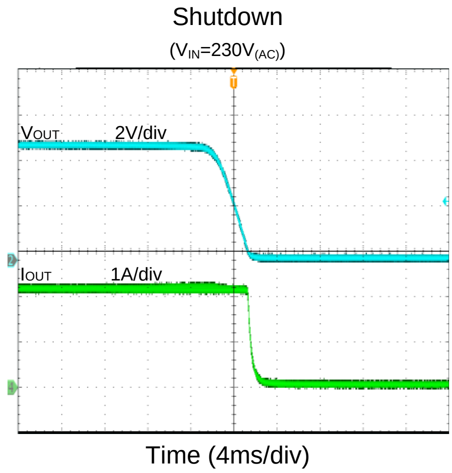
Typical Performance Characteristics

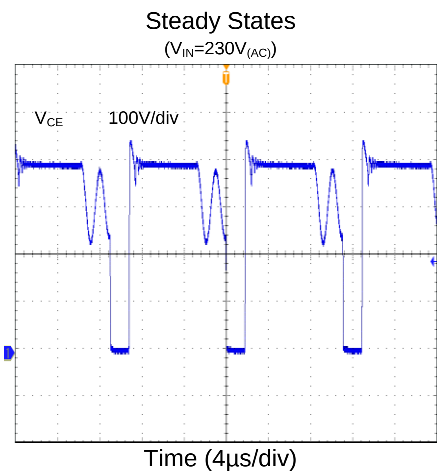
(Test condition: input voltage: 90~264Vac; output spec: 5Vdc_2.1A; output cable: 22AWG_1.2m; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

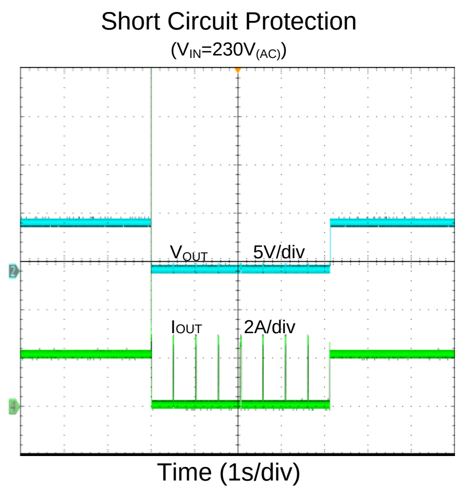


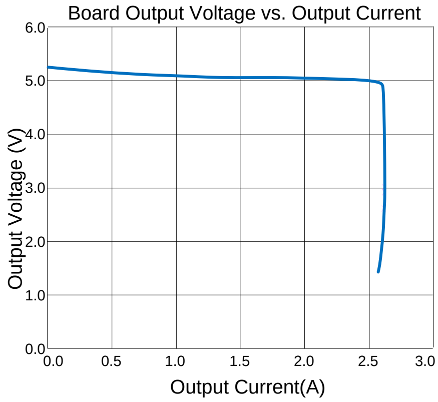


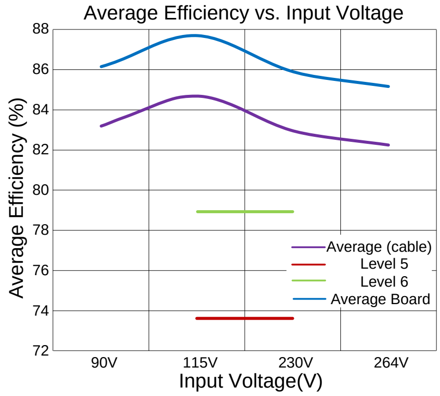









Board Output Voltage vs. Output Current
Output Voltage (V)
Output Current(A)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0


Average Efficiency vs. Input Voltage
Average Efficiency (%)
Input Voltage(V)
88
86
84
82
80
78
76
74
72
90V
115V
230V
264V
Average (cable)
Level 5
Level 6
Average Board

Operation Principles

Start-up Operation

After AC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VIN and GND pins, C_{VIN}, is charged up by the BUS voltage through a start up resistor R_{ST}. Once V_{VIN}, the voltage on the VIN pin, rises up to V_{VIN_ON}, the internal blocks starts the operation. V_{VIN} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VIN} above V_{VIN_OFF}.

The start-up procedure is divided into two sections, as shown in Fig.1: t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

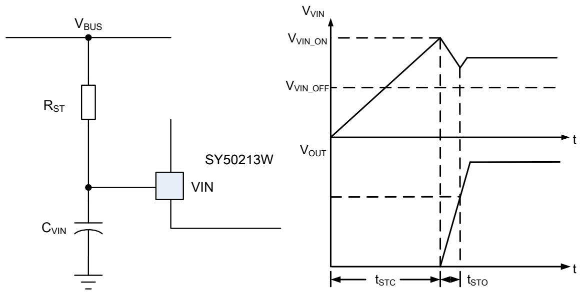


Fig.1 Start up

The start up resistor R_{ST} and C_{VIN} are designed by the following rules:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS\_MIN}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start-up time t_{ST}, and ensure the output voltage is built up with only one try.

$$C_{VIN} = \frac{\left(\frac{V_{BUS\_MIN}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage with one try, increase C_{VIN} and decrease R_{ST}, go back to step (a) and repeat the same design flow until the ideal start up procedure is obtained.

Shut-down Operation

After AC supply is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VIN pin, V_{VIN} will decrease. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Quasi-Resonant Operation (Valley Detection)

The Quasi-Resonant switching mode is applied, which means to turn on the integrated bipolar NPN transistor at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

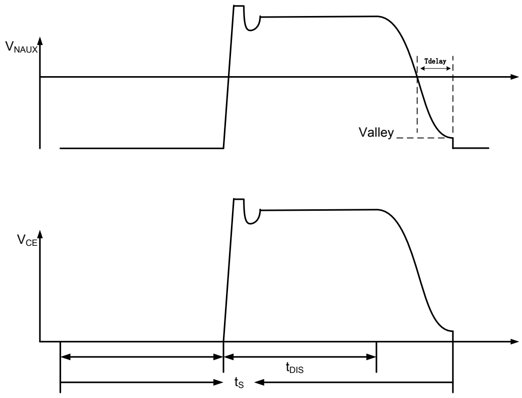


Fig.2 QR mode operation

The voltage across collector and emitter of the primary integrated bipolar NPN transistor is reflected to the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Fig.2, when the voltage on VSEN pin across zero, the bipolar NPN transistor would be turned on after 400ns delay.

Output Voltage Control (CV Control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding.

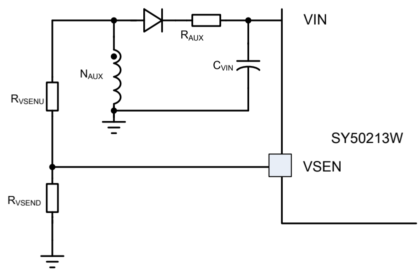


Fig.3 VSEN pin connection

As shown in Fig.4, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

where R_{VSEND} and R_{VSENU} are the low side and high resistors at the VSEN pin, respectively, and V_{VSEN_REF} is the internal voltage reference at 1.25V

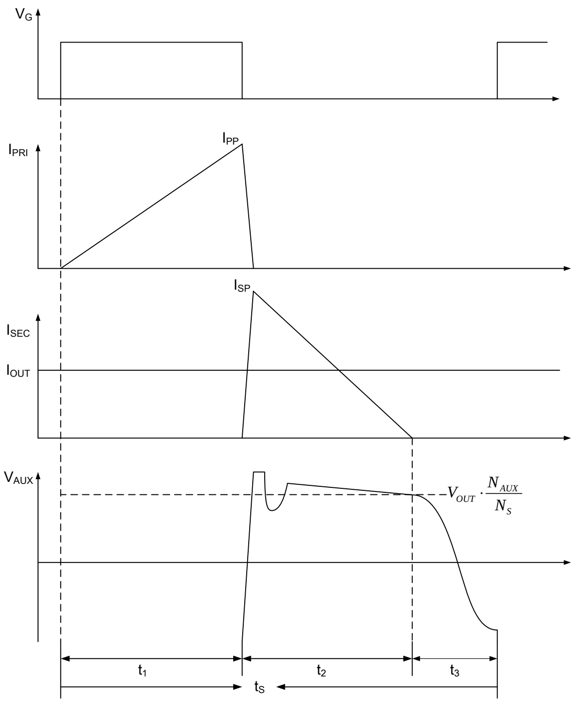


Fig.4 Auxiliary winding voltage waveforms

Output Current Control (CC Control)

The output current is regulated by SY50213W with primary side detection technology, the maximum output current I_{OUT_LIM} can be set by

$$I_{OUT\_LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} \quad (6)$$

K_1 is set to 0.5

When the over current operation or short circuit operation takes place, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.5.

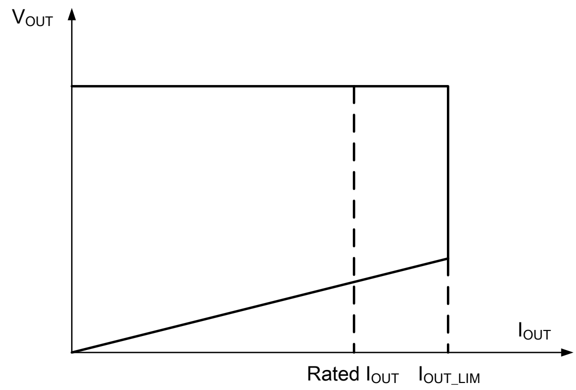


Fig.5 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit.

Cable Impedance Compensation

SY50213W incorporates the cable impedance compensation to provide a better load regulation of output voltage at cable terminals. When the converter output load increases from no load to full load, the resulting voltage decrease on the output cables are compensated by decreasing the voltage feedback signals, which is shown by Fig. 6.

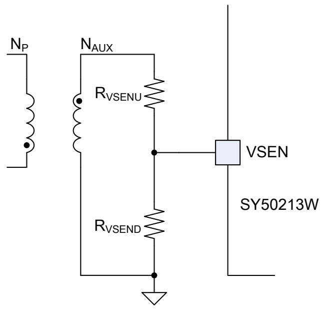


Fig. 6 Cable compensation

$$R_{VSENU} = \frac{R_{Cable}}{2k_3 \cdot R_S} \cdot \frac{N_P}{N_S} \cdot \frac{N_{AUX}}{N_S} \quad (7)$$

where k_3 is set to 25uA/V, R_S is the current sense resistor connecting to the ISEN pin.

R_{cable} is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of R_{VSENU} to achieve good load regulation of different output cables. The larger R_{VSENU}, the stronger cable compensation effect will be.

If the output current is below 10% the OCP point, the cable compensation is disabled.

Fault Protection Modes

Over-temperature Protection (OTP)

SY50213W includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the junction temperature exceeds the OTP threshold, about 150°C. In OTP mode, if the junction temperature decreases by approximately 20°C, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the junction temperature does not exceed the OTP threshold.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The valley signal of the auxiliary winding voltage might not be detected by the VSEN pin. In this case, bipolar NPN transistor cannot be turned on until maximum off time is reached. IC will shut down until VIN is below V_{VIN_OFF}, and then enter the hiccup mode.

When the output voltage is not low enough to disable the valley detection in short condition, SY50213W will operate in CC mode until VIN decreases below V_{VIN_OFF}. As shown in Fig.7, a filter resistor R_{AUX} is needed to prevent the SCP function from being affected by the voltage spikes of the auxiliary winding,

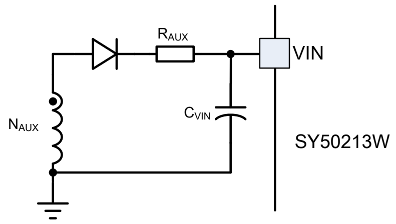


Fig. 7 Filter resistor R_{AUX}

VIN Voltage OVP Protection

When the VIN voltage exceeds V_{VIN_OVP} threshold, SY50213W will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the SY50213W will shut down and VIN will be charged again.

Output Voltage OVP Protection

When the VSEN pin signal exceeds 1.5V, reflecting an output over-voltage conditions, SY50213W will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

VSEN Pin Short Protection

The SY50213W has a protection against the faults caused by shorting VSEN pin to GND. When the VSEN voltage does not reach the sense protection trigger level at the end of startup, the VSEN pin is deemed shorting to GND, and the protection is activated: the IC stops switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode. In order to ensure reliable detection, the pull-down resistor at VSEN pin should be larger than 2kΩ.

ISEN Pin Short Protection

The SY50213W has a protection against the faults caused by shorting ISEN pin to GND. If ISEN short is detected at startup the IC stops switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

VSEN Pin Upper Divider Resistor Disconnect Protection

If the upper divider resistor disconnected lasting for 8 switching cycles, the IC will stop switching and discharge the VIN voltage. Meanwhile, limit the V_{ISEN} at V_{I_MIN}. Once V_{VIN} is below V_{VIN_OFF}, the SY50213W will shut down and VIN will be charged again.

Power Supply Design Considerations

Power Rating

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50213W	90Vac~264Vac	10.5W	5V/2.1A	55℃
	90Vac~264Vac	12W	12V/1A	40℃

The test is conducted in a natural cooling condition at 25 ℃ ambient temperature.

Transformer Design Considerations (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the internal power bipolar NPN transistor:

$$N_{PS} \le \frac{V_{(BR)CBO} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (8)$$

where $V_{(BR)CBO}$ is the breakdown voltage of the integrated bipolar NPN transistor. V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle, t_S, consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

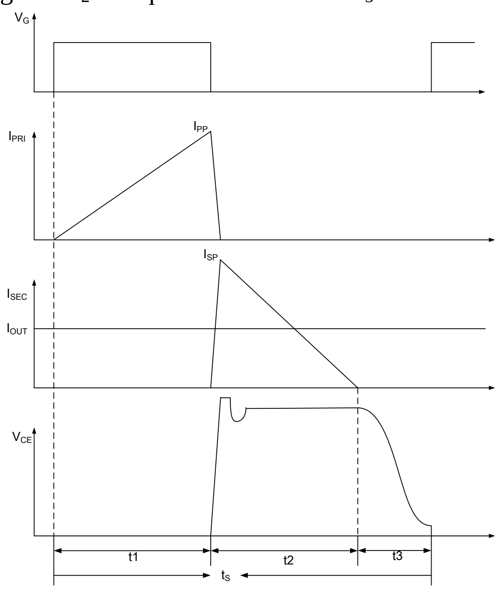


Fig.8 switching waveforms

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is minimum while the peak current through integrated bipolar NPN transistor is maximum.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed. The design flow is shown below.

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{(BR)CBO} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (9)$$

(b) Preset minimum frequency f_{S_MIN}

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times V_{DC\_MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi\sqrt{\frac{2P_{OUT}}{\eta} \times C_{Collector} \times f_{S\_MIN}} \quad (10)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}} \quad (11)$$

where $C_{Collector}$ is the parasitic capacitance at collector of integrated bipolar NPN transistor, η is the efficiency, and P_{OUT} is the rated full load power

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS}} \quad (12)$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} \quad (13)$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Collector}} \quad (14)$$

$$t_S = t_1 + t_2 + t_3 \quad (15)$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (16)$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (17)$$

$$I_{S\_RMS\_MAX}=\frac{\sqrt{3}}{3}N_{PS}\times I_{P\_PK\_MAX}\times\sqrt{\frac{t_2}{t_S}} \quad (18)$$

Transformer Design Considerations

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.28T

(c) Compute primary turn N_P

$$N_P=\frac{L_M\times I_{P\_PK\_MAX}}{\Delta B\times A_e} \quad (19)$$

(d) Compute secondary turn N_S

$$N_S=\frac{N_P}{N_{PS}} \quad (20)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX}=N_S\times\frac{V_{VIN}}{V_{OUT}} \quad (21)$$

where V_{VIN} is the working voltage of VIN pin (6V~14V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to achieve the current density from 4A/mm^2 to 10A/mm^2.

(g) If the window area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Diode Selection

Under the conditions of the maximum input voltage and full load, the voltage stress of secondary power diode is maximum;

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT} \quad (22)$$

where V_{AC_MAX} is maximum input AC RMS voltage, N_{PS} is the primary to secondary turns ratio of the Flyback transformer and V_{OUT} is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power diode is maximum.

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (23)$$

$$I_{D\_AVG}=I_{OUT} \quad (24)$$

where $I_{P\_PK\_MAX}$ is maximum primary peak current.

Input Capacitor C_{BUS} Selection

Generally, the input capacitor C_{BUS} is selected by

$C_{BUS}=2\sim 3\mu F/W$,

or more accurately by

$$C_{BUS}=\frac{\dfrac{\arcsin\left(1-\dfrac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}\right)+\dfrac{\pi}{2}}{\pi}\times\dfrac{P_{OUT}}{\eta}\times 1}{2f_{IN}V_{AC\_MIN}^2\left[1-\left(1-\dfrac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}\right)^2\right]} \quad (25)$$

Where ΔV_{BUS} is the voltage ripple of BUS line.

RCD snubber for bipolar NPN transistor selection

The power loss of the snubber P_{RCD} is evaluated as:

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT} \quad (26)$$

where V_{OUT} is the output voltage, V_{D_F} is the forward voltage of the power diode, ΔV_S is the overshoot voltage clamped by RCD snubber, L_K is the leakage inductor, L_M is the inductance of the Flyback transformer and P_{OUT} is the output power.

The R_{RCD} is calculated as:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (27)$$

The C_{RCD} is calculated as:

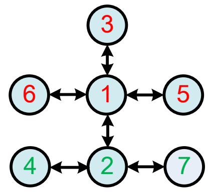
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (28)$$

Layout Considerations

A proper PCB design must follow the below guidelines:
(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

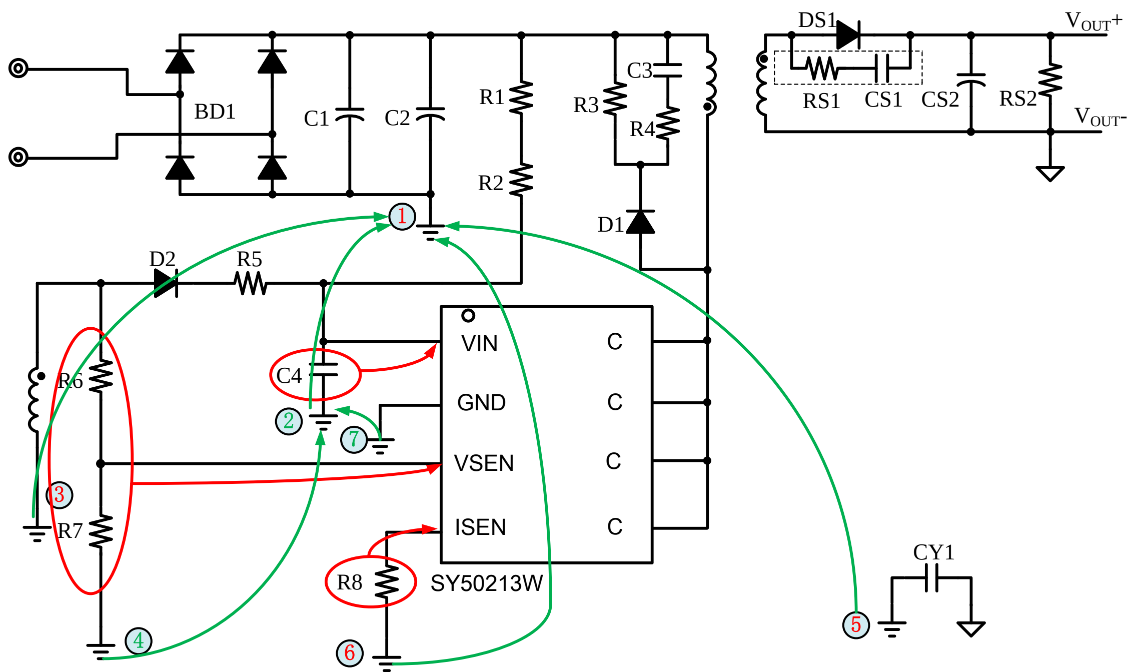
(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:

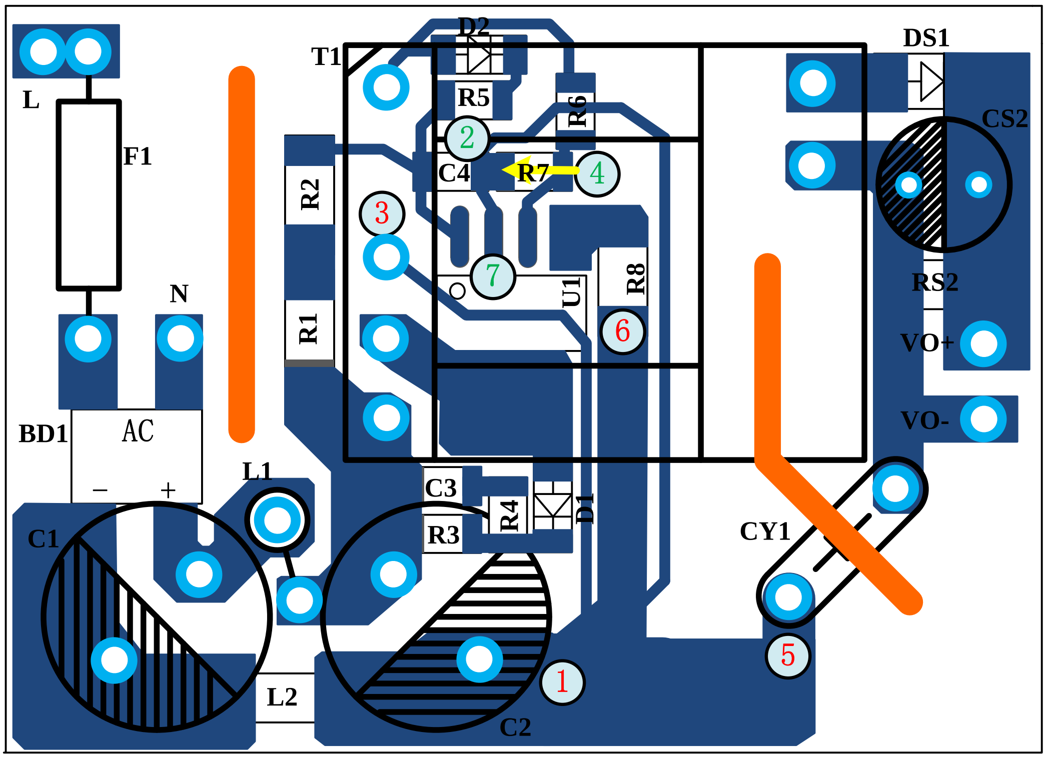


Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground node of divider resistor
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.
Ground ⑦: ground of IC GND.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.
(e) The loop consisting of 'ISEN pin – current sense resistor – GND pin' should be kept as small as possible.
(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note：Ground node of current sample resistor must be connected to the ground of bus line capacitor



Example layout

Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 1.8us.
2. VIN voltage should be designed to higher than 11V for all conditions.
3. RCD snubber's influence:
   At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. If Imin (Imin=0.24V/Rs) is 0.1A, the snubber capacitor should be no larger than 470pF.
4. At heavy load, the peak-to-peak voltage at the Vsen pin should be less than approximately 100mVp-p after off-min time (1.8us). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
5. R_{VSENU} is the upper resistor of the divider. Normally, its value should be in 20kΩ~130kΩ.
6. In order to ensure the CC/CV loop stability, the output capacitor should use the following formula to estimate:
   Cout= 3.7m*Iou t/Vout.
   For example, in the 5V/2A output case, Cout=3.7*2/5=1.48mF. The output capacitor can choose from 1270uF to 1680uF. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of Cout properly or use low ESR capacitor.

Design Example

A design example of typical application is shown below step by step. (Cable Test)
Note: All selected parameter (set value) need to adjust according to the practical condition.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	5V
I_{OUT}	2.1A	η	85%

#2. Transformer design (N_{PS}, L_M, N_P, N_S, N_{AUX})

(**1**)Refer to **Transformer selection (N_{PS} and L_M)**

Conditions			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
ΔV_S	75V	$V_{(BR)CBO}$	800V
P_{OUT}（Max）	10.5W	V_{D_F}	1V
$C_{Collector}$	100pF	f_{S_MIN}	60kHz
ΔV_{BUS}	30% V_{BUS_MIN}		

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{(BR)CBO} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$
$$= \frac{800V \times 0.9 - \sqrt{2} \times 264V - 75V}{5V + 1.0V}$$
$$= 45.3$$

N_{PS} is set to

$$N_{PS} = 16$$

(b)f_{S_MIN} is preset

$$f_{S\_MIN} = 60kHz$$

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times \left(\sqrt{2} V_{AC\_MIN} - \Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Collector} \times f_{S\_MIN}}$$
$$= \frac{2 \times 10.5W}{0.85 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 10.5W}{0.85 \times 16 \times (5V + 1V)} + \pi \times \sqrt{\frac{2 \times 10.5W}{0.85} \times 100pF \times 60KHz}$$
$$= 0.573A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$
$$= \frac{2 \times 10.5W}{0.85 \times (0.573A)^2 \times 60kHz}$$
$$= 1.255mH$$

Set: L_M=1.2mH. (Note: the actual value generally less than the compute value)

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS\_MIN}} = \frac{1.2mH \times 0.573A}{\sqrt{2} \times 90V} = 5.401\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{1.2mH \times 0.573A}{16 \times (5V + 1V)} = 7.161\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Collector}} = \pi \times \sqrt{1.2mH \times 100pF} = 1.088\mu s$$

$$t_S = t_1 + t_2 + t_3 = 5.401\mu s + 7.161\mu s + 1.088\mu s = 13.65\mu s$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 0.573A \times \sqrt{\frac{5.401\mu s}{13.65\mu s}} = 0.208A$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 16 \times 0.573A = 9.166A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}} = 16 \times \frac{\sqrt{3}}{3} \times 0.573A \times \sqrt{\frac{7.161}{13.65}} = 3.833A$$

(2) Refer to **Transformer number of turns selection (N_P, N_S, N_{AUX})**

(a) Select the magnetic core style, identify the effective area A_e. There select EF15-10 for compute example. Its A_e is 38.8 mm^2. The EF15-10 can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux ΔB. Usually ΔB=0.22~0.29T .

Set: ΔB=0.28T .

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} = \frac{1.2*10^{-3}*0.573A}{0.28*38.8*10^{-6}} = 63.28$$

Set: N_P=64

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{64}{16} = 4$$

Set: N_S=4

(e) compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} = 4 * \frac{12}{5} = 9.6$$

Set: N_{AUX}=10
Where V_{VIN} is the working voltage of VIN pin (6V~14V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

Primary wire diameter selection: current density j is set to 8 A/mm^2.

The compute primary wire cross-sectional area $S1 = \frac{I_{P\_RMS\_MAX}}{j} = \frac{0.208}{8} = 0.026mm^2$

The compute primary wire diameter $D1 = 2*\sqrt{\frac{S1}{\pi}} = 2*\sqrt{\frac{0.026}{\pi}} = 0.182mm$

Set: D1=0.19mm.

Secondary wire diameter selection: current density j is set to 10 A/mm^2.

The compute secondary wire cross-sectional area $S2 = \frac{I_{S\_RMS\_MAX}}{j} = \frac{3.833}{10} = 0.383mm^2$

The compute secondary wire diameter $D2 = 2*\sqrt{\frac{S2}{\pi}} = 2*\sqrt{\frac{0.383}{\pi}} = 0.699mm$

Set: D2=0.65mm*1.

Consider transformer style, the actual primary and secondary wire diameter can be adjusted for best production.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

(h) Other usually transformer inductance

	Specification	Remark
Thickened EE16 (90~264Vac,5V2.1A)		
Primary-Side Inductance	1.2mH±5%	40kHz,1V,25±5 ℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	96	
N_S	6	
N_A	15	
EF1510 (90~264Vac,5V2.1A)		
Primary-Side Inductance	1.2mH±5%	40kHz,1V,25±5 ℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	64	
N_S	4	
N_A	10	
Thickened EE16 (90~264Vac,12V1A)		
Primary-Side Inductance	1.25mH±5%	40kHz,1V,25±5 ℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	105	
N_S	15	
N_A	16	

#3. Select secondary power diode

Refer to **Diode selection**

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}=\frac{\sqrt{2}\times 264V}{16}+5V=28.335V$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=16\times 0.573A=9.166A$$

$$I_{D\_AVG}=2.1A$$

#4. Select the input capacitor CIN

Refer to **Input capacitor C_{BUS}**

Known conditions at this step			
V_{AC_MIN}	90V	ΔV_{BUS}	30% V_{BUS_MIN}

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC\_MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})+\frac{\pi}{2}}{\pi}\times\frac{10.5W}{0.85}\times\frac{1}{2\times 50\times 90V^2\times[1-(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})^2]}$$

$$=22.33\mu F$$

Set: C_{BUS}=20 μF

Where ΔV_{BUS} is the voltage ripple of BUS line.

#5. Set VIN pin

Refer to **Start up**

Conditions			
V_{BUS_MIN}	$90V\times\sqrt{2}$	V_{BUS_MAX}	$264V\times\sqrt{2}$
I_{ST}	5μA (max)	V_{VIN_ON}	21.5V (typical)
I_{VIN_OVP}	5.5mA (typical)	t_{ST}	3s (designed by user)

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS\_MIN}}{I_{ST}}=\frac{90V\times\sqrt{2}}{5\mu A}=25.46M\Omega,$$

$$R_{ST}>\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}}=\frac{264V\times\sqrt{2}}{5.5mA}=67.87k\Omega$$

Set R_{ST}

$$R_{ST}=5.4M$$

(b) Design C_{VIN}

$$C_{VIN}=\frac{(\frac{V_{BUS\_MIN}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}=\frac{(\frac{90V\times\sqrt{2}}{5.4M\Omega}-5\mu A)\times 3s}{21.5V}=2.590\mu F$$

Set C_{VIN}

$$C_{VIN}=4.7\mu F$$

#6. Set current sense resistor to achieve ideal output current

Refer to **Output current control (CC control)**

Known conditions at this step			
k_1	0.5	N_{PS}	16
V_{REF}	0.42V	I_{OUT_LIM}	2.73A

The current sense resistor is

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} = \frac{0.5 \times 0.42V \times 16}{2.73A} = 1.231\Omega$$

Set R_S

$R_S = 1.2\Omega$

#7. Set VSEN pin

Refer to **Output voltage control (CV control)**

First compute R_{VSENU}

Conditions			
V_{OUT}	5V	V_{VSEN_REF}	1.25V
R_{Cable}	0.130Ω(22AWG 1.2m)	N_S	4
N_{AUX}	10	K_3	25uA/V

$$R_{VSENU} = \frac{N_P}{N_S} \cdot R_{Cable} \cdot \frac{N_{AUX}}{N_S} \cdot \frac{1}{2K_3 \cdot R_S} = 86.67K\Omega$$

Set R_{VSENU}

$R_{VSENU} = 91K\Omega$

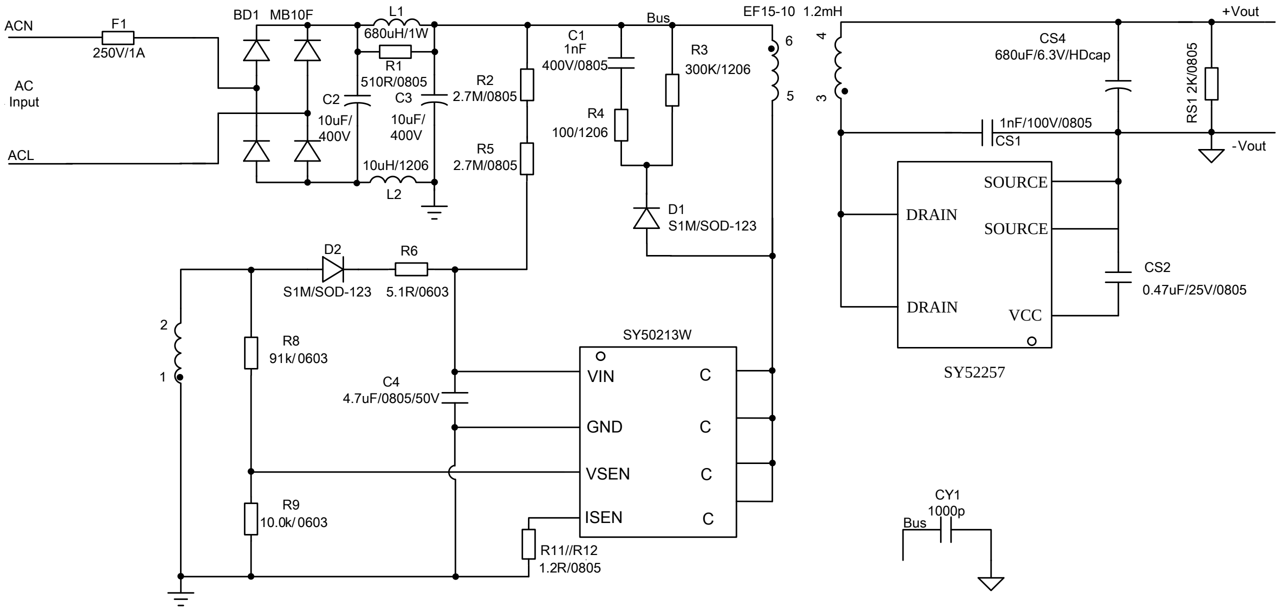
Then compute R_{VSEND}

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} N_{AUL}}{V_{VSEN\_REF} N_S} - 1} = \frac{91K}{(\frac{5V \times 10}{1.25V \times 4} - 1)} = 10.11K$$

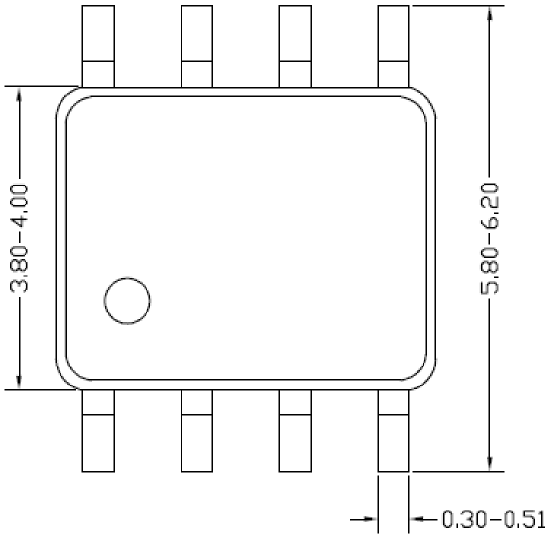
Set R_{VSEND}

$R_{VSEND} = 10k\Omega$

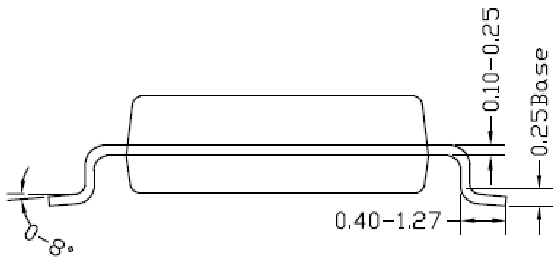
#8. Final result



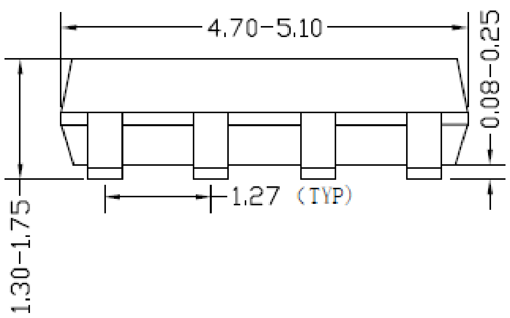
SO8 Package outline & PCB layout design



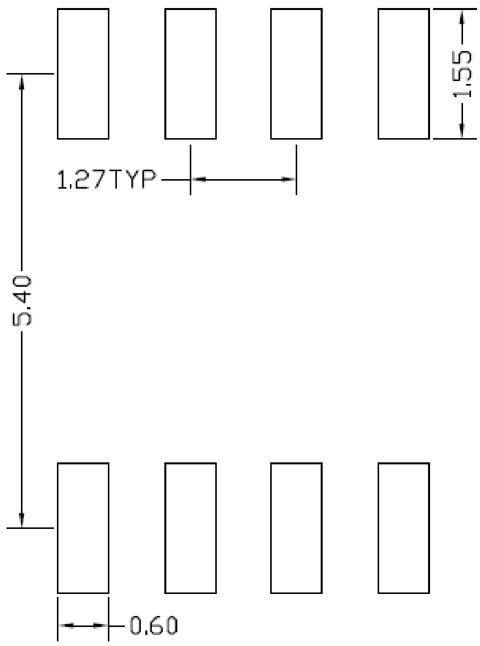
Top view



Side view



Front view

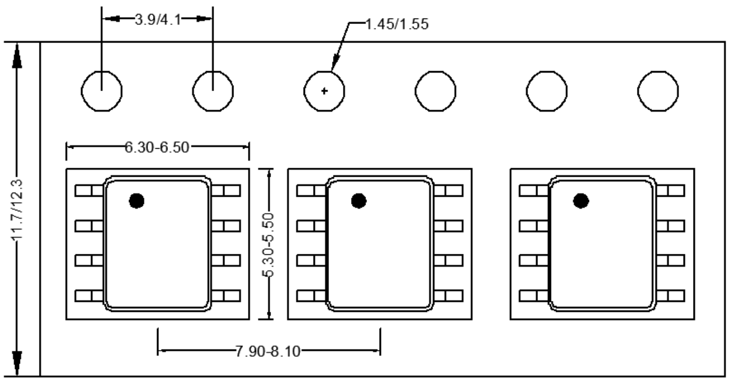


Recommended Pad Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

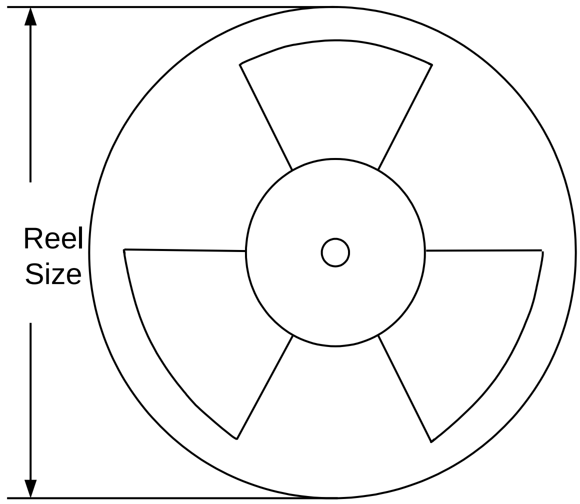
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
November 13,2019	Revision 0.9	Initial Release

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