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XINBOLE

Product Specification

XBLW CD4051

8-channel Analog Multiplexer/Demultiplexer

WEB | www.xinboleic.com

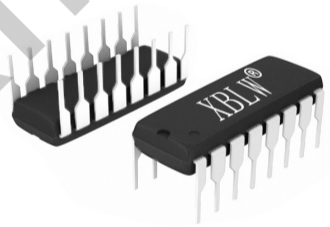
Description

The CD4051 is an 8-channel analog multiplexer/demultiplexer with three address inputs (S1 to S3), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z). With $\overline{E}$ LOW, one of the eight switches is selected (low-impedance ON-state) by S1 to S3. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 to S3, and $\overline{E}$). The V_{DD} to V_{SS} range is 3V to 9V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 9V. Unused inputs must be connected to V_{DD}, V_{SS}, or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

Features

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16



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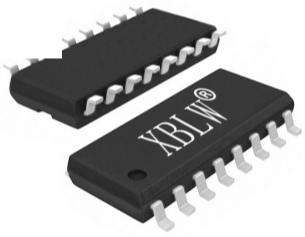

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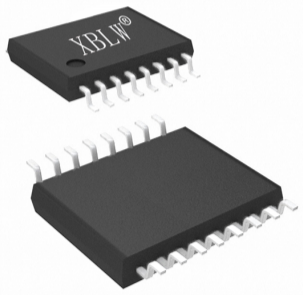


TSSOP-16

Applications

- Analog and digital multiplexing and demultiplexing
- Analog to digital and digital to analog conversion
- Signal gating
- Factory automation
- Televisions
- Appliances
- Consumer audio
- Programmable logic circuits
- Sensors

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW CD4051BE	DIP-16	CD4051BE	Tube	1000Pcs/Box
XBLW CD4051BDTR	SOP-16	CD4051B	Tape	2500Pcs/Reel
XBLW CD4051BTDTR	TSSOP-16	CD4051B	Tape	3000Pcs/Reel

Block Diagram

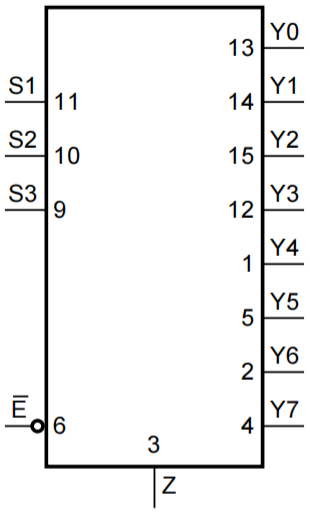


Figure 1. Logic symbol

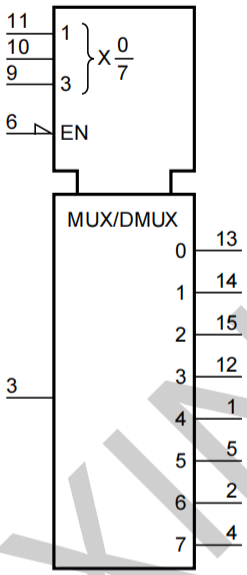


Figure 2. IEC logic symbol

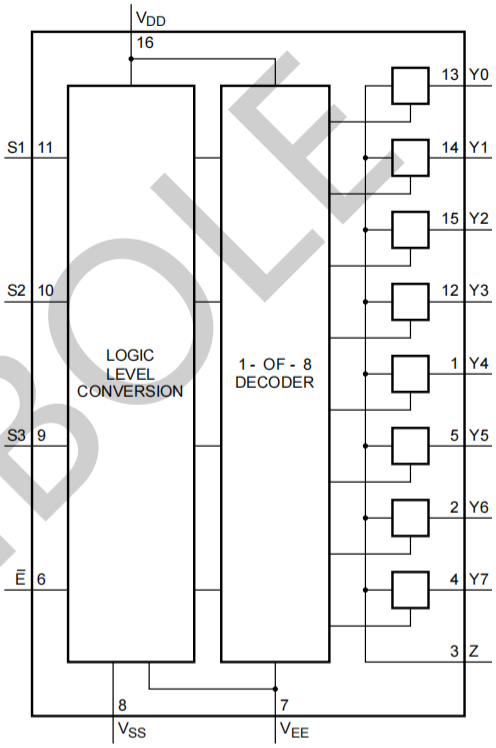


Figure 3. Functional diagram

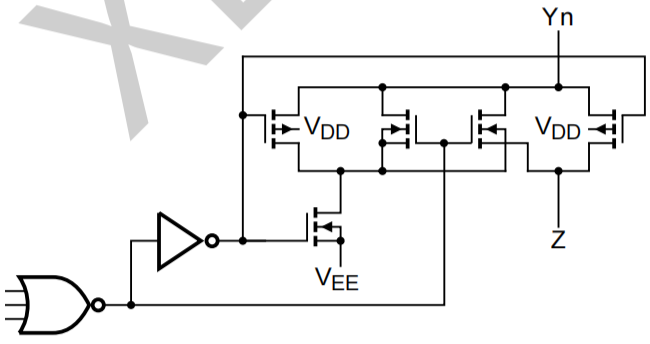


Figure 4. Schematic diagram (one switch)

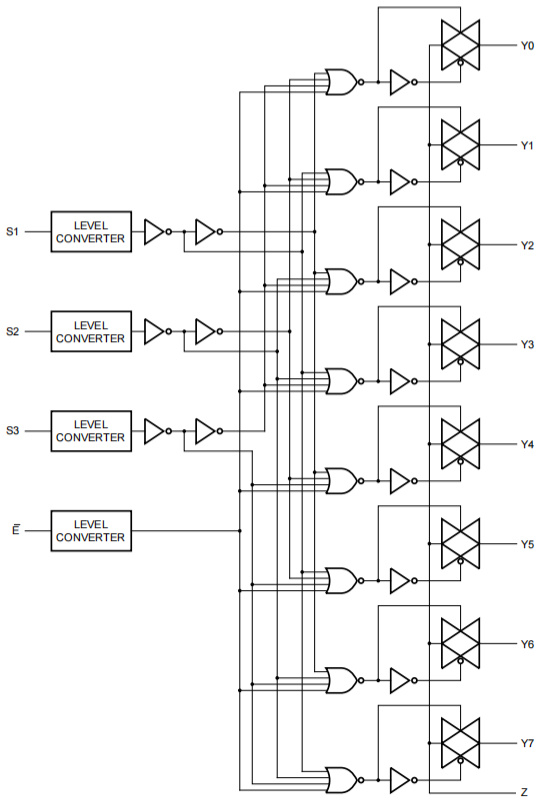
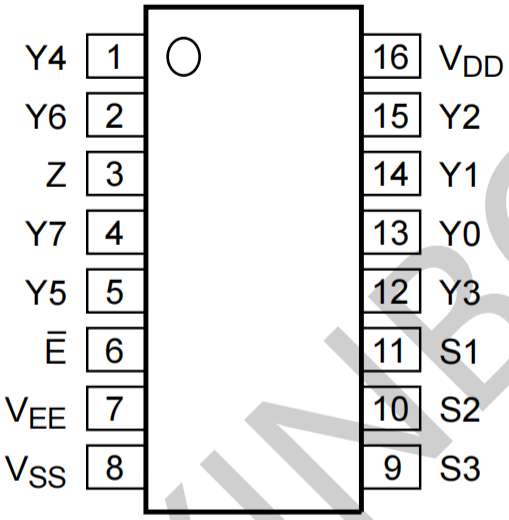


Figure 5. Logic diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	Y4	independent input or output
2	Y6	independent input or output
3	Z	common output or input
4	Y7	independent input or output
5	Y5	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V_{EE}	supply voltage
8	V_{SS}	ground (0V)
9	S3	select input
10	S2	select input
11	S1	select input
12	Y3	independent input or output
13	Y0	independent input or output
14	Y1	independent input or output
15	Y2	independent input or output
16	V_{DD}	supply voltage

Function Table

Input				Channel ON
$\bar{E}$	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+12	V
Power Supply Voltage	V_{EE}	-		-12	+0.5	V
input clamping current	I_{IK}	V_I<0.5V or V_I>V_{DD}+0.5V		-	±10	mA
switch current	I	-		-	±10	mA
input voltage	V_I	all inputs		-0.5	V_{DD}+0.5	V
storage temperature	T_{stg}	-		-65	+150	°C
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		°C
			SOP/TSSOP	260		°C

Recommended Operating Conditions

(T_{amb}=25°C; R_L=10kΩ; C_L=50pF; $\bar{E}$ =V_{DD}; Vis=V_{DD}=5V.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	5	9	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
supply voltage	V_{EE}	-	-6.0	-	0	V
supply voltage	V_{DD}-V_{EE}	-	3.0	-	9.0	V
input voltage	V_I	-	0	-	VDD	V
Disable output time （High level→turnoff）	t_{PHZ}	$\bar{E}$ to Z or $\bar{E}$ to Yn	-	85	170	ns
Disable output time （Low level→turnoff）	t_{PLZ}	$\bar{E}$ to Z or $\bar{E}$ to Yn	-	115	230	ns
Enable output time （turnoff→high/low level）	t_{PZH}, t_{PZL}	-	-	40	80	ns
input capacitance	C_I	-	-	-	7.5	pF

Electrical Characteristics

DC Characteristics 1

(T_{amb}=25°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		Tamb=25°C			Unit
				Min.	Typ.	Max.	
supply current	I_{DD}	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	-	20	uA
			V_{DD}=9V	-	-	40	uA
HIGH-level input voltage	V_{IH}	|I_O|<1uA	V_{DD}=5V	3.5	-	-	V
			V_{DD}=9V	7.0	-	-	V
LOW-level input voltage	V_{IL}	|I_O|<1uA	V_{DD}=5V	-	-	1.5	V
			V_{DD}=9V	-	-	3.0	V
input leakage current	I_I	V_I=0V or 9V, V_{DD}=9V		-	-	1.0	uA
3 state output leakage current	I_{OZ}	V_{DD}=9V	output to V_{DD}	-	-	1.6	uA
			output to V_{SS}	-	-	-1.6	uA
ON resistance (rail)	R_{ON}	V_{is}=0V to V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	350	2500	Ω
			V_{DD}-V_{EE}=9V	-	80	245	Ω
		V_{is}=0V	V_{DD}-V_{EE}=5V	-	115	340	Ω
			V_{DD}-V_{EE}=9V	-	50	160	Ω
		V_{is}=V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	120	365	Ω
			V_{DD}-V_{EE}=9V	-	65	200	Ω
ON resistance mismatch between channels	△ R_{ON}	V_{is}=0V to V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	25	-	Ω
			V_{DD}-V_{EE}=9V	-	10	-	Ω
OFF-state leakage current	$I_{S(OFF)}$	VSS=V_{EE}, V_{DD}-V_{EE}=9V	all channel off; $\overline{E}$=V_{DD}	-	-	1.0	uA
			any channel; $\overline{E}$=V_{SS}	-	-	1.0	uA

DC Characteristics 2

(T_{amb}=-40°C to +85°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		Tamb=-40°C		Tamb=+85°C		Unit
				Min.	Max.	Min.	Max.	
supply current	I_{DD}	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	20	-	150	uA
			V_{DD}=9V	-	40	-	300	uA
HIGH-level input voltage	V_{IH}	|I_O|<1uA	V_{DD}=5V	3.5	-	3.5	-	V
			V_{DD}=9V	7.0	-	7.0	-	V
LOW-level input voltage	V_{IL}	|I_O|<1uA	V_{DD}=5V	-	1.5	-	1.5	V
			V_{DD}=9V	-	3.0	-	3.0	V
input leakage current	I_I	V_I=0V or 9V,V_{DD}=9V		-	1.0	-	1.0	uA
3 state output leakage current	I_{OZ}	V_{DD}=9V	output to V_{DD}	-	1.6	-	12.0	uA
			output to V_{SS}	-	-1.6	-	-12.0	uA

DC Characteristics 3

(T_{amb}=-40°C to +125°C, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		Tamb=-40°C		Tamb=+125°C		Unit
				Min.	Max.	Min.	Max.	
supply current	I_{DD}	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	20	-	150	uA
			V_{DD}=9V	-	40	-	300	uA
HIGH-level input voltage	V_{IH}	|I_O|<1uA	V_{DD}=5V	3.5	-	3.5	-	V
			V_{DD}=9V	7.0	-	7.0	-	V
LOW-level input voltage	V_{IL}	|I_O|<1uA	V_{DD}=5V	-	1.5	-	1.5	V
			V_{DD}=9V	-	3.0	-	3.0	V
input leakage current	I_I	V_I=0V or 9V, V_{DD}=9V		-	1.0	-	1.0	uA
3 state output leakage current	I_{OZ}	V_{DD}=9V	output to V_{DD}	-	1.6	-	12.0	uA
			output to V_{SS}	-	-1.6	-	-12.0	uA

AC Characteristics 1

(T_{amb}=25°C, V_{EE}=V_{SS}=0V, t_r, t_f≤20ns, C_L=50pF, R_L=10kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay time	t_{PHL}	Yn to Z; Z to Yn; see Figure 7	V_{DD}=5V	-	15	30	ns
			V_{DD}=9V	-	5	10	ns
		Sn to Yn, Z; see Figure 8	V_{DD}=5V	-	150	300	ns
			V_{DD}=9V	-	60	120	ns
LOW to HIGH propagation delay	t_{PLH}	Yn to Z; Z to Yn; see Figure 7	V_{DD}=5V	-	15	30	ns
			V_{DD}=9V	-	5	10	ns
		Sn to Yn, Z; see Figure 8	V_{DD}=5V	-	150	300	ns
			V_{DD}=9V	-	65	130	ns
HIGH to OFF-state propagation delay	t_{PHZ}	$\overline{E}$ to Yn, Z; see Figure 9	V_{DD}=5V	-	120	240	ns
			V_{DD}=9V	-	90	180	ns
LOW to OFF-state propagation delay	t_{PLZ}	$\overline{E}$ to Yn, Z; see Figure 9	V_{DD}=5V	-	145	290	ns
			V_{DD}=9V	-	120	240	ns
OFF-state to HIGH propagation delay	t_{PZH}	$\overline{E}$ to Yn, Z; see Figure 9	V_{DD}=5V	-	140	280	ns
			V_{DD}=9V	-	55	110	ns
OFF-state to LOW propagation delay	t_{PZL}	$\overline{E}$ to Yn, Z; see Figure 9	V_{DD}=5V	-	140	280	ns
			V_{DD}=9V	-	55	110	ns

AC Characteristics 2

(T_{amb}=25°C, V_{EE}=V_{SS}=0V, V_I=0.5V_{DD} (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Square wave distortion	d_{sin}	see Figure 10; R_L=10kΩ; C_L=15pF; channel ON; f_i=1kHz	V_{DD}=5V	0.25	-	-	%
			V_{DD}=9V	0.04	-	-	%
any two channel crosstalk	f_{ct}	V_{DD}=9V, see note2		1	-	-	MHz
crosstalk voltage ($\overline{E}$ to Sn or Yn to Z)	V_{ct}	see Figure 11; R_L=10kΩ; C_L=15pF; $\overline{E}$ or Sn=V_{DD} (square-wave)		50	-	-	mV
OFF frequency	f_{OFF}	V_{DD}=9V, see note3		1	-	-	MHz
conduction frequency	f_{ON}	V_{DD}=5V, see note4		13	-	-	MHz
		V_{DD}=9V, see note4		40	-	-	MHz

Note:

[1] f_i is biased at 0.5V_{DD}; V_I=0.5V_{DD} (p-p).

[2] R_L=1kΩ; 20logVos/Vis=-50dB, see Figure 12.

[3] R_L=1kΩ; C_L=5pF, channel off, 20logVos/Vis=-50dB, see Figure 10.

[4] R_L=1kΩ; C_L=5pF, channel on, 20logVos/Vis=-3dB, see Figure 10.

Testing Circuit

AC Testing Circuit 1

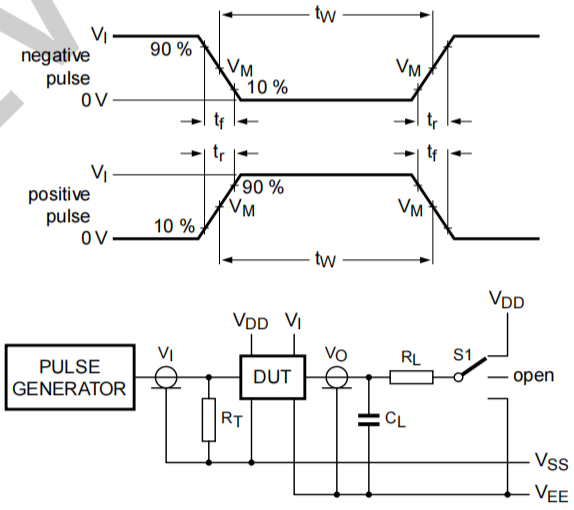


Figure 6. Test circuit for switching times

Definitions for test circuit: DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

AC Testing Waveforms

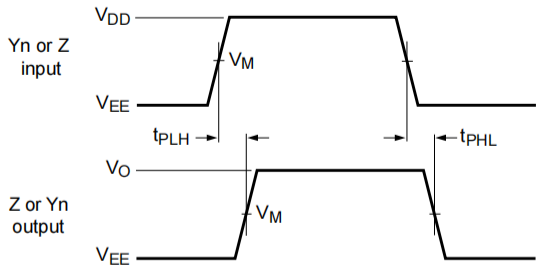


Figure 7. Yn, Z to Z, Yn propagation delays

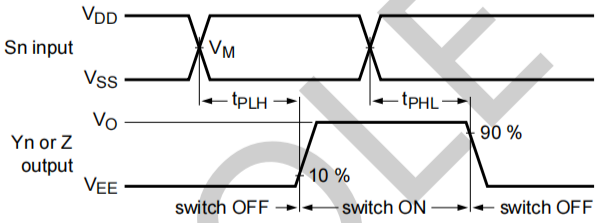


Figure 8. Sn to Yn, Z propagation delays

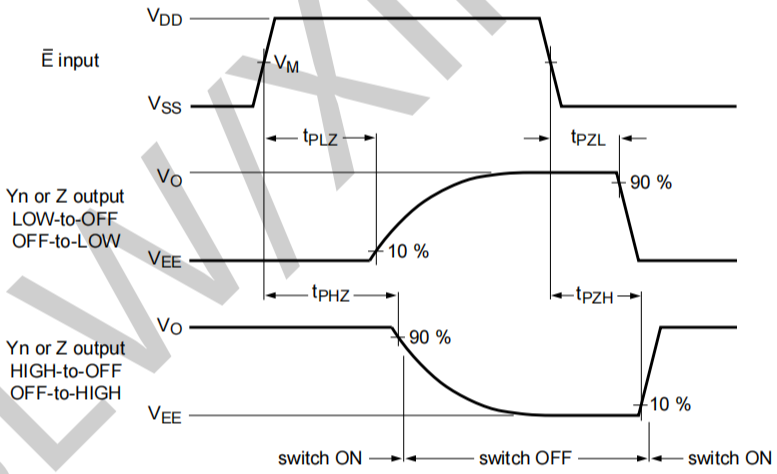


Figure 9. Enable and disable times

AC Testing Circuit 2

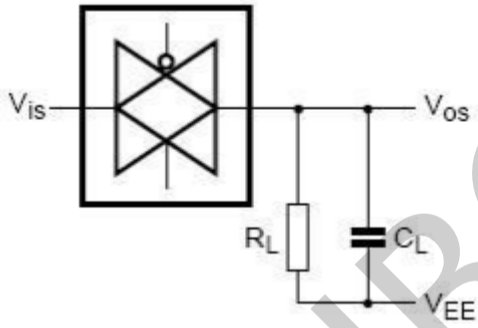


Figure 10. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

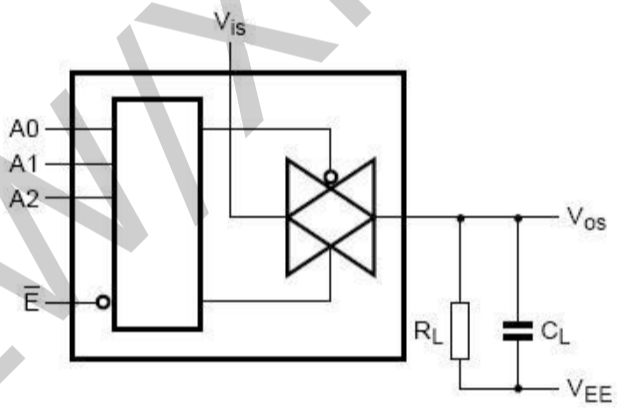


Figure 11. Crosstalk logical input/output test

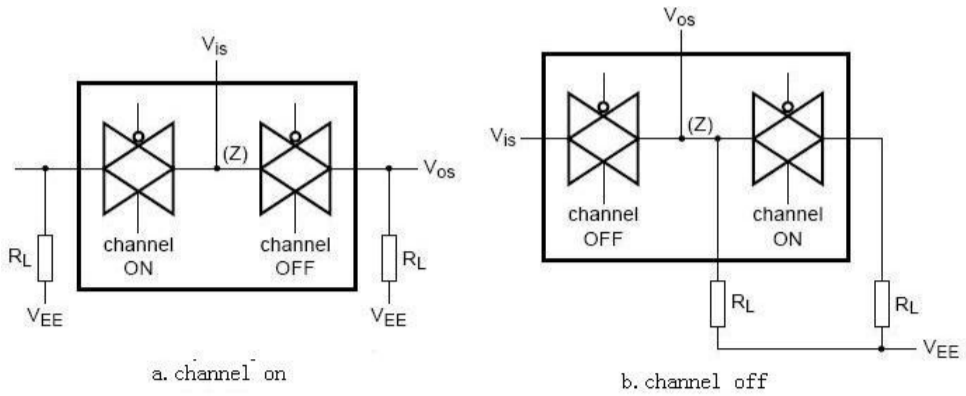


Figure 12. Inter channel Crosstalk

Measurement Points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	0.5×V_{DD}	0.5×V_{DD}

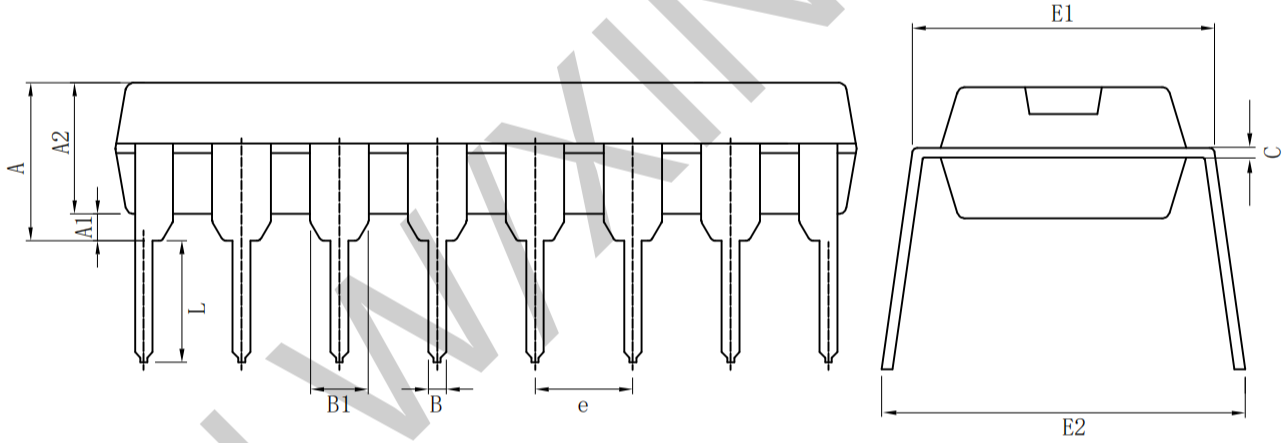
Test Data

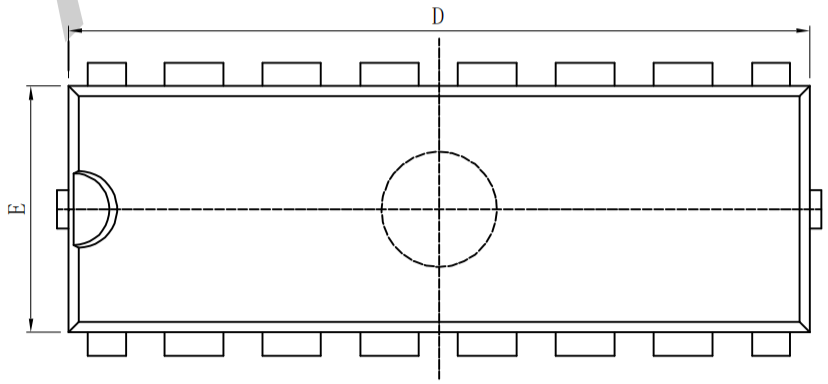
Test	Input		Load		Switch
	V_{is}	t_r,t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
others	pulse	20ns	50pF	10kΩ	open

Package Information

· DIP-16

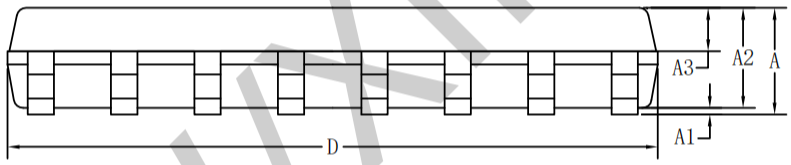
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

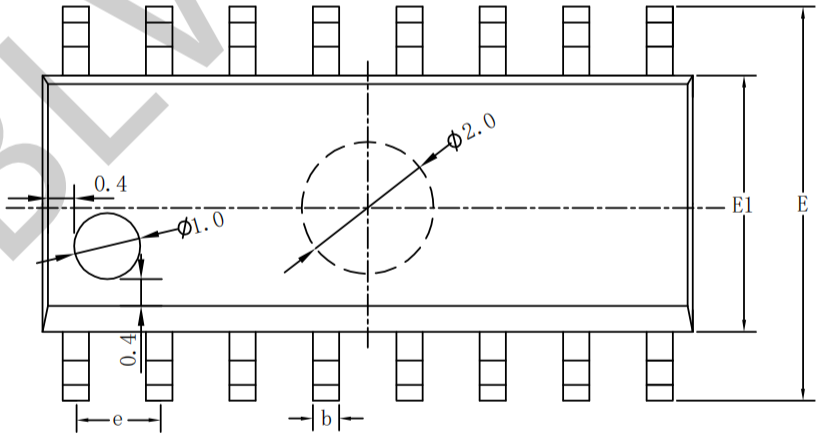


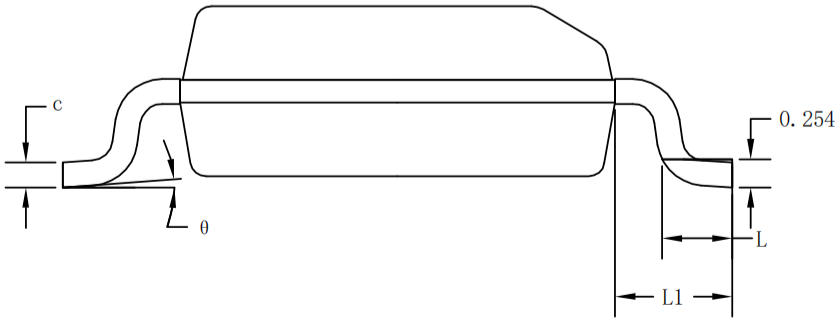


· SOP-16

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27(BSC)			e	0.050(BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05(BSC)			L1	0.041(BSC)		
θ	0°	4°	8°	θ	0°	4°	8°







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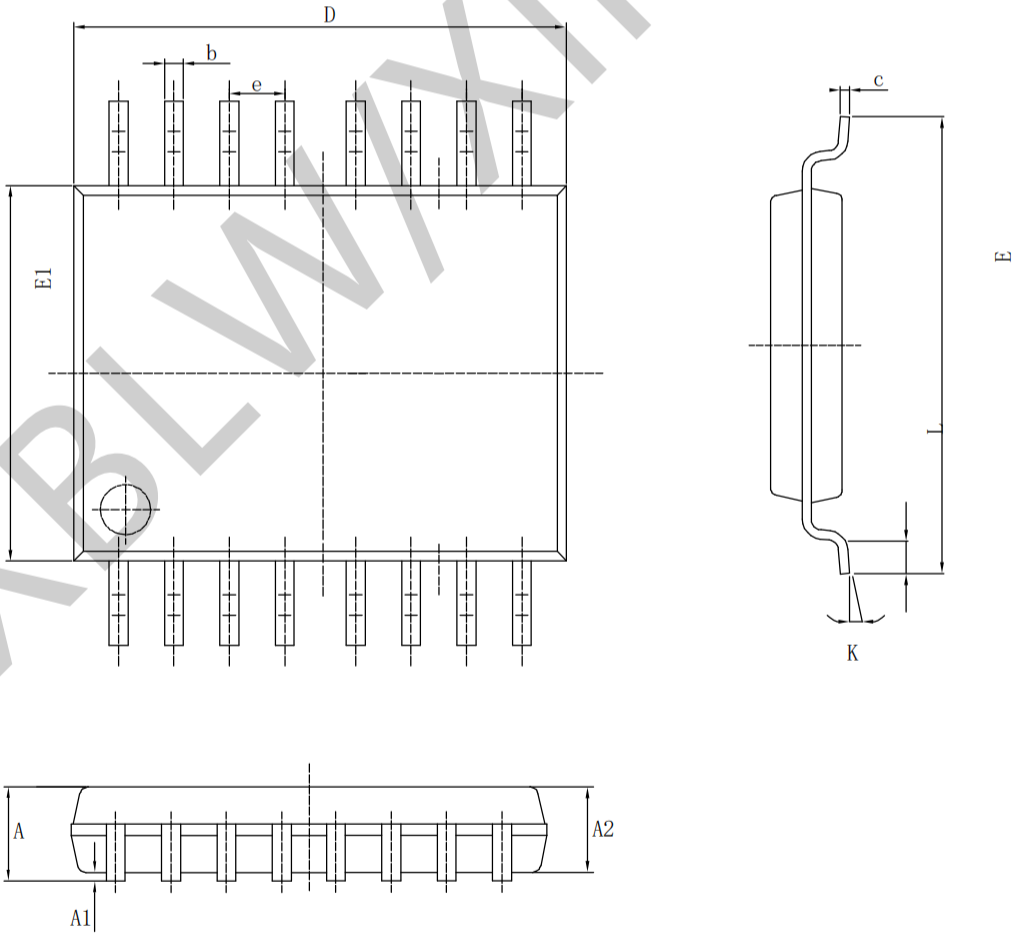
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65(BSC)		e	0.0256(BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



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