Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

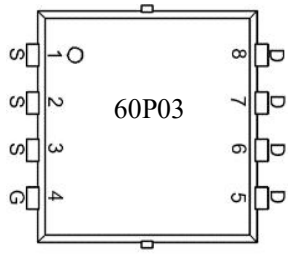
Bvdss	Rdson	ID
-30V	-7.5mΩ	-55A

Application

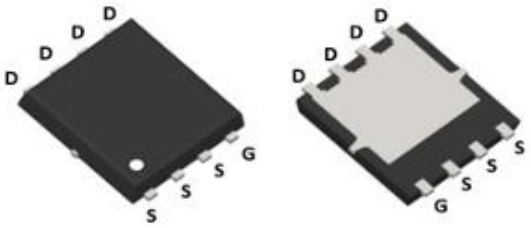
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

RoHS

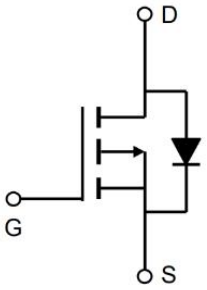
Package



Marking and pin assignment



PDFN3*3-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
60P03	60P03D	PDFN3*3-8L	5000

Absolute Maximum Ratings (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current,V_{GS}@10V[1]	T_C=25℃	I_D	-55	A
	T_C=100℃	I_D	-30	A
Pulsed Drain Current[1]		I_{DM}	-168	A
Single Pulsed Avalanche Energy[2]		EAS	45	mJ
Avalanche Current		I_{AS}	-	A
Total Power Dissipation[4]		P_D@T_C=25℃	37	W
Operating Junction Temperature Range		T_J	-55 ~ +150	℃
Storage Temperature Range		T_{STG}	-55 ~ +150	℃

Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	--	3.36	℃/W
Thermal Resistance Junction-to-Ambient[3]	$R_{\theta JA}$	--	75	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL60P03D	PDFN3*3-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics (T_J=25℃,unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-30	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V,T_J=25℃	-	-	-1	uA
		V_{DS}=-30V,V_{GS}=0V,T_J=100℃	-	-	-100	uA
Gate-Source Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-	-2.5	V
Static Drain-Source On-Resistance[4]	$R_{DS(on)}$	V_{GS}=-10V, I_D=-30A	-	7.5	14	mΩ
		V_{GS}=-4.5V, I_D=-15A	-	10	22	
Forward Transconductance[4]	gfs	V_{DS}=-5V,I_D=-30A	-	57	-	S
Gate Resistance	R_g	f=1MHz	-	10.5	-	Ω
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V, f=1MHz	-	2396	-	pF
Output Capacitance	C_{oss}		-	325	-	
Reverse Transfer Capacitance	C_{rss}		-	283	-	
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V, I_D=-30A	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	7.5	-	
Turn-on Delay Time	$T_{d(on)}$	V_{GS}=-10V,V_{DD}=-15V, R_G=3Ω,I_D=-30A	-	14.1	-	nS
Turn-on Rise Time	T_r		-	20	-	
Turn-Off Delay Time	$T_{d(off)}$		-	94	-	
Turn-Off Fall Time	T_f		-	65	-	
Continuous Source Current	I_S	T_J=25℃	-	-	-55	A
Diode Forward Voltage[4]	V_{SD}	V_{GS}=0V,I_S=-1A	-	-	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=-30A,dI/dt=100A/us	-	19	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	9	-	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C.

2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}=-10V, L= 0.1mH, I_{AS}=-30A.

3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.

5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

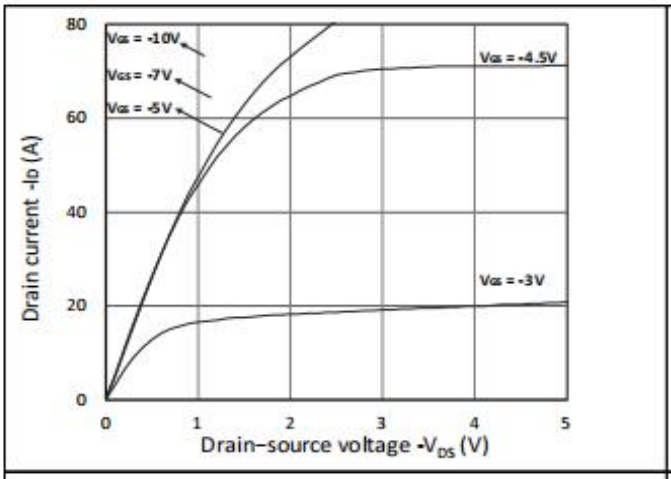


Figure 1. Output Characteristics

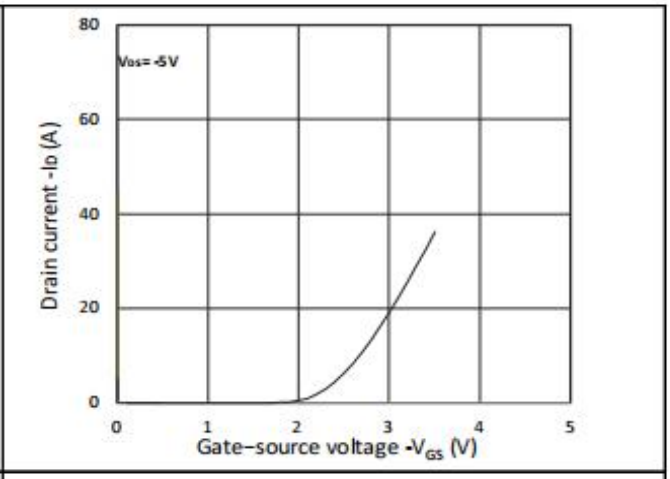


Figure 2. Transfer Characteristics

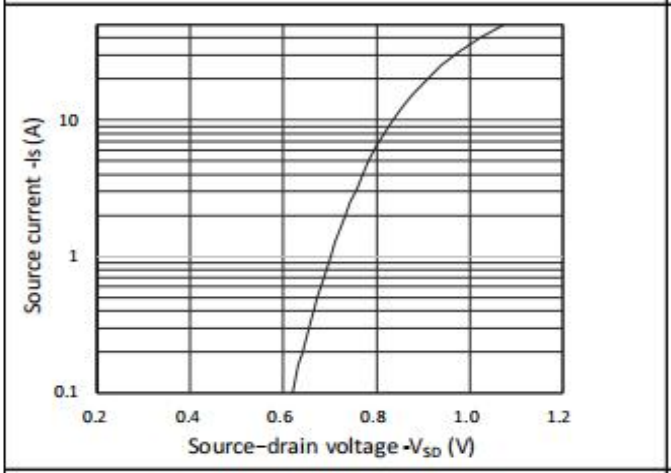


Figure 3. Forward Characteristics of Reverse

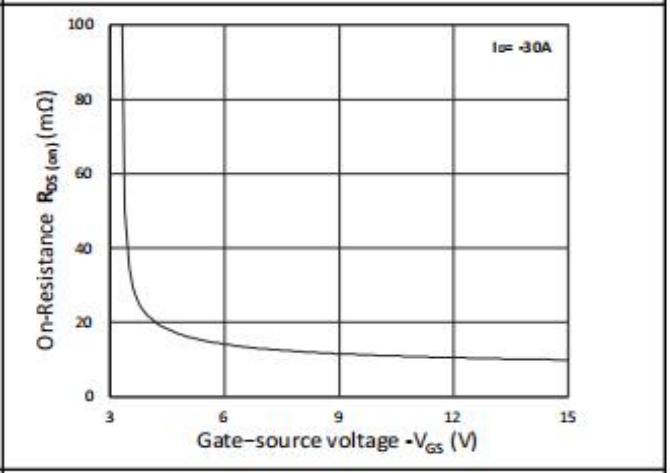


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

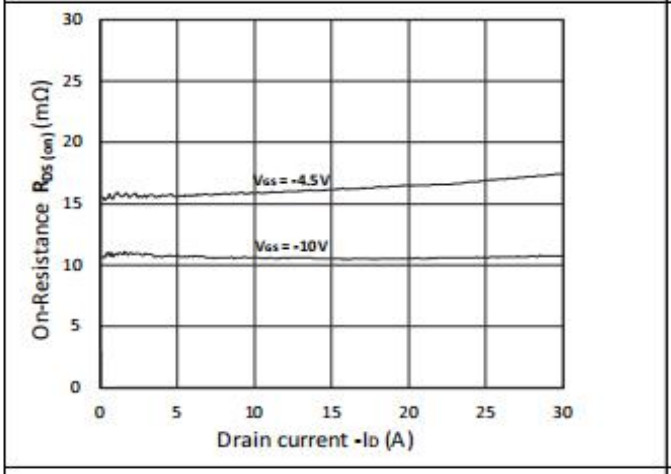


Figure 5. $R_{DS(ON)}$ vs. I_D

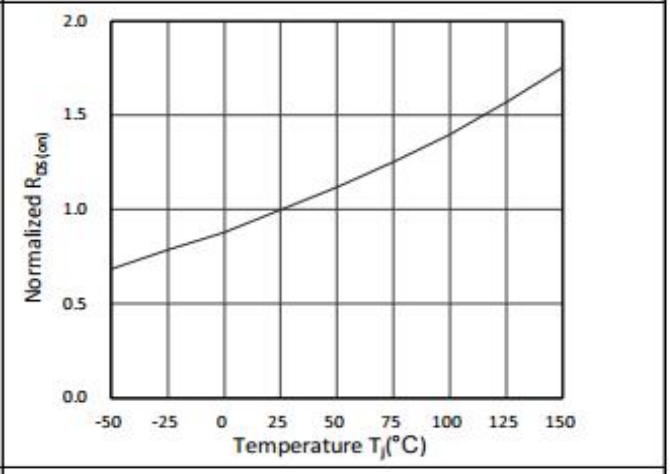


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

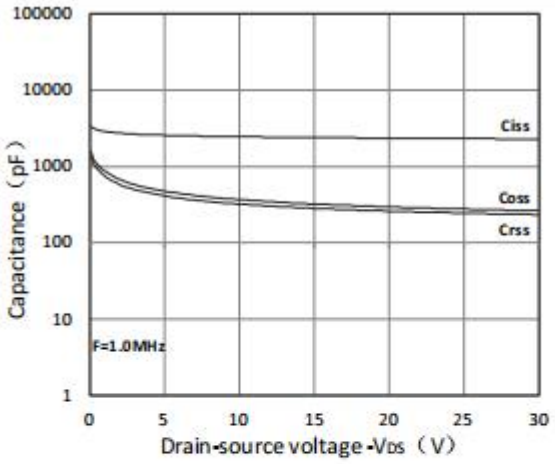


Figure 7. Capacitance Characteristics

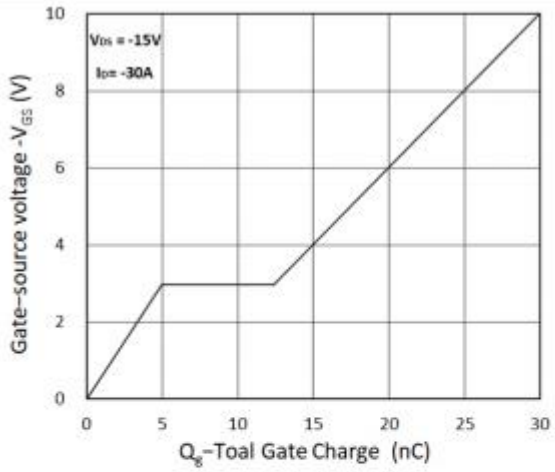


Figure 8. Gate Charge Characteristics

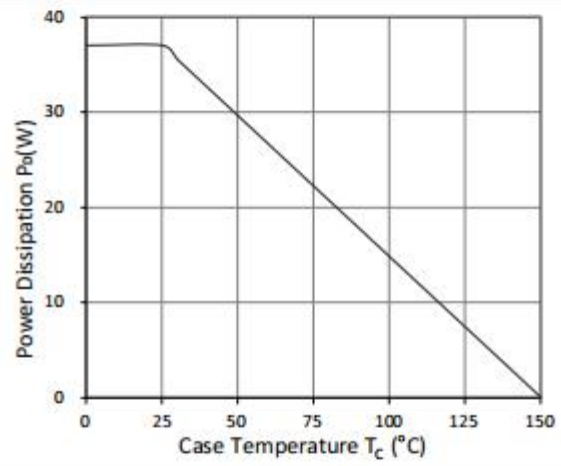


Figure 9. Power Dissipation

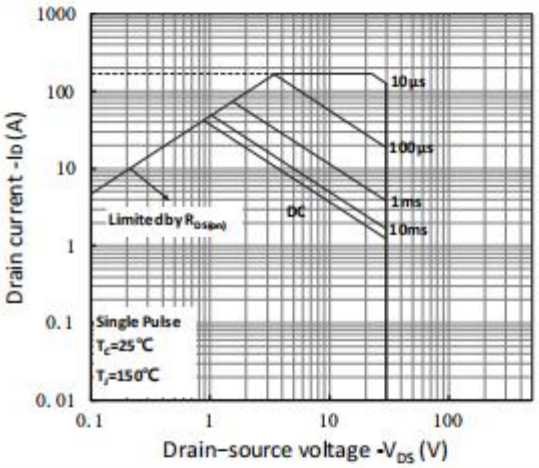


Figure10. Safe Operating Area

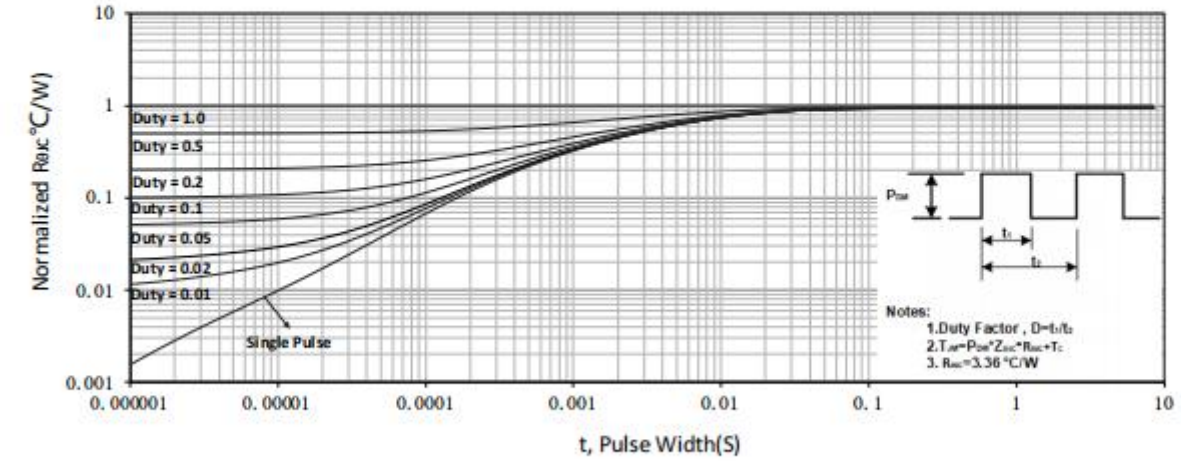
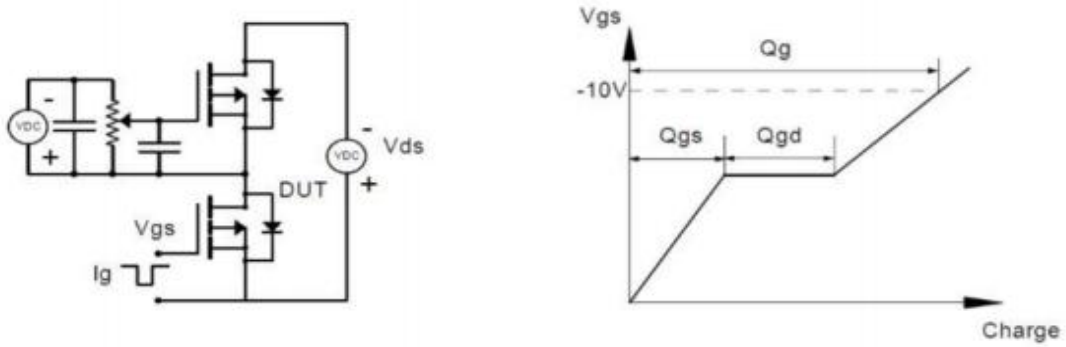


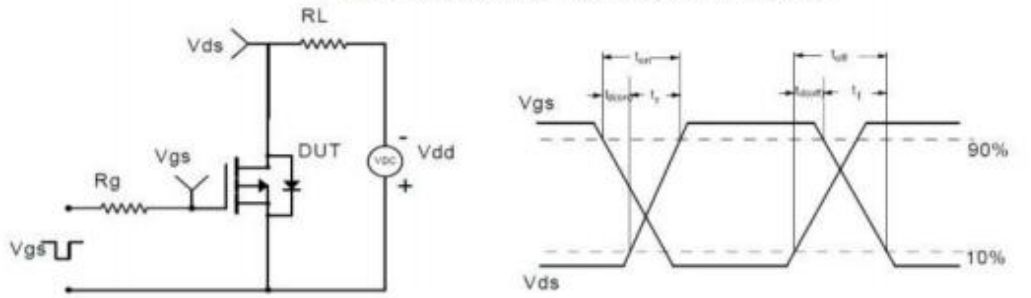
Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

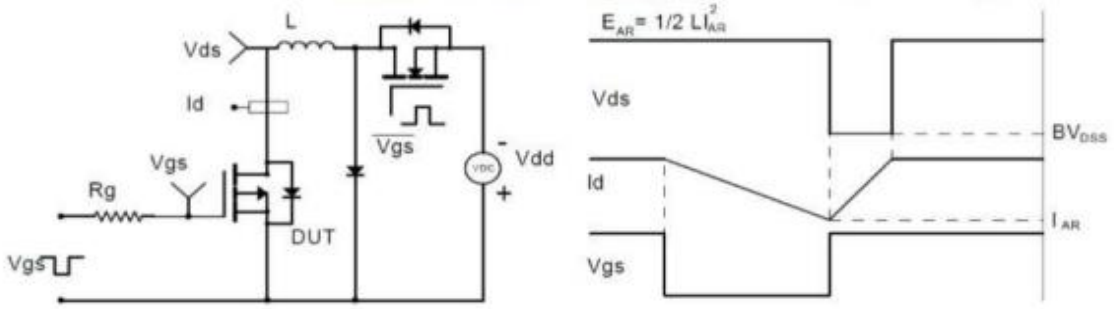
Gate Charge Test Circuit & Waveform



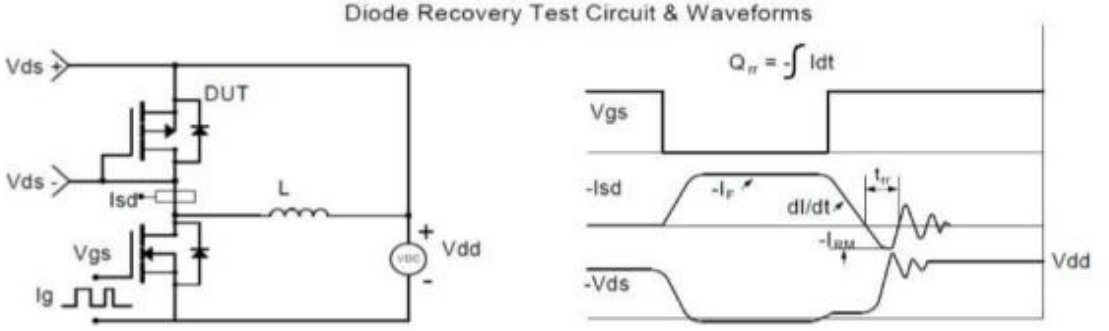
Resistive Switching Test Circuit & Waveforms



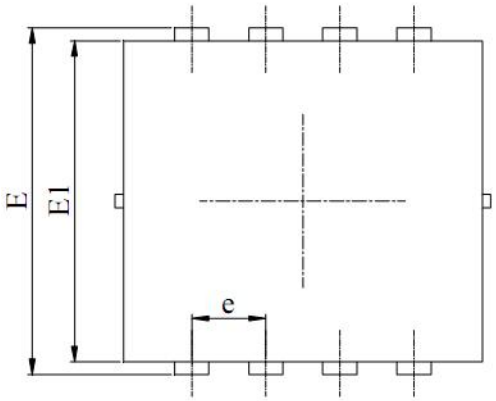
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



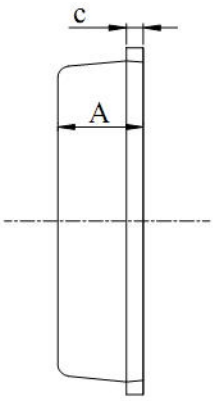
Diode Recovery Test Circuit & Waveforms



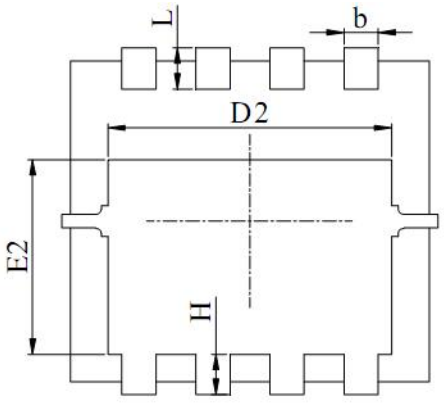
Package Mechanical Data PDFN3x3-8L



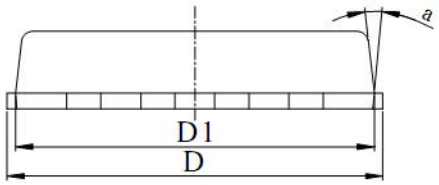
Top View



Side View



Bottom View

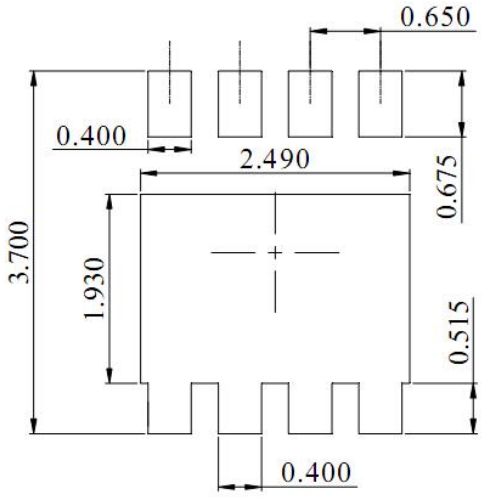


Front View

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS

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