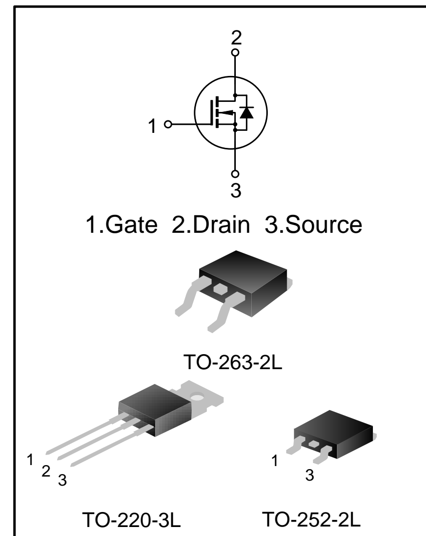
18A, 200V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD640T/D/S is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 18A,200V,$R_{DS(on)(typ.)}$=0.12Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVD640T	TO-220-3L	SVD640T	Pb free	Tube
SVD640D	TO-252-2L	SVD640D	Halogen free	Tube
SVD640DTR	TO-252-2L	SVD640D	Halogen free	Tape&Reel
SVD640S	TO-263-2L	SVD640S	Halogen free	Tube
SVD640STR	TO-263-2L	SVD640S	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (T_c=25°C unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVD640T/S	SVD640D	
Drain-Source Voltage		V_{DS}	200		V
Gate-Source Voltage		V_{GS}	±20		V
Drain Current	T_C=25°C	I_D	18		A
	T_C=100°C		11		
Drain Pulsed Current		I_{DM}	72		A
Power Dissipation(T_C=25°C)		P_D	150	110	W
-Derate above 25°C			1.2	0.88	W/°C
Single Pulsed Avalanche Energy (Note 1)	L=30mH	E_{AS}	635		mJ
	L=10mH		211		mJ
Operation Junction Temperature Range		T_J	150		°C
Storage Temperature Range		T_{stg}	-65～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Typ.		Unit.
		SVD640T/S	SVD640D	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.83	1.14	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit.
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	200	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=200V, V_{GS}=0V	--	--	1	μA
		V_{DS}=200V,V_{GS}=0V,T_C=125°C	--	--	1.0	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	3.0	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=9A	--	0.12	0.15	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	1108	--	pF
Output Capacitance	C_{oss}		--	160	--	
Reverse Transfer Capacitance	C_{rss}		--	34	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=100V, V_{GS}=10V, R_G=2.5Ω, I_D=11A （Notes2，3）	--	15	--	ns
Turn-on Rise Time	t_r		--	47	--	
Turn-off Delay Time	$t_{d(off)}$		--	110	--	
Turn-off Fall Time	t_f		--	36	--	
Total Gate Charge	Q_g	V_{DD}=160V, V_{GS}=10V, I_D=11A （Notes2，3）	--	41	--	nC
Gate-Source Charge	Q_{gs}		--	6.0	--	
Gate-Drain Charge	Q_{gd}		--	20	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	18	A
Pulsed Source Current	I_{SM}		--	--	72	
Diode Forward Voltage	V_{SD}	I_S=11A,V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	T_{rr}	V_{DD}=50V, di/dt=100A/μS, I_F=11A (Note 2)	--	160	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.98	--	μC

Notes:

1. V_{DD}=100V, R_G=25Ω,starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

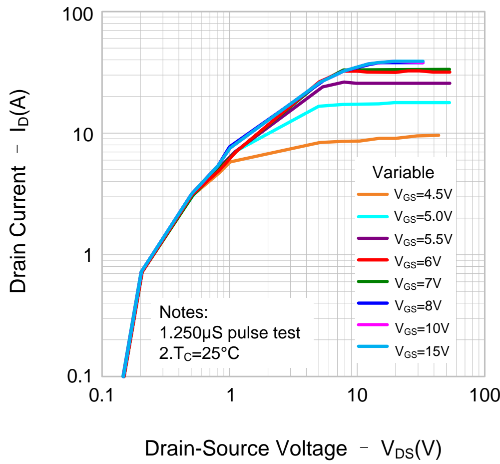


Figure 2. Transfer Characteristics

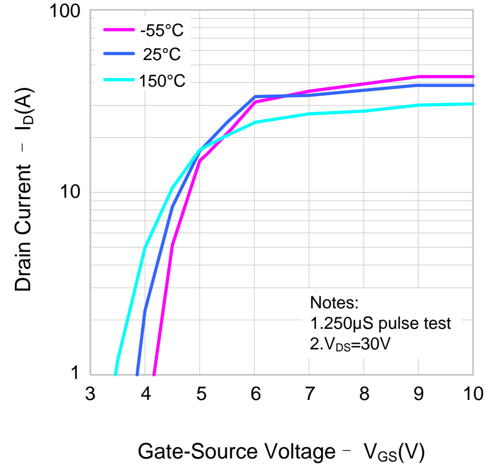


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

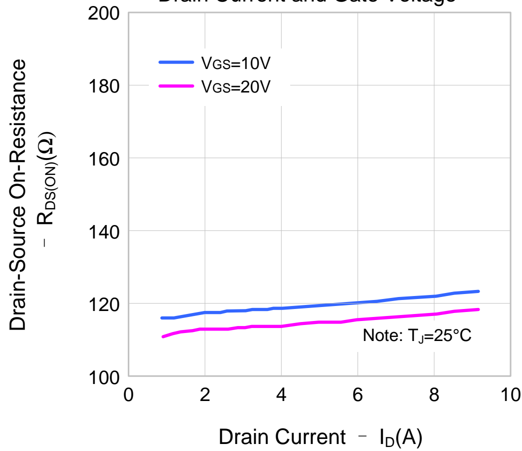


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

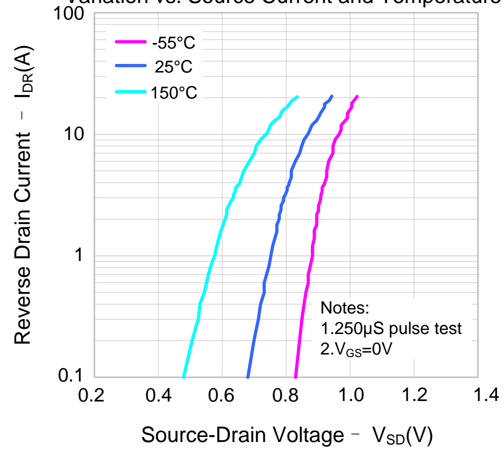


Figure 5. Capacitance Characteristics

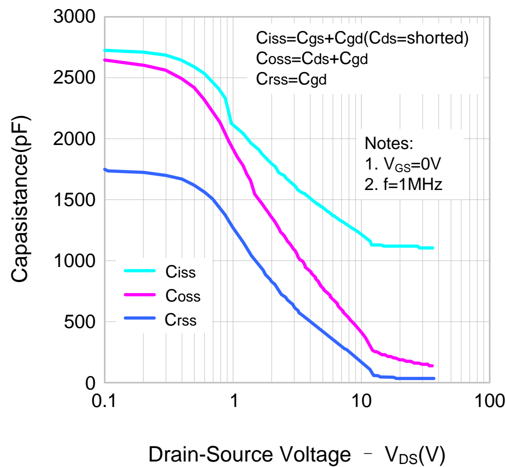
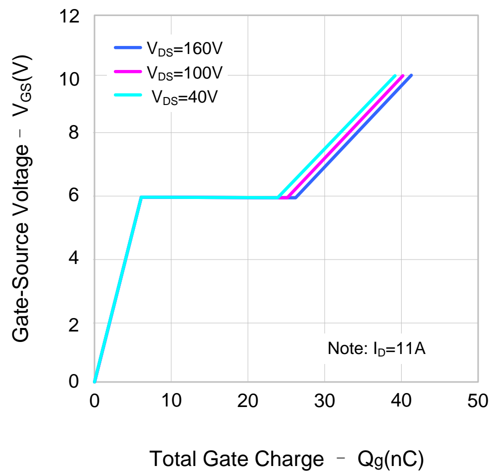
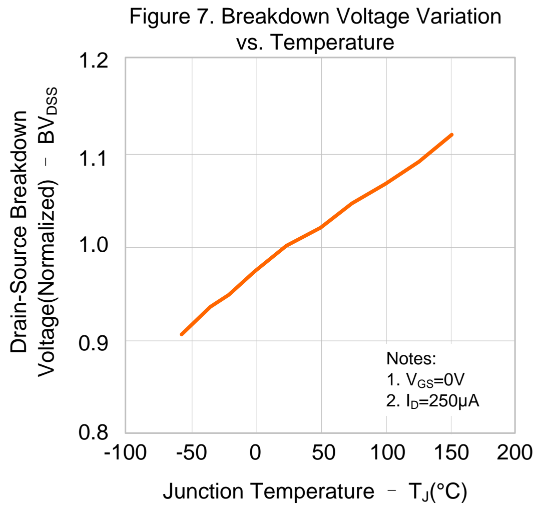
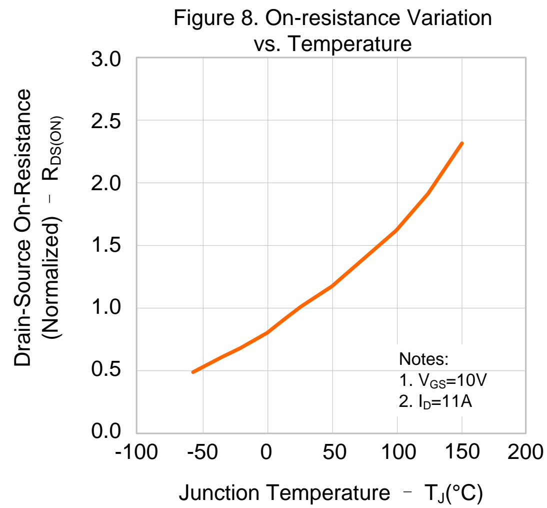


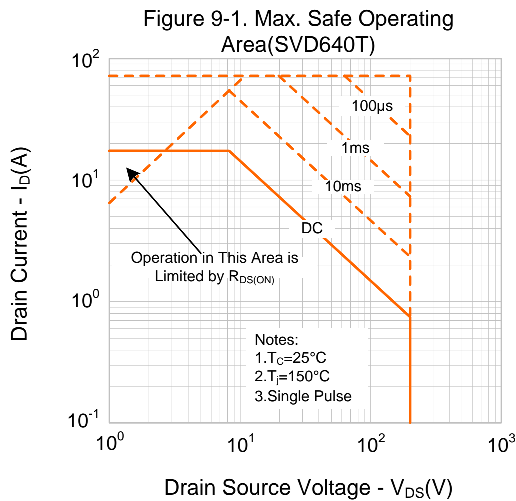
Figure 6. Gate Charge Characteristics

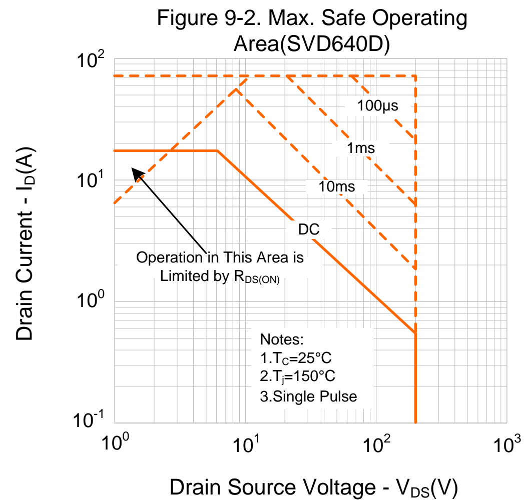


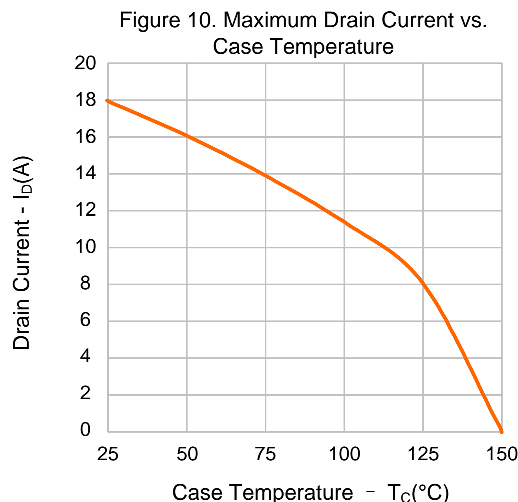
TYPICAL CHARACTERISTICS(continued)



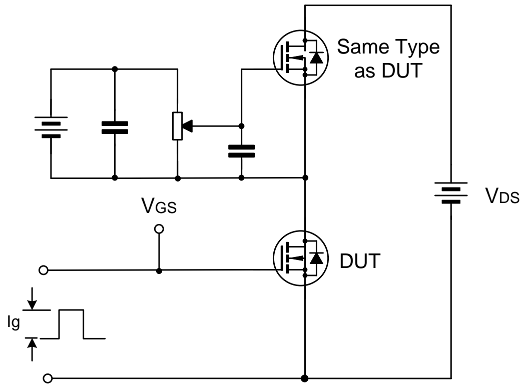


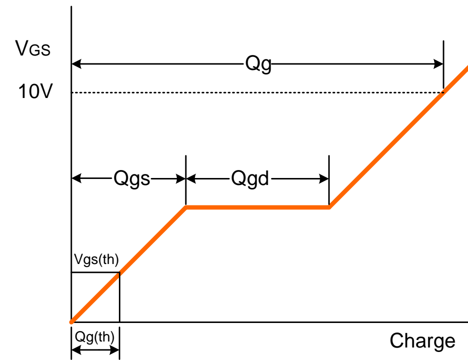




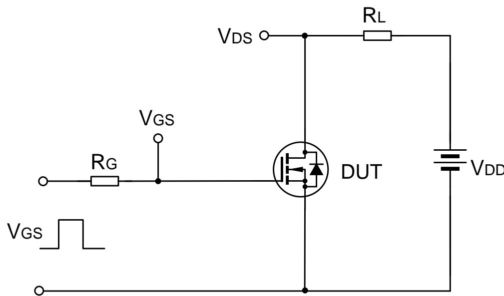


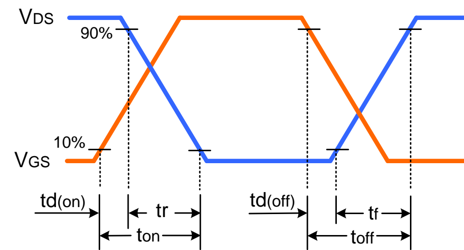
TYPICAL TEST CIRCUIT



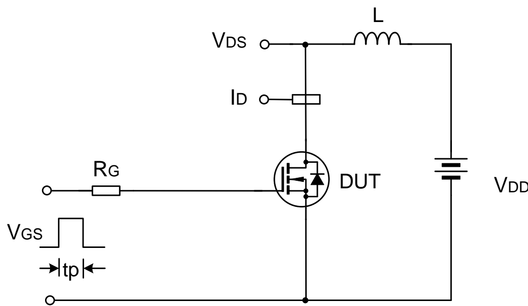


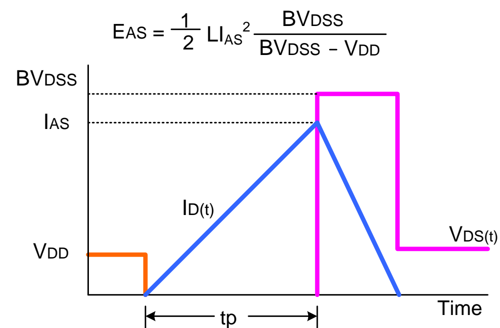
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveform

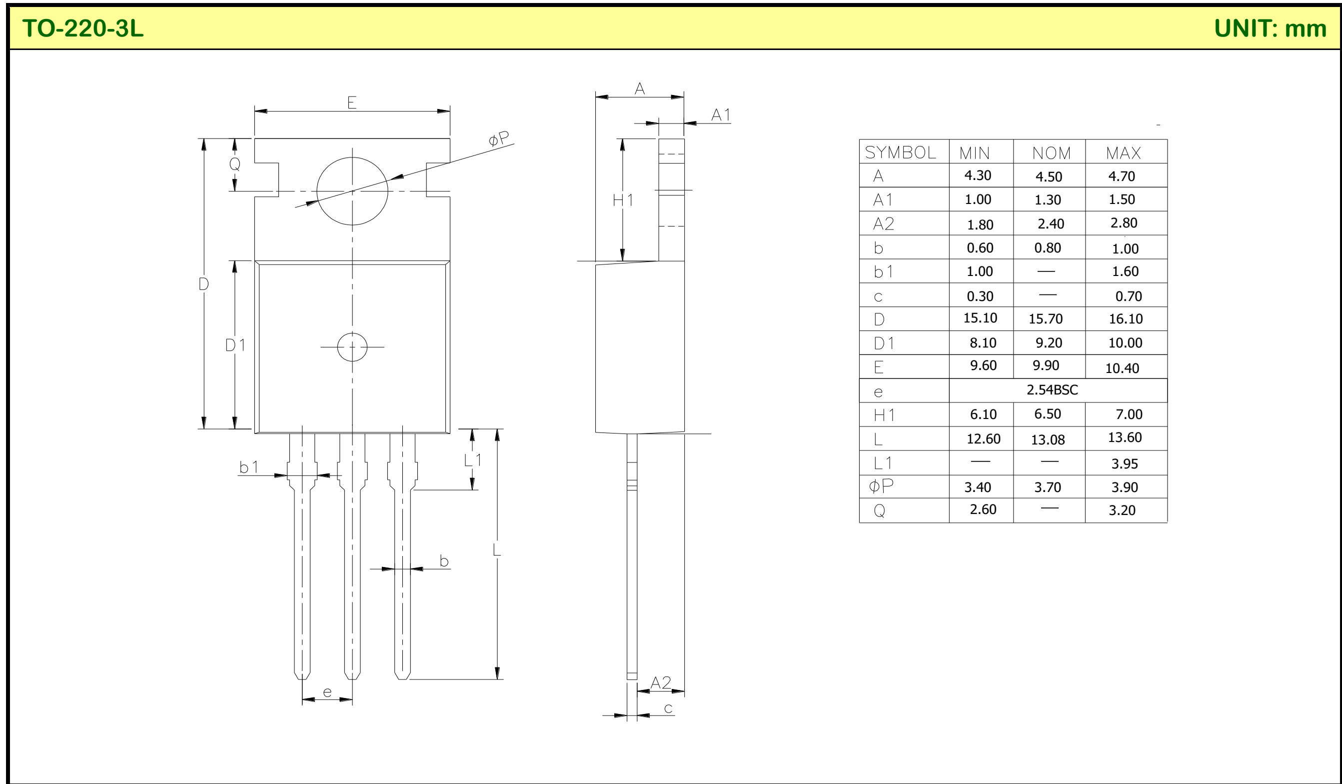




Unclamped Inductive Switching Test Circuit & Waveform

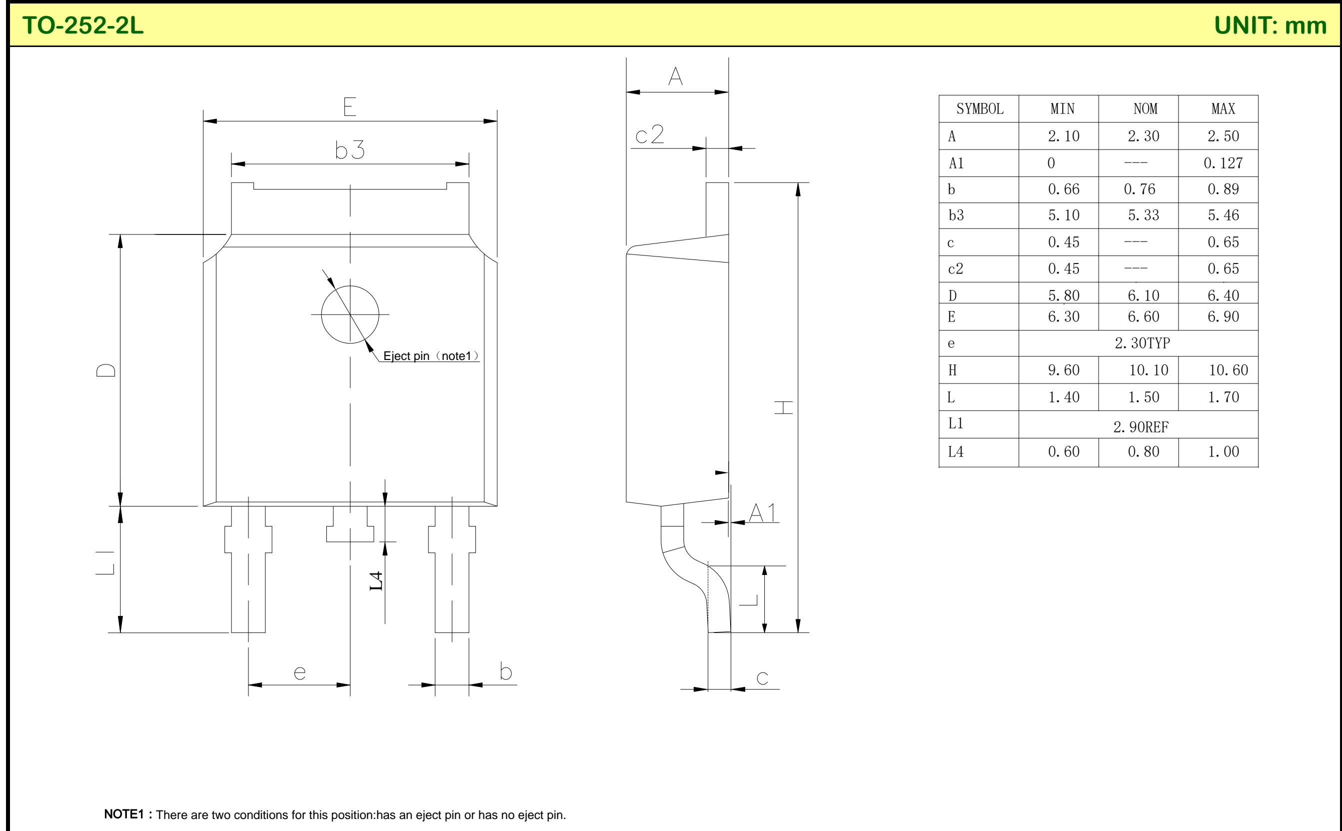
PACKAGE OUTLINE

TO-220-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ΦP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-252-2L **UNIT: mm**

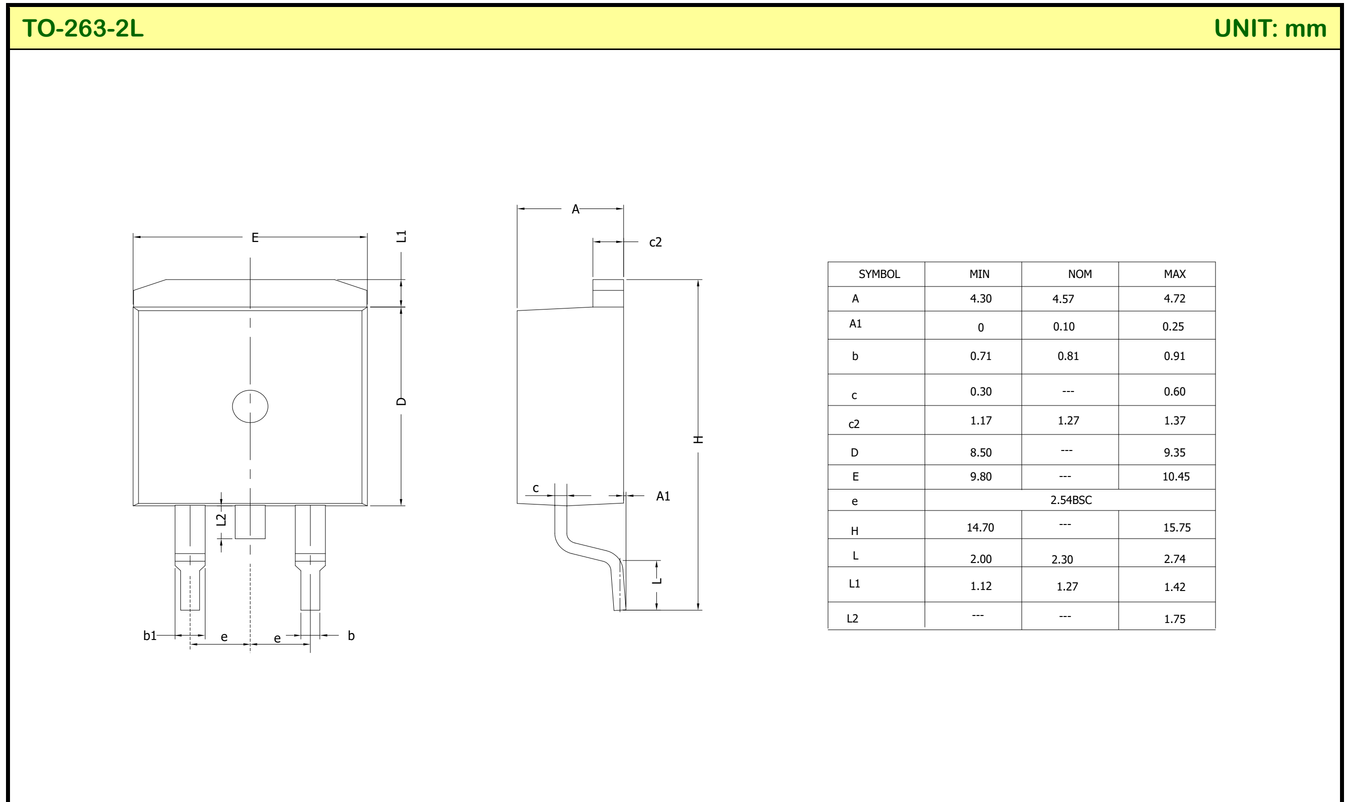


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE (continued)

TO-263-2L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.57	4.72
A1	0	0.10	0.25
b	0.71	0.81	0.91
c	0.30	---	0.60
c2	1.17	1.27	1.37
D	8.50	---	9.35
E	9.80	---	10.45
e	2.54BSC		
H	14.70	---	15.75
L	2.00	2.30	2.74
L1	1.12	1.27	1.42
L2	---	---	1.75

Important notice :

- **The instructions are subject to change without notice！ Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
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Rev.: 1.4

Revision History:

1. Add SVD640S(To-263-2L) encapsulation
2. Add parameters and curves with SVD640T
3. Modify ORDERING INFORMATION
4. Modify TYPICAL TEST CIRCUIT
5. Modify Important notice

Rev.: 1.3

Revision History:

1. Add the EAS value under L=10mH
2. Update the package outline of TO-220-3L

Rev.: 1.2

Revision History:

1. Delete the package information of TO-220F-3L

Rev.: 1.1

Revision History:

1. Modify the package information of TO-220F-3L
2. Modify the package information of TO-252-2L
3. Modify the package information of TO-220-3L

Rev.: 1.0

Revision History:

1. First release