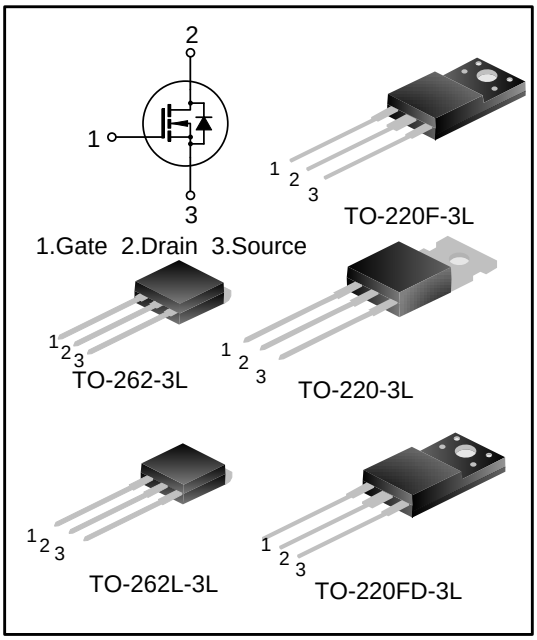
7A, 800V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF7N80T/F/KL/K/FD is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drives.



FEATURES

- 7A,800V,$R_{DS(on)(typ.)}$=1.39Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF7N80T	TO-220-3L	SVF7N80T	Pb free	Tube
SVF7N80F	TO-220F-3L	SVF7N80F	Pb free	Tube
SVF7N80KL	TO-262L-3L	SVF7N80KL	Pb free	Tube
SVF7N80K	TO-262-3L	SVF7N80K	Pb free	Tube
SVF7N80FD	TO-220FD-3L	SVF7N80FD	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings			Unit
			SVF7N80T	SVF7N80F/FD	SVF7N80KL/K	
Drain-Source Voltage		V_{DS}	800			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	7.0			A
	T_C=100°C		4.4			
Drain Current Pulsed		I_{DM}	28.0			A
Power Dissipation(T_C=25°C)		P_D	154	50	150	W
-Derate above 25°C			1.23	0.40	1.20	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	534			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF7N80T	SVF7N80F/FD	SVF7N80KL/K	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.81	2.50	0.83	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	800	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=800V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	1.4	1.6	Ω
Gate Resistance	R_g	f=1MHz	--	4.6	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	---	1087	---	pF
Output Capacitance	C_{oss}		--	104	--	
Reverse Transfer Capacitance	C_{rss}		--	5.7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=400V, R_G=25Ω , I_D=7.0A (Note 2,3)	--	34	--	ns
Turn-on Rise Time	t_r		--	72	--	
Turn-off Delay Time	$t_{d(off)}$		--	63	--	
Turn-off Fall Time	t_f		--	35	--	
Total Gate Charge	Q_g	V_{DS}=640V, I_D=7.0A, V_{GS}=10V (Note 2,3)	--	23	--	nC
Gate-Source Charge	Q_{gs}		--	7.0	--	
Gate-Drain Charge	Q_{gd}		--	9.0	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	7.0	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	28	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=7.0A,V_{GS}=0V,	--	590	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μS (Note2)	--	3.9	--	μC

Notes:

1. L=30mH, I_{AS}=5.50A, V_{DD}=100V, R_G=20Ω, starting TB_{JB}=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

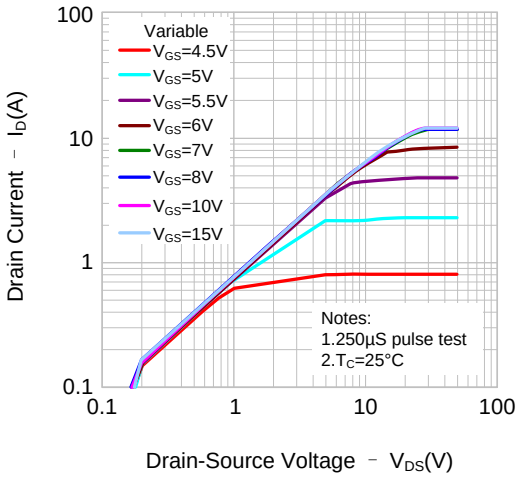


Figure 2. Transfer Characteristics

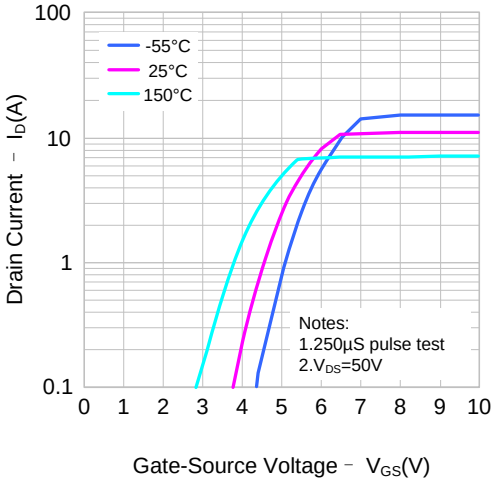


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

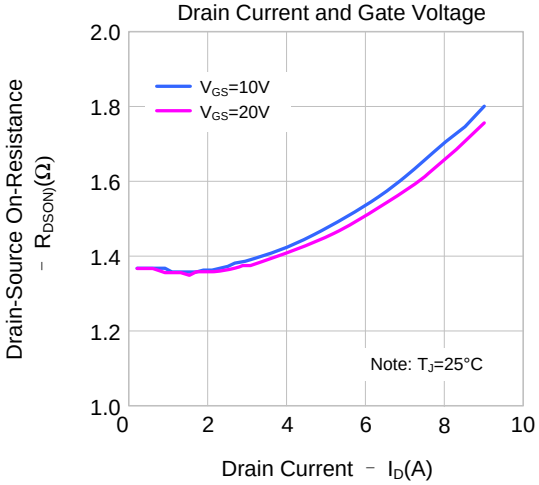


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

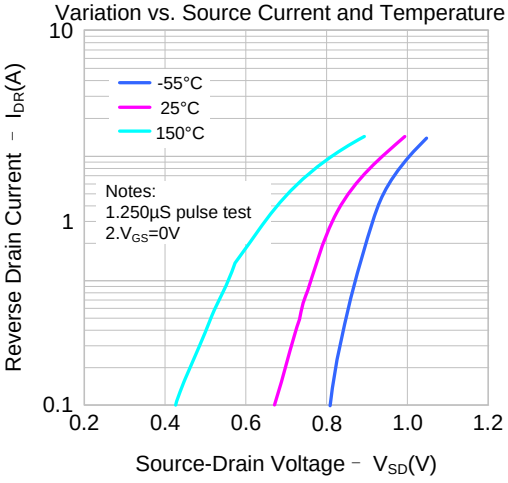


Figure 5. Capacitance Characteristics

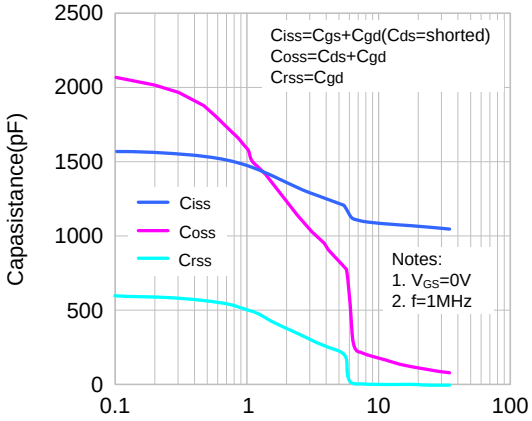
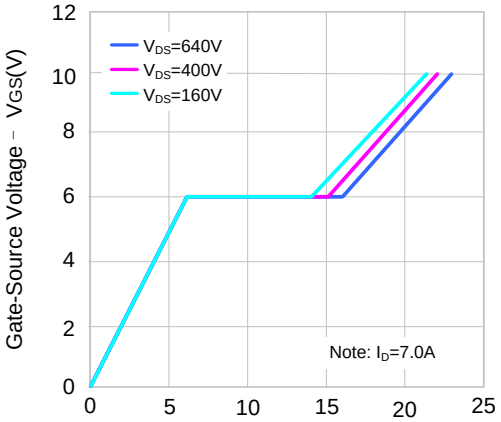


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

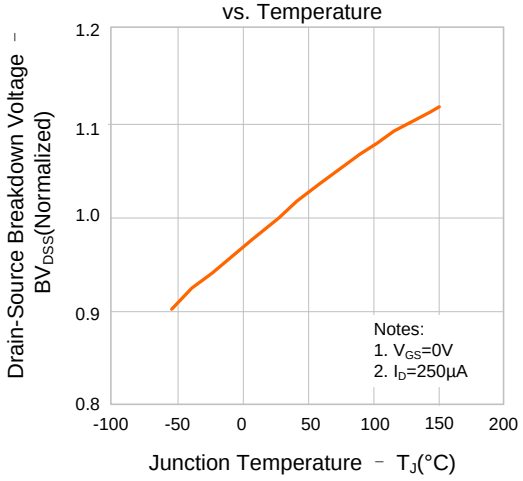


Figure 8. On-resistance Variation vs. Temperature

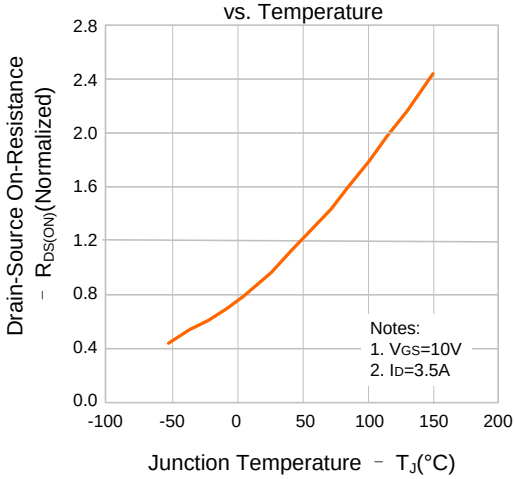


Figure 9-1. Max. Safe Operating Area(SVF7N80T)

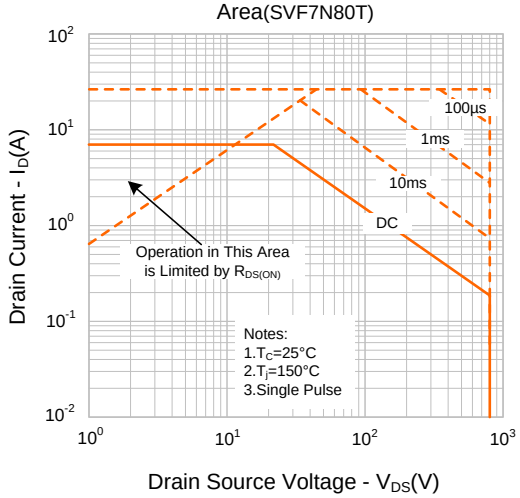


Figure 9-2. Max. Safe Operating Area(SVF7N80F/FD)

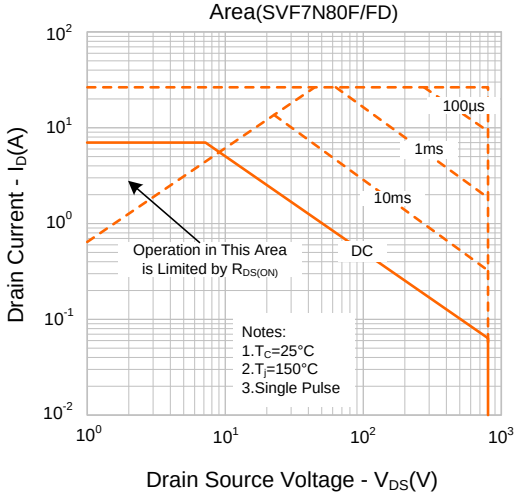


Figure 9-3. Max. Safe Operating Area(SVF7N80KL/K)

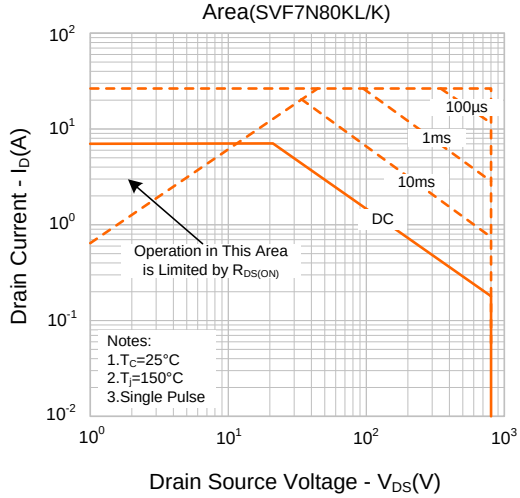
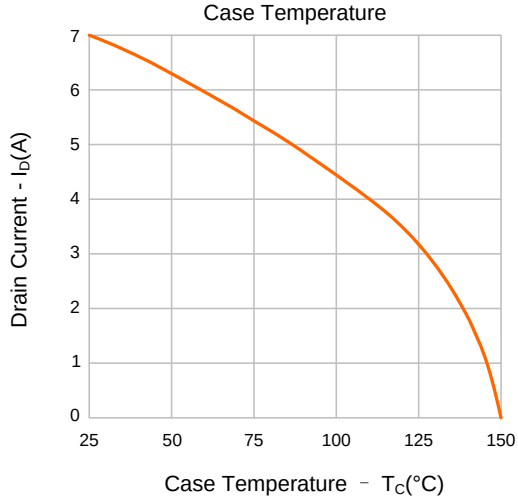
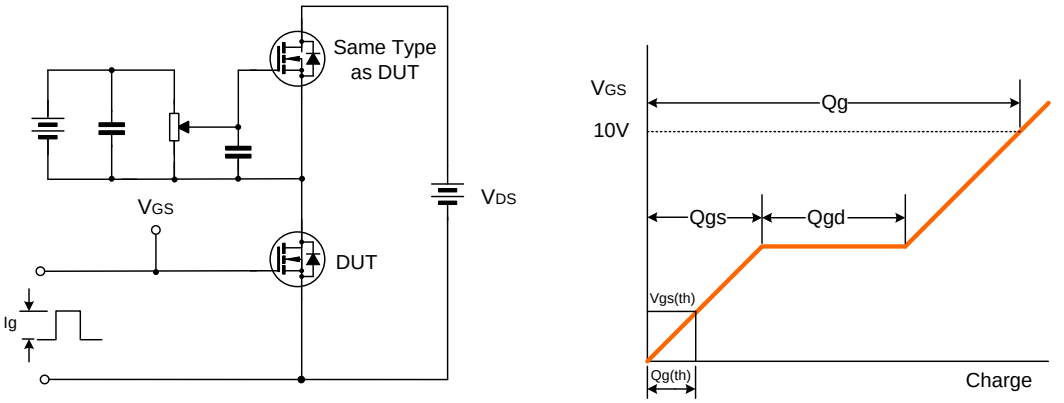


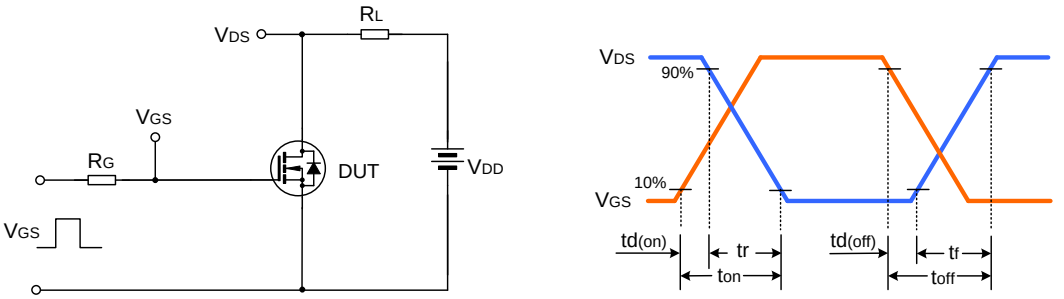
Figure 10. Maximum Drain Current vs. Case Temperature



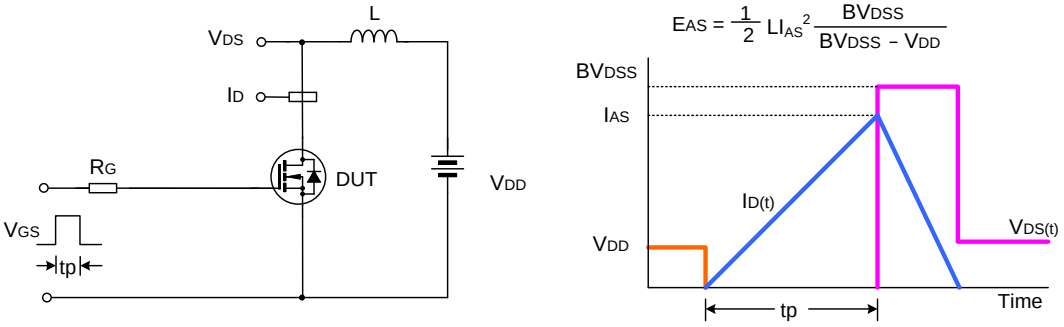
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

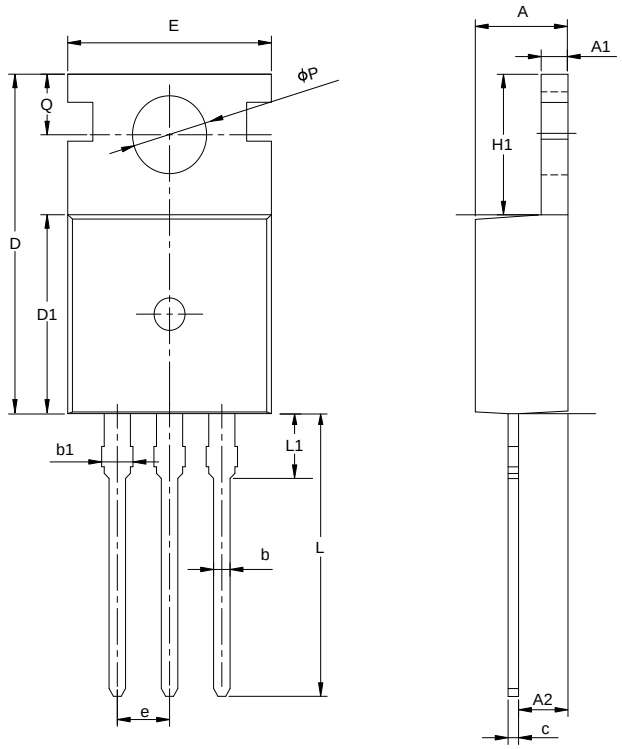


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-220-3L

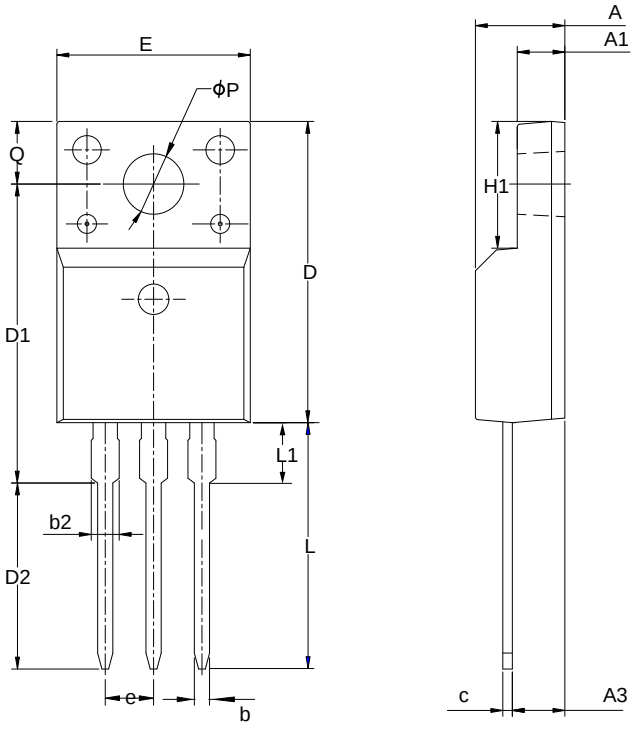
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-220F-3L

UNIT: mm

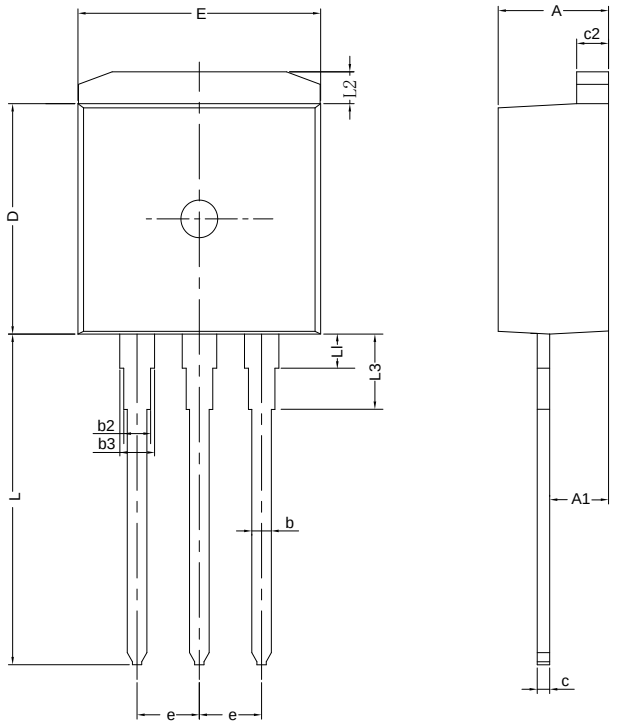


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE(CONTINUED)

TO-262L-3L

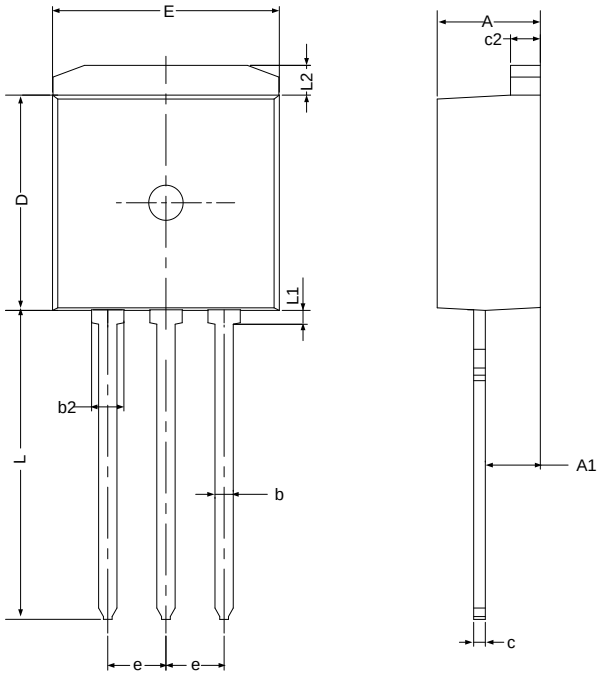
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.88
b2	0.90	1.01	1.08
b3	1.20	—	1.50
c	0.34	—	0.76
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	1.40	1.50	1.60
L2	1.12	—	1.42
L3	3.00	3.20	3.40

TO-262-3L

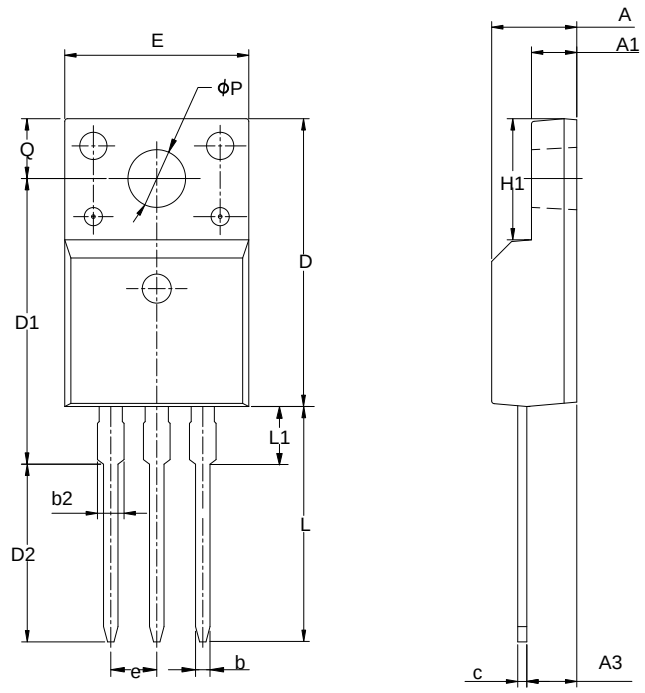
UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	2.20	—	2.92
b	0.71	0.80	0.90
b2	1.20	—	1.50
c	0.34	—	0.65
c2	1.22	1.30	1.35
D	8.38	—	9.30
E	9.80	10.16	10.54
e	2.54 BSC		
L	12.80	—	14.10
L1	—	—	0.75
L2	1.12	—	1.42

PACKAGE OUTLINE(CONTINUED)

TO-220FD-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

Important notice :

- **The instructions are subject to change without notice！ Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **Our products are consumer electronic products, and / or civil electronic products.**
- **When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.**
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Part No.:	SVF7N80T/F/KL/K/FD	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.: 2.9

Revision History:

1. Deleted NOMENCLATURE
2. Modify Important notice

Rev.: 2.8

Revision History:

1. Add SVF7N80FD (to-220FD-3L) package
2. Add parameters and curves with SVF7N80F
3. Update corresponding electrical diagram and typical circuit diagram
4. Modify NOMENCLATURE
5. Modify TYPICAL TEST CIRCUIT
6. Modify Important notice

Rev.: 2.7

Revision History:

1. Add the package outline of TO-262-3L

Rev.: 2.6

Revision History:

1. Add the package outline of TO-262L-3L
2. Delete the package outline of TO-262-3L

Rev.: 2.5

Revision History:

1. Update the package outline of TO-262-3L
2. Add another 3D image of TO-220-3L

Rev.: 2.4

Revision History:

1. Delete the package outline of TO-262L-3L

Rev.: 2.3

Revision History:

1. Update the package outline of TO-262-3L

Rev.: 2.2

Revision History:

1. Add the package outline of TO-262L-3L

Rev.: 2.1

Revision History:

1. Modify the ordering information
2. Modify the package outline of TO-262-3L

Rev.: 2.0

Revision History:

1. Modify the ordering information

2. Modify the package outline of TO-220-3L

Rev.: 1.9

Revision History:

1. Modify the ordering information

Rev.: 1.8

Revision History:

1. Modify the thermal characteristics

Rev.: 1.7

Revision History:

1. Add the package of TO-262-3L

Rev.: 1.6

Revision History:

1. Modify the ordering information

Rev.: 1.5

Revision History:

1. Change the schematic diagram of MOS
2. Modify the figure 7 and figure 8

Rev.: 1.4

Revision History:

1. Modify the figure 7 and figure 8

Rev.: 1.3

Revision History:

1. Modify the values of T_{rr} and Q_{rr}

Rev.: 1.2

Revision History:

1. Modify “ORDERING INFORMATION”

Rev.: 1.1

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.0

Revision History:

1. Initial release