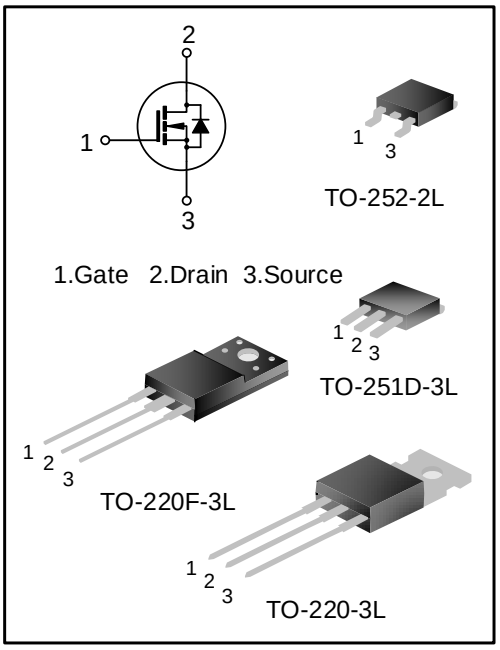
4A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF4N60D/F/T/M is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 4A, 600V, $R_{DS(on)(typ.)}$=2.0Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVF4N60F	TO-220F-3L	SVF4N60F	Pb free	Tube
SVF4N60T	TO-220-3L	SVF4N60T	Pb free	Tube
SVF4N60DTR	TO-252-2L	SVF4N60D	Halogen free	Tape & Reel
SVF4N60M	TO-251D-3L	SVF4N60M	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings			Unit
			SVF4N60F	SVF4N60D/M	SVF4N60T	
Drain-Source Voltage		V_{DS}	600			V
Gate-Source Voltage		V_{GS}	±30			V
Drain Current	T_C=25°C	I_D	4.0			A
	T_C=100°C		2.5			
Drain Current Pulsed		I_{DM}	16			A
Power Dissipation(T_C=25°C)		P_D	33	77	110	W
-Derate above 25°C			0.26	0.62	0.88	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	217			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVF4N60F	SVF4N60D/M	SVF4N60T	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.85	1.61	1.14	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2.0A	--	2.0	2.4	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	--	433	--	pF
Output Capacitance	C_{oss}		--	55	--	
Reverse Transfer Capacitance	C_{rss}		--	4.5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V, I_D=4A, R_G=25Ω (Note2,3)	--	10	--	ns
Turn-on Rise Time	t_r		--	26	--	
Turn-off Delay Time	$t_{d(off)}$		--	29	--	
Turn-off Fall Time	t_f		--	26	--	
Total Gate Charge	Q_g	V_{DS}=480V, I_D=4A, V_{GS}=10V (Note 2,3)	--	13	--	nC
Gate-Source Charge	Q_{gs}		--	2.8	--	
Gate-Drain Charge	Q_{gd}		--	6.2	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 2)	--	420	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.75	--	μC

Notes:

1. L=30mH, I_{AS}=3.75A, V_{DD}=100V, R_G=25Ω, starting TB_{JB}=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

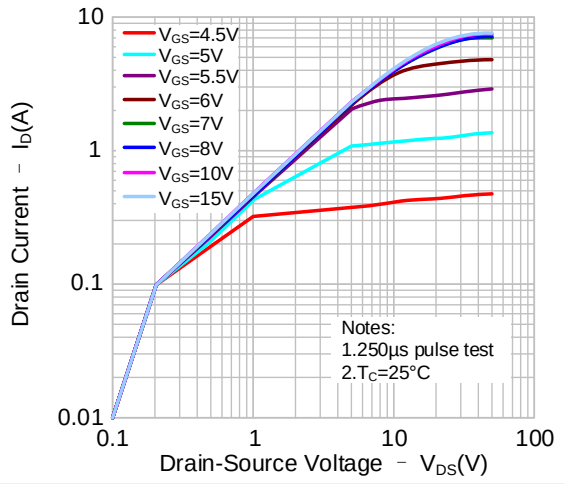


Figure 2. Transfer Characteristics

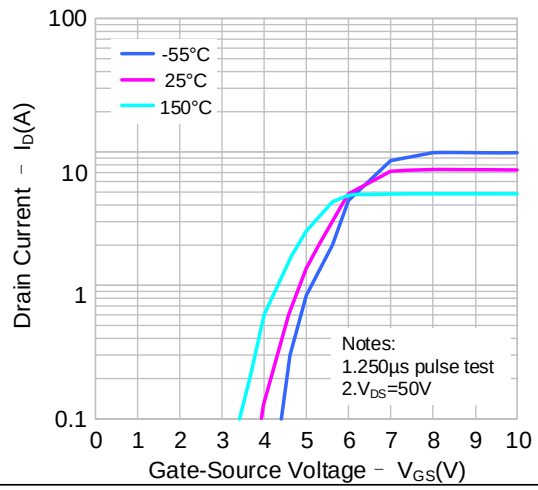


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

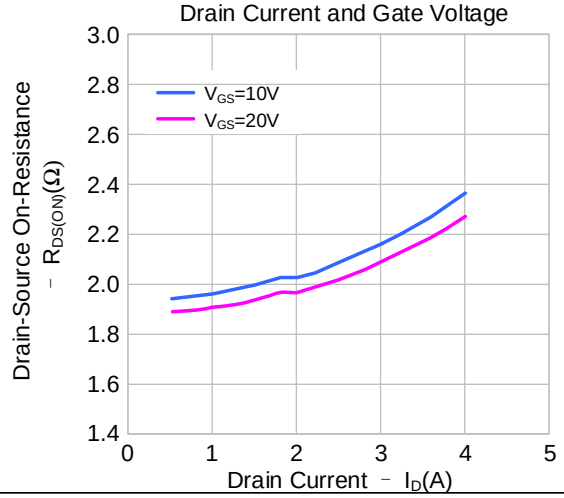


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

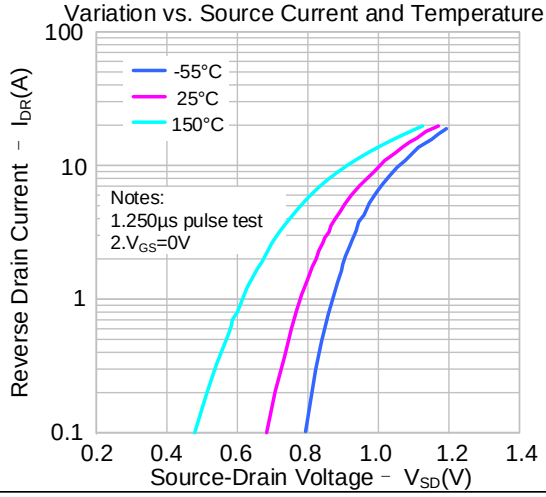


Figure 5. Capacitance Characteristics

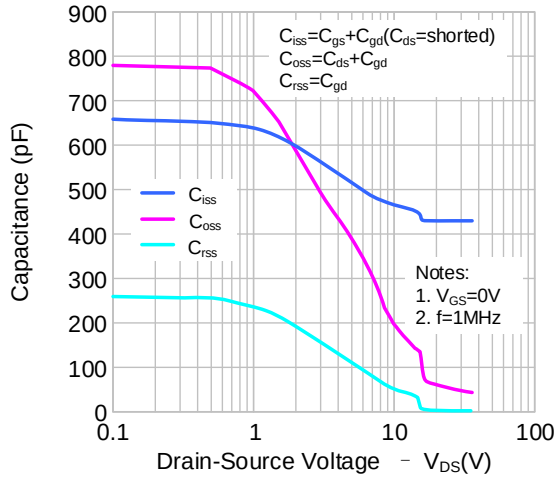
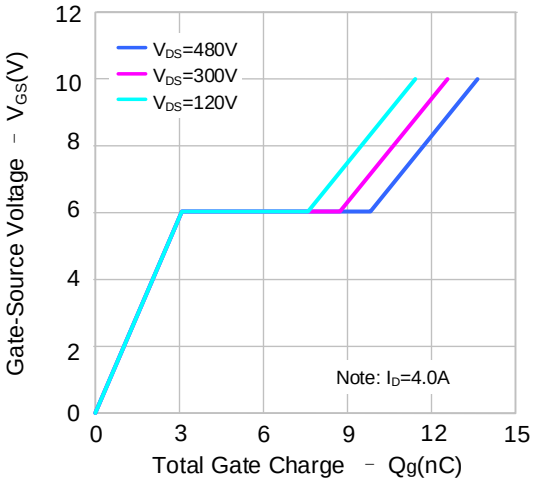


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS (CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

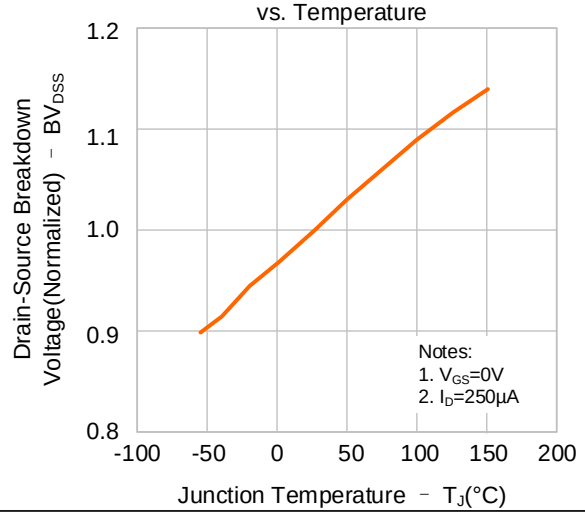


Figure 8. On-resistance Variation vs. Temperature

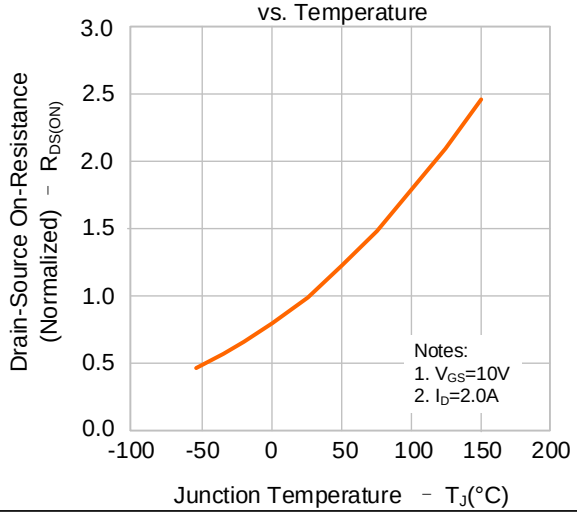


Figure 9-1. Max. Safe Operating Area(SVF4N60F)

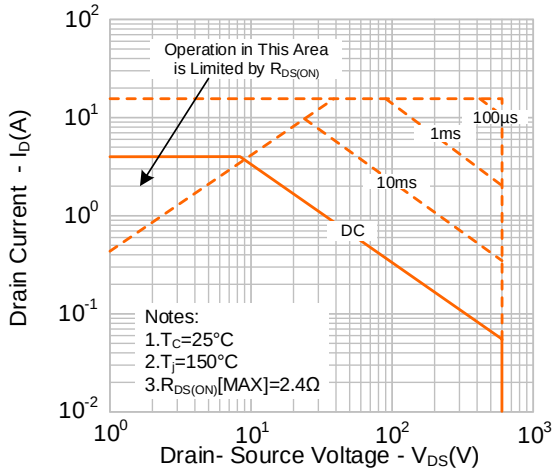


Figure 9-2. Max. Safe Operating Area(SVF4N60D/M)

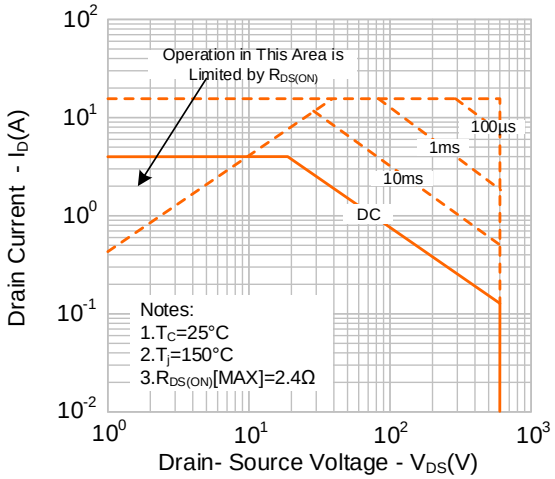


Figure 9-3. Max. Safe Operating Area(SVF4N60T)

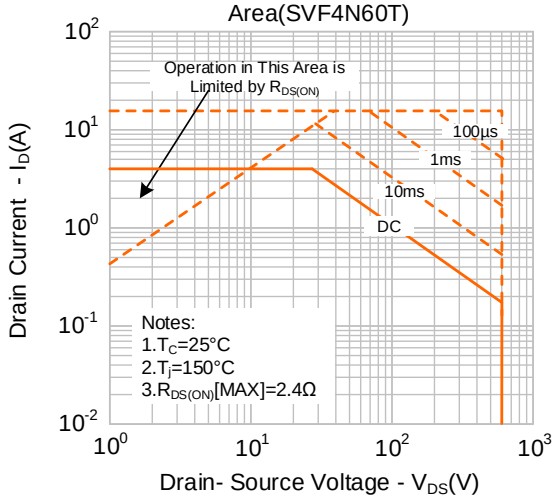
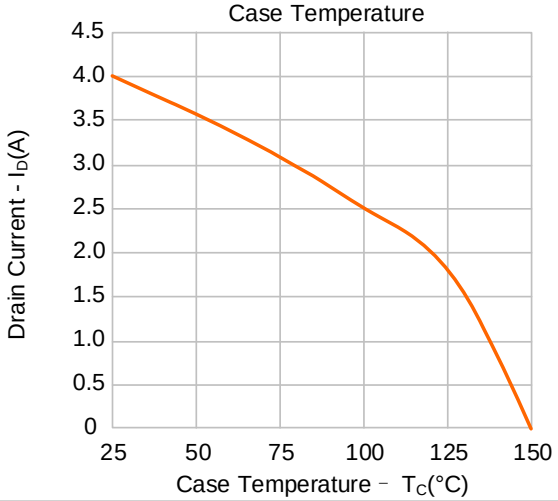
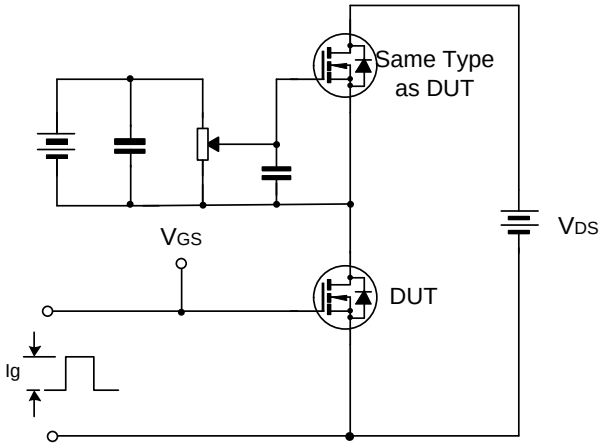


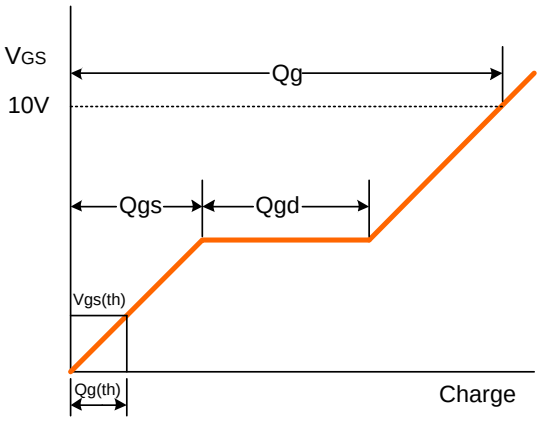
Figure 10. Maximum Drain Current vs. Case Temperature



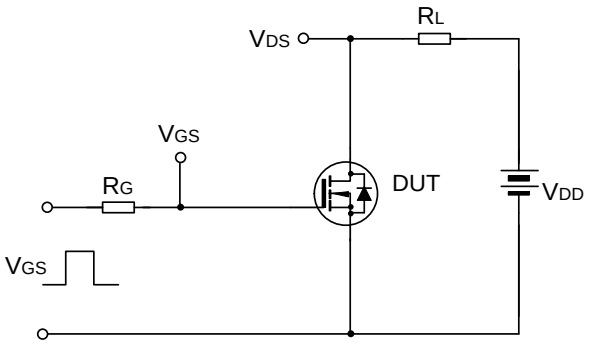
TYPICAL TEST CIRCUIT

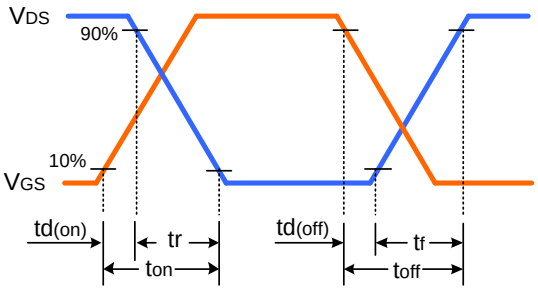
Gate Charge Test Circuit & Waveform



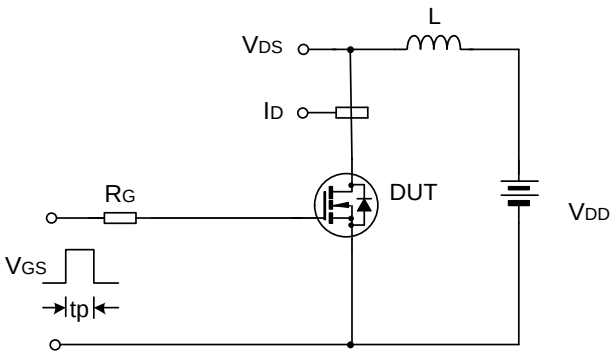


Resistive Switching Test Circuit & Waveform

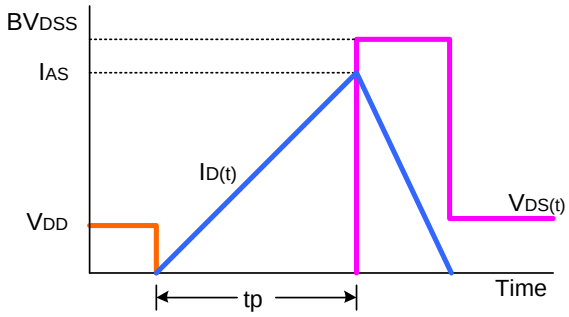




Unclamped Inductive Switching Test Circuit & Waveform

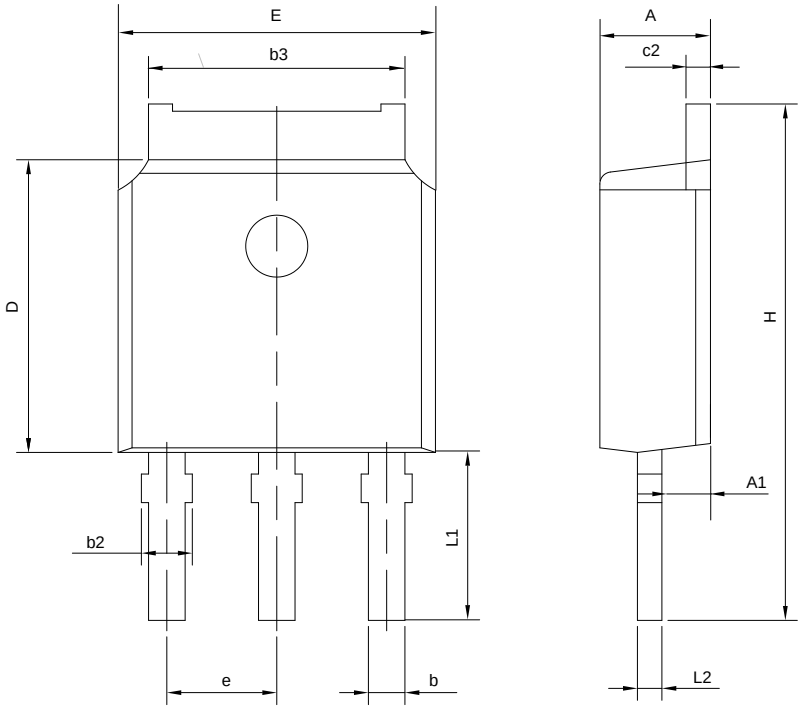


$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



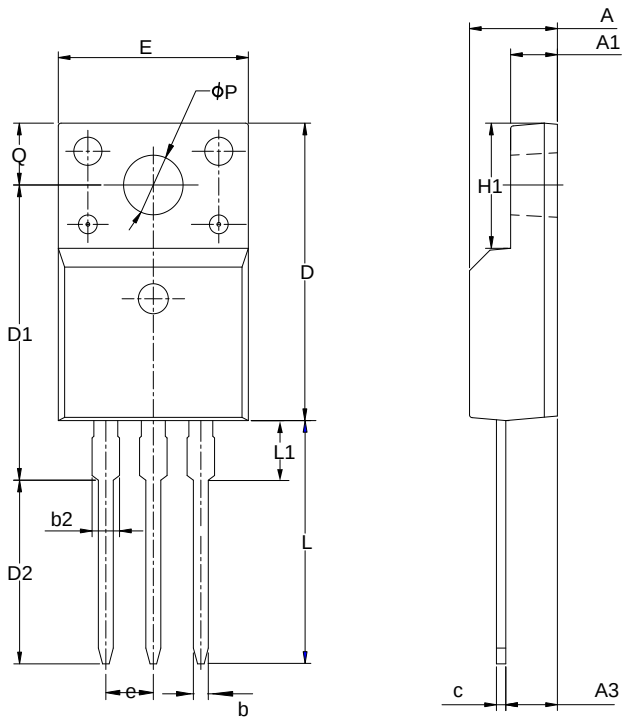
PACKAGE OUTLINE

TO-251D-3L **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.66	–	0.86
b2	0.72	–	0.90
b3	5.10	5.33	5.46
c2	0.46	–	0.60
D	6.00	6.10	6.20
E	6.50	6.60	6.70
e	2.186	2.286	2.386
H	10.40	10.70	11.00
L1	3.50 REF		
L2	0.508 BSC		

TO-220F-3L **UNIT: mm**

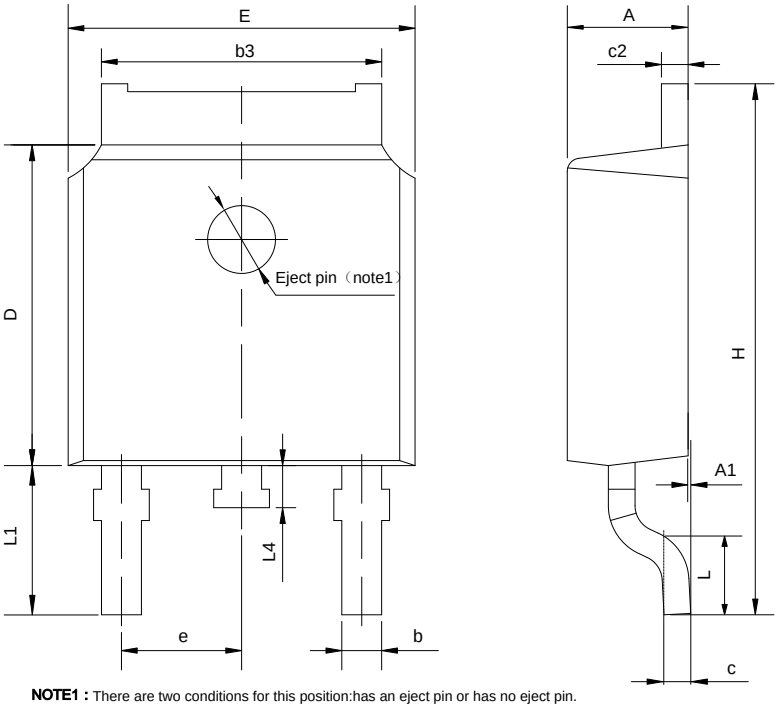


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	–	–	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BSC		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	–	–	3.50
ϕP	3.00	3.18	3.40
Q	3.05	3.30	3.55

PACKAGE OUTLINE (CONTINUED)

TO-252-2L

单位:毫米

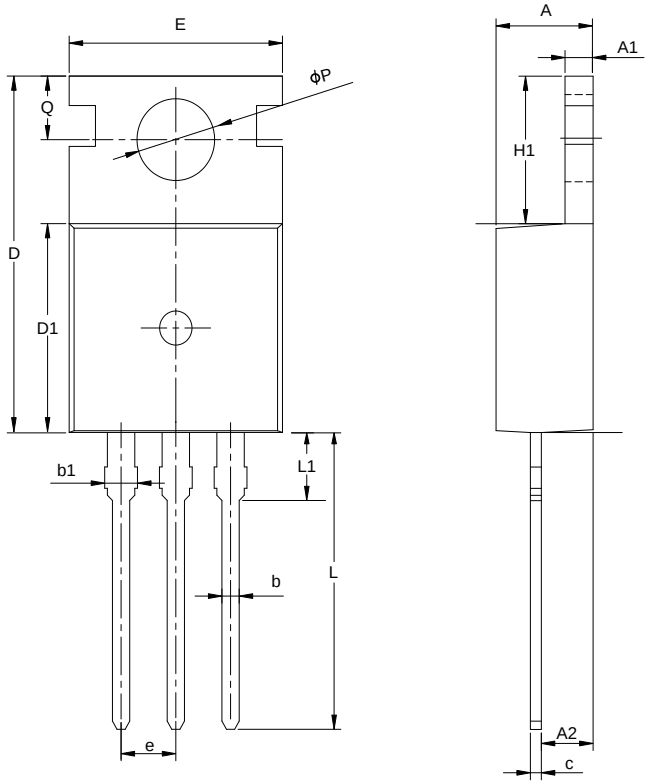


NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

TO-220-3L

单位：毫米



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

Important notice :

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Rev.: 3.5

Revision History:

1. Modify electrical diagram and typical circuit diagram
2. Update the template of characteristic curves
3. Update the important notice
4. Update the package outlines

Rev.: 3.4

Revision History:

1. Delete the package outline of TO-251J-3L
2. Delete the package outline of TO-262-3L

Rev.: 3.3

Revision History:

1. Update the package outline of TO-251J-3L
2. Delete the package outline of TO-220F-3L(2)

Rev.: 3.2

Revision History:

1. Update Electrical characteristics

Rev.: 3.1

Revision History:

1. Modify the Ordering information

Rev.: 3.0

Revision History:

1. Modify the Ordering information
2. Modify the package information of TO-262-3L and TO-251J-3L

Rev.: 2.8

Revision History:

1. Modify the package information of TO-220F-3L
2. Modify the package information of TO-252-2L

Rev.: 2.7

Revision History:

1. Modify the thermal characteristics

Rev.: 2.6

Revision History:

1. Add the pin No

Rev.: 2.5

Revision History:

1. Modify the package outline of TO-251J-3L

Rev.: 2.4

Revision History:

1. Modify the ordering information

Rev.: 2.3

Revision History:

1. Modify the electrical characteristics and typical characteristics

Rev.: 2.2

Revision History:

1. Change the schematic diagram of MOS

Rev.: 2.1

Revision History:

1. Modify the package outline of TO-251D-3L

Rev.: 2.0

Revision History:

1. Update the package outline of TO-262-3L

Rev.: 1.9

Revision History:

1. Add halogen free information of SVF4N60D

Rev.: 1.8

Revision History:

1. Modify “PACKAGE OUTLINE”

Rev.: 1.7

Revision History:

1. Add the halogen free information of SVF4N60MJ

Rev.: 1.6

Revision History:

1. Modify “ELECTRICAL CHARACTERISTICS”

Rev.: 1.5

Revision History:

1. Modify the values of T_{rr} and $Q_{rr;}$ Update the package outline of TO-251D-3L

Rev.: 1.4

Revision History:

1. The package outline of TO-220F-3L(1) and TO-220F-3L(2) are changed.

Rev.: 1.3

Revision History:

1. Add the halogen free information of SVF4N60F

Rev.: 1.2

Revision History:

1. Add the packages of TO-251J-3L and TO-262-3L
2. Delete the package of TO-251-3L

Rev.: 1.1

Revision History:

1. Add the packages of TO-251-3L and TO-251D-3L

Rev.: 1.0

Revision History:

1. Original