

Description:

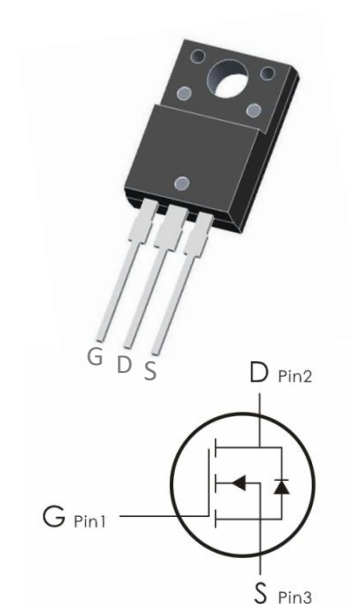
This N-Channel MOSFET uses advanced Planar technology and

design to provide excellent $R_{DS(on)}$ with low gate charge.

It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=650V, I_D=2A, R_{DS(on)} < 5000m\Omega @ V_{GS}=10V$ (Typ: $4400m\Omega$)
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(on)}$.
- 5) Excellent package for good heat dissipation.



Package Marking and Ordering Information:

Part NO.	Marking	Package	Packing
DOPF2N65	2N65	TO- 220F	50 pcs/Tube

Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Continuous Drain Current	2	A
	Continuous Drain Current- $T_C=100^\circ C$	1.4	
I_{DM}	Pulsed Drain Current ¹	8	
P_D	Power Dissipation	28	W
E_{AS}	Single pulse avalanche energy ²	68	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55-+150	$^\circ C$

Thermal Characteristics:

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62	$^\circ C/W$

Electrical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	650	---	---	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} =0V, V _{DS} =650V	---	---	1	μ A
I _{GSS}	Gate-Source Leakage Current	V _{GS} =± 30V, V _{DS} =0A	---	---	± 100	nA
On Characteristics						
V _{GS(th)}	Gate-Source Threshold Voltage	V _{GS} =V _{DS} , I _D =250 μ A	2	---	4	V
R _{DS(ON)}	Drain-Source On Resistance ³	V _{GS} =10V, I _D =1A	---	4400	5000	m Ω
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz	---	336	---	pF
C _{oss}	Output Capacitance		---	27	--	
C _{rss}	Reverse Transfer Capacitance		---	19	---	
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DS} =325V, I _D =2A, R _{ENG} =10 Ω ,V _{GS} =10V	---	9	---	ns
t _r	Rise Time		---	1.1	---	ns
t _{d(off)}	Turn-Off Delay Time		---	16	---	ns
t _f	Fall Time		---	2	---	ns
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =325V, I _D =2A	---	9	---	nC
Q _{gs}	Gate-Source Charge		---	4.6	---	nC
Q _{gd}	Gate-Drain “Miller” Charge		---	0.3	---	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _{SD} =180A	---	---	1.5	V
I _S	Continuous Drain Curren	V _D =V _G =0V	---	---	2	A
I _{SM}	Pulsed Drain Current		---	---	8	A
T _{rr}	Reverse Recovery Time	I _F =3A, T _J =25℃	---	209	---	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/us	---	383	---	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition : $T_J=25^{\circ}\text{C}$, $V_{DD}=325\text{V}$, $V_G=10\text{V}$, $L=0.5\text{mH}$
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Characteristics: ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

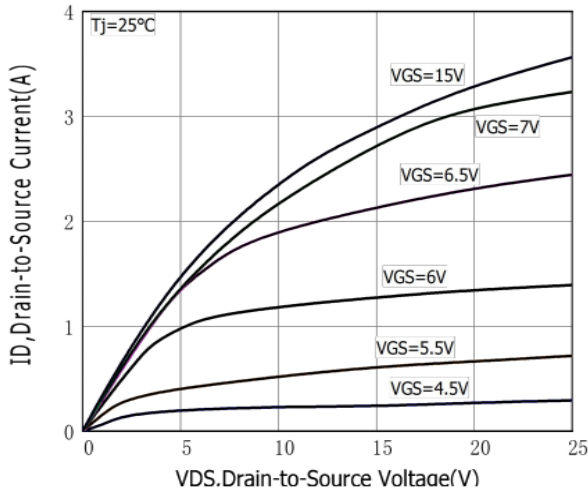


Figure.1 Typical Output Characteristics

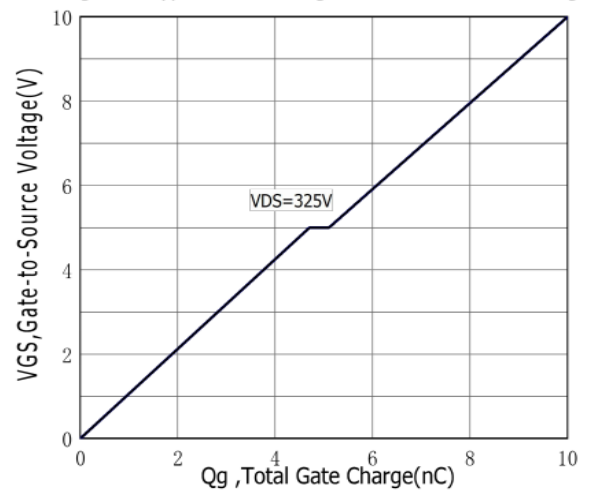


Figure.2 Typical Gate Charge vs Gate to Source Voltage

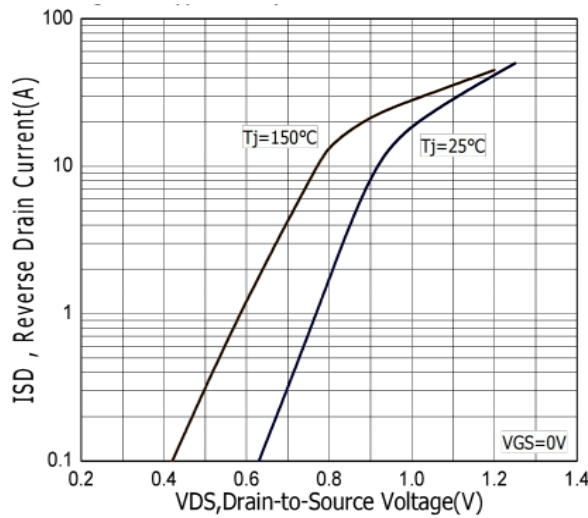


Figure.3 Typical Body Diode Transfer Characteristics

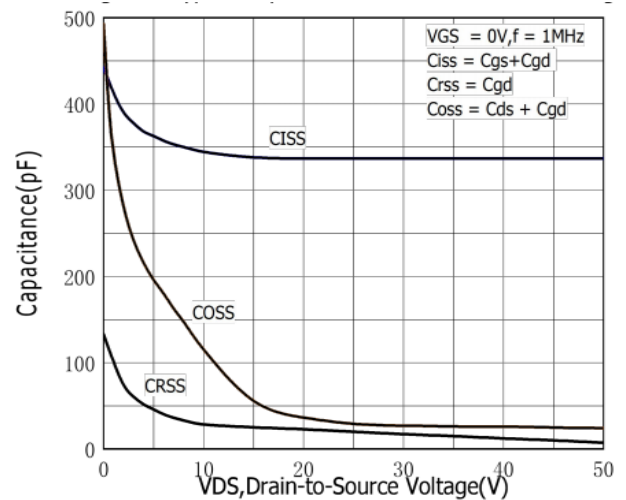


Figure.4 Typical Capacitance vs Drain to Source Voltage

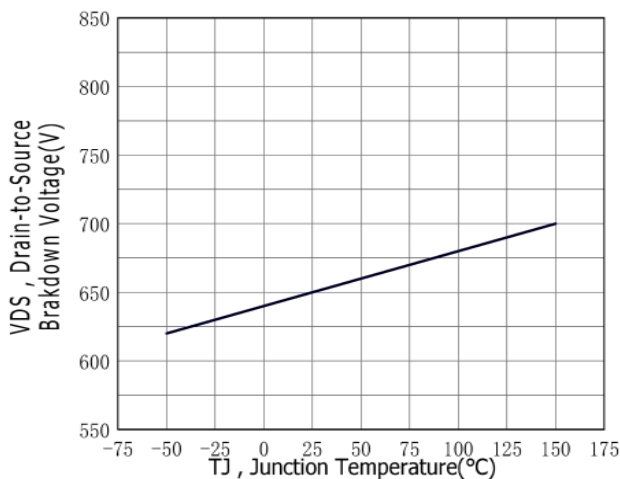


Figure.5 Typical Breakdown Voltage vs Junction Temperature

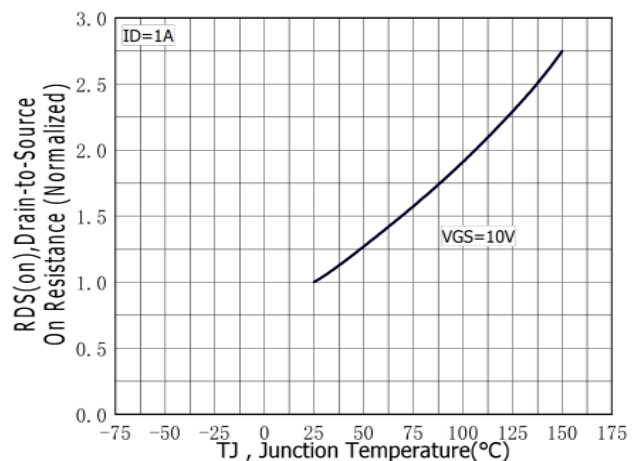


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

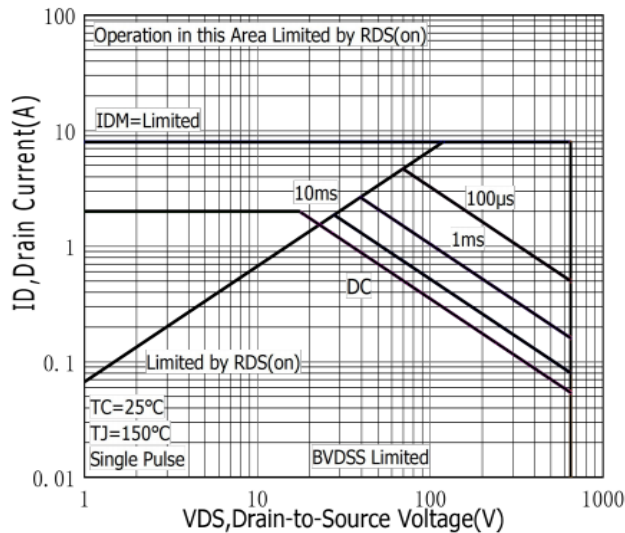


Figure.7 Maximum Forward Bias Safe Operating Area

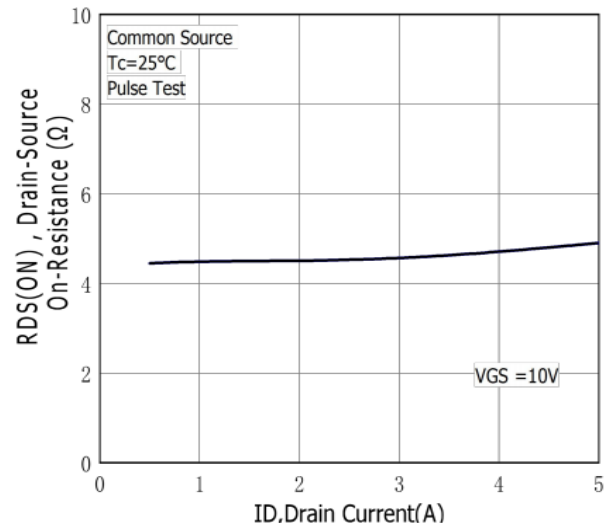


Figure.8 Typical Drain to Source ON Resistance vs Drain Current

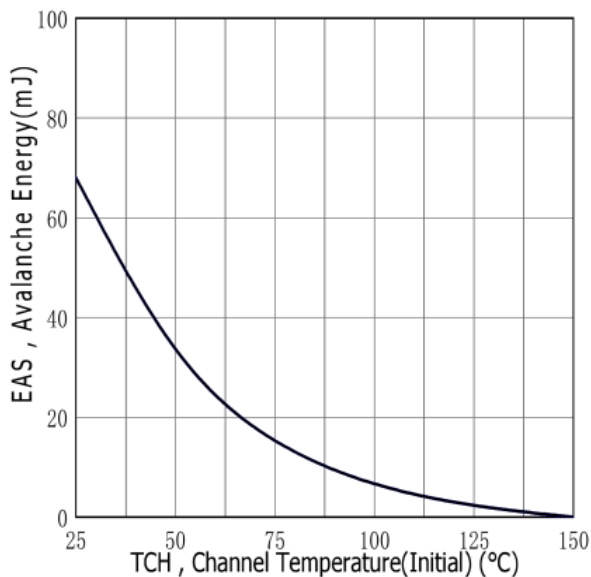


Figure.9 Maximum EAS vs Channel Temperature

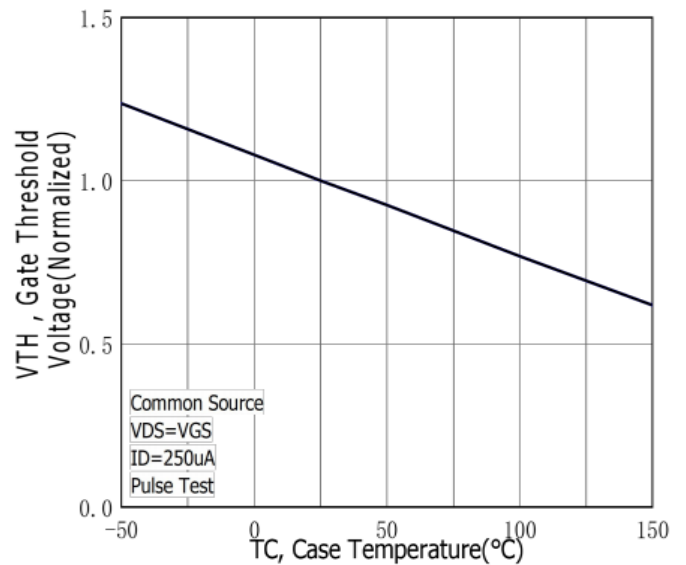


Figure.10 Typical Threshold Voltage vs Case Temperature

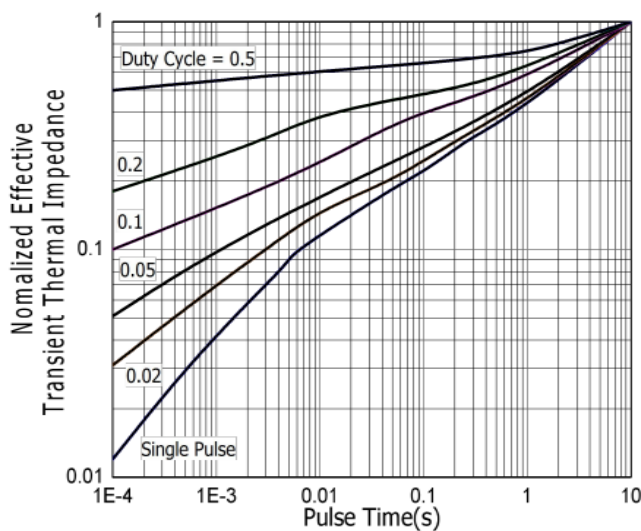


Figure.11 Maximum Effective Thermal Impedance, Junction to Case

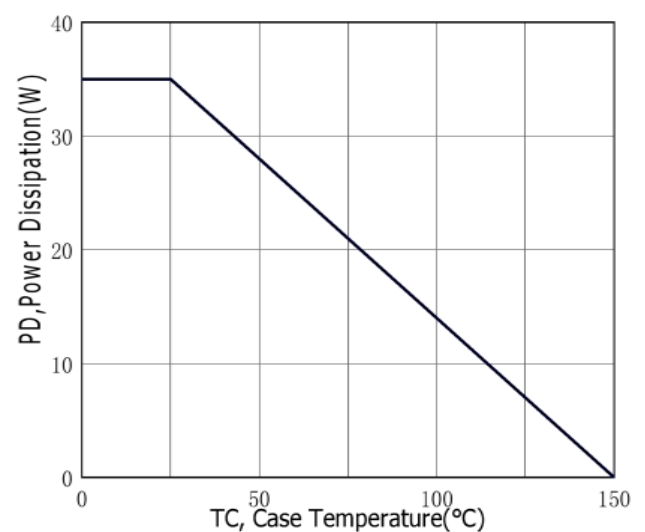
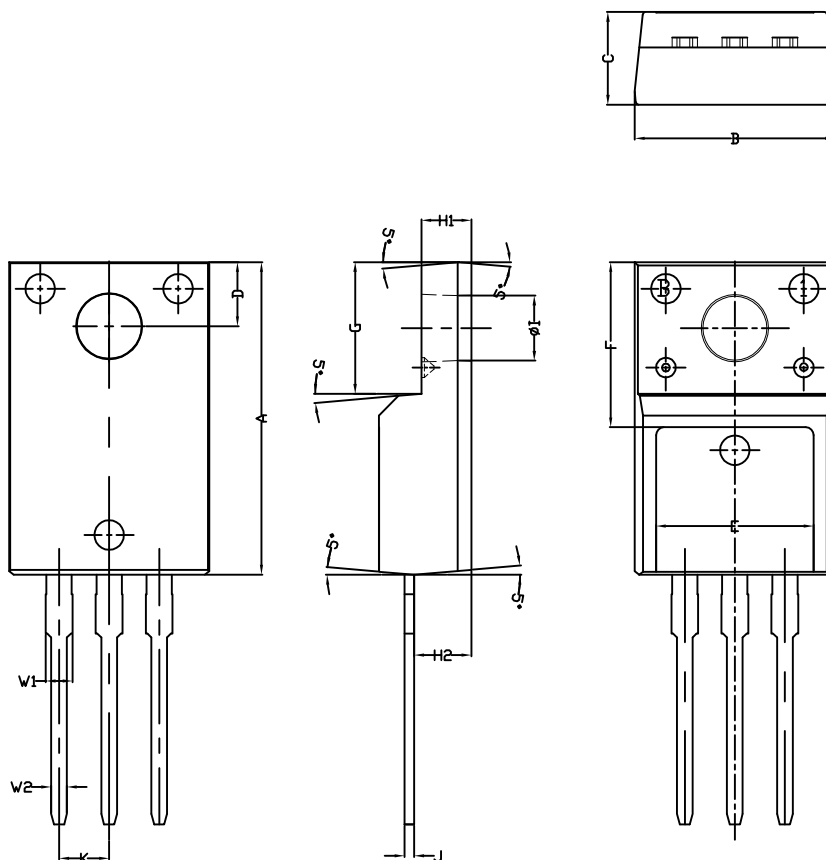


Figure.12 Maximum Power Dissipation vs Case Temperature

TO-220F Package Information:


Symbol	MM			Inch		
	Min	Mim	Max	Min	Mim	Max
A	15.67	15.87	16.07	0.6169	0.6248	0.6328
B	9.86	10.16	10.46	0.3882	0.4000	0.4118
C	4.50	4.70	4.90	0.1772	0.1850	0.1929
D	3.15	3.35	3.55	0.1240	0.1319	0.1398
E	7.80	8.00	8.20	0.3071	0.3150	0.3228
F	8.18	8.38	8.58	0.3220	0.3299	0.3378
H1	2.34	2.54	2.84	0.0921	0.1000	0.1118
H2	2.40	2.90	3.40	0.0945	0.1141	0.1339
I	3.10	3.30	3.50	0.1220	0.1299	0.1378
W1	1.08	1.28	1.48	0.0425	0.0504	0.0583
W2	0.70	0.80	0.90	0.0276	0.0315	0.0354
K	2.44	2.54	2.64	0.0961	0.1000	0.1039
G	6.48	6.68	6.88	0.2551	0.2630	0.2709
J	0.45	0.50	0.6	0.0177	0.0197	0.0236

Marking Information:

①. Doingter LOGO

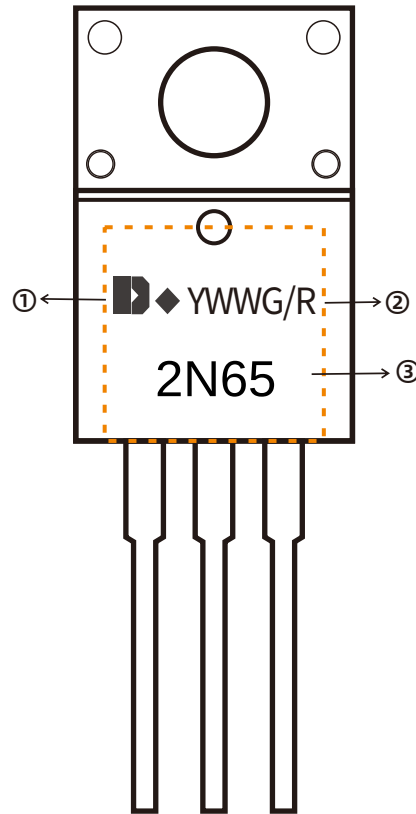
②. Date Code(YWWG / R)

Y : Year Code , last digit of the year

WW : Week Code(01-53)

G/R : G(Green) /R(Lead Free)

③. Part NO.



Previous Version

Version	Date	Subjects (major changes since last revision)
1.0	2024-10-10	Release of final version

Attention :

- Information furnished in this document is believed to be accurate and reliable. However, Shenzhen Doingter Semiconductor Co.,Ltd. assumes noresponsibility for the consequences of use without consideration for such information nor use beyond it.
- Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Shenzhen Doingter complies with the agreement. Products and information provided in this document have no infringement of patents.
- Shenzhen Doingter assumes noresponsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.



Is a registered trademark of Shenzhen Doingter Semiconductor Co., Ltd. Copyright © 2013 Shenzhen DoingterSemiconductor Co.,Ltd. Printed All rights reserved.