Features

- Super_Junction technology
- Much lower Ron*A performance for On-state efficiency
- Better efficiency due to very low FOM
- Qualified for industrial grade applications according to JEDEC

Bvdss	Rdson	ID
650V	430mΩ	8A

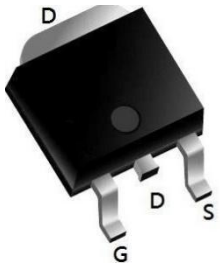
Application

RoHS

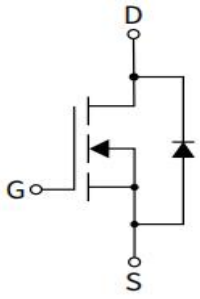
- PWM applications
- Load Switch
- Power management

Package

Marking and pin assignment



TO252-3L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
HL8N65R	HL8N65R	TO252-3L	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current, V_{GS}@10V[1,6]	T_C= 25℃	I_D	8	A
	T_C = 100℃		5	A
Pulsed Drain Current[2]		I_{DM}	32	A
Single Pulse Avalanche Energy[3]		E_{AS}	65	mJ
Avalanche Current		I_{AS}	-	A
Total Power Dissipation[4]@T_C = 25℃		P_D	73	W
Storage Temperature Range		T_{STG}	-55 ~ 150	℃
Operating Junction Temperature Range		T_J	-55 ~ 150	℃

Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance Junction-Ambient [1]	$R_{\theta JA}$	-	143	℃/W
Thermal Resistance Junction-Case[1]	$R_{\theta JC}$	-	1.7	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL8N65R	TO252-3L	1	2	3	Tape Reel

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	650	-	-	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V,T_J=25°C	-	-	1	uA
		V_{DS}=650V, V_{GS}=0V,T_J=100°C	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{GS}=V_{DS},I_D=250uA	3	-	4	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=10V, I_D=5.5A	-	430	550	mΩ
Forward Transconductance	gfs	V_{DS}=20V,I_D=4A	-	6.6	-	S
Gate Resistance	R_g	V_{DS}=0V,V_{GS}=0V,f=1MHz	-	14	-	Ω
Input Capacitance	C_{iss}	V_{DS}=100V,V_{GS}=0V,f=1MHZ	-	470	-	pF
Output Capacitance	C_{oss}		-	25	-	
Reverse Transfer Capacitance	C_{rss}		-	0.47	-	
Total Gate Charge	Q_g	V_{DS}=480V,V_{GS}=10V, I_D=5.5A	-	15.6	-	nC
Gate-Source Charge	Q_{gs}		-	3.1	-	
Gate-Drain Charge	Q_{gd}		-	6.5	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=400V, R_G=27Ω,I_D=4A	-	15	-	ns
Rise Time	t_r		-	17	-	
Turn-Off Delay Time	$t_{d(off)}$		-	78	-	
Fall Time	t_f		-	16	-	
Continuous Source Current[1,4]	I_S	V_G=V_D=0V,Force Current	-	-	8	A

Diode Forward Voltage[2]	V_{SD}	V_{GS}=0V,I_S=5.5A,T_J=25℃	-	-	1.2	V
Reverse Recovery Time	t_{rr}	IF=5.5A,di/dt=100A/μs, T_J=25℃	-	210	-	nS
Reverse Recovery Charge	Q_{rr}		-	1.76	-	nC

Note:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.

3.The EAS data shows Max. rating . The test condition is T_J=25℃,V_{DD}=200V,V_{GS}=10V,L=60mH.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM} , in real applications,should be limited by total power dissipation.

Typical Performance Characteristics

Fig 1. Output Characteristics (Tj=25℃)

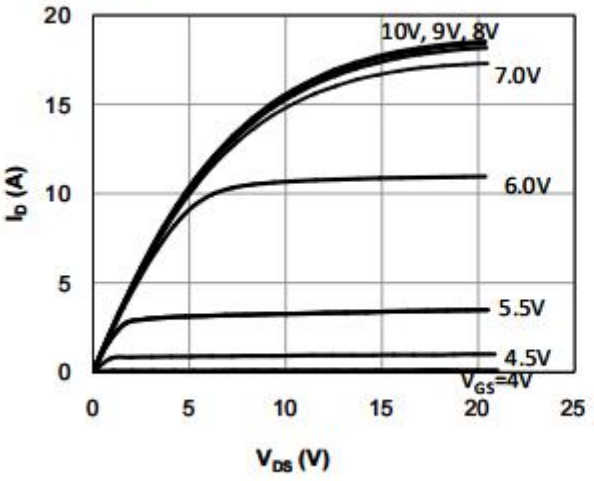


Fig 2. Output Characteristics (Tj=150℃)

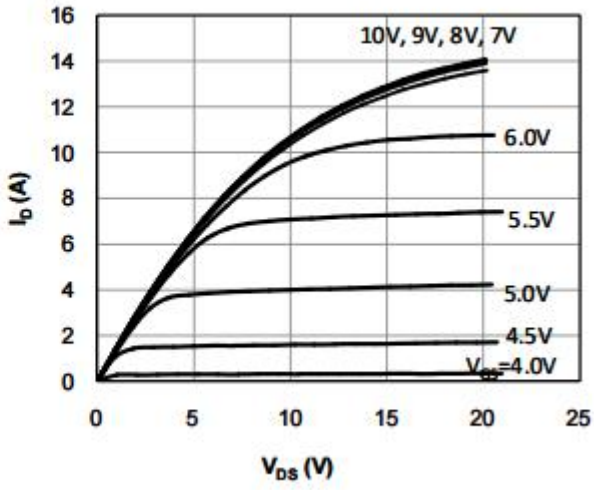


Fig 3: Transfer Characteristics

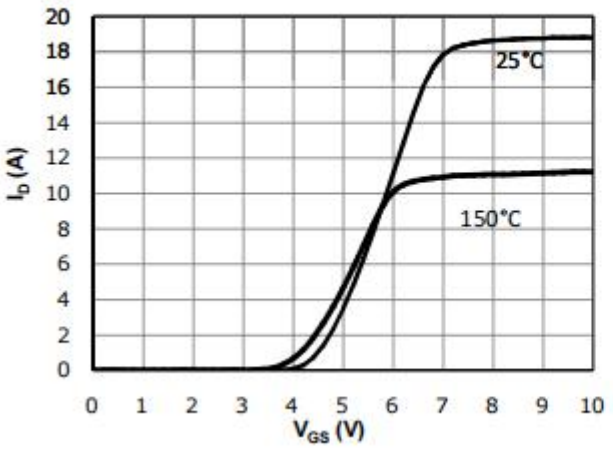


Fig 4: V_{TH} Vs Tj Temperature Characteristics

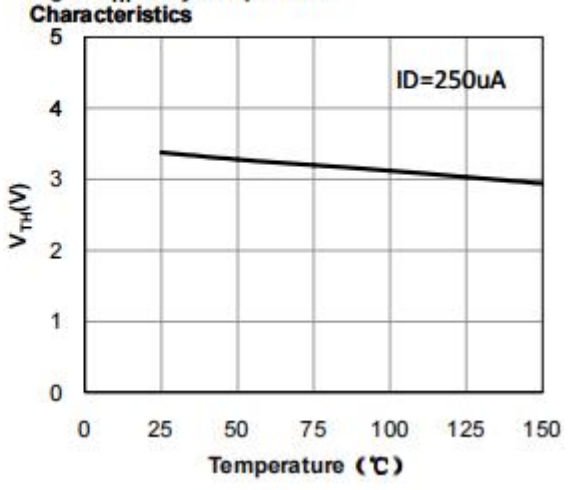


Fig 5: Rdson Vs Ids Characteristics(Tc=25℃)

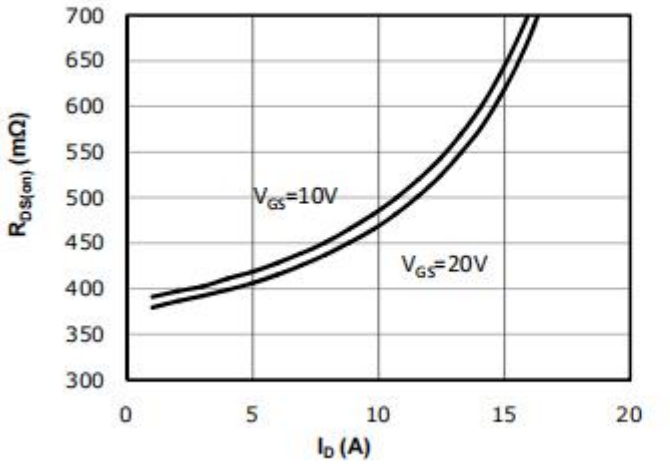


Fig 6: Rds(on) vs. Temperature

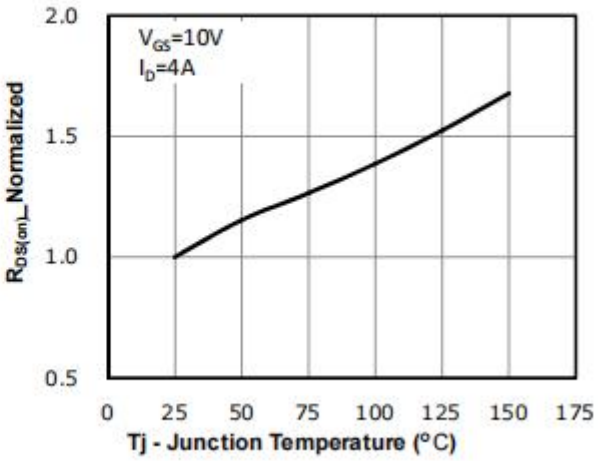


Fig 7: BVDSS vs. Temperature

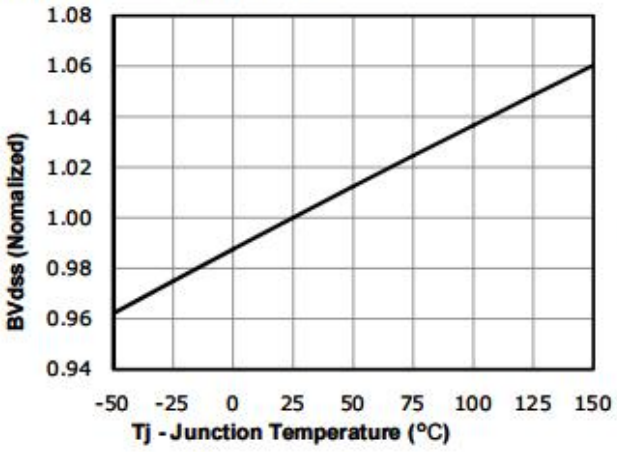


Fig 8: Rds(on) vs Gate Voltage

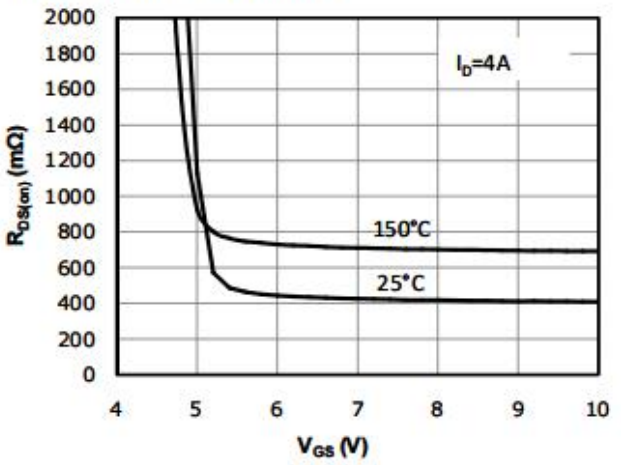


Fig 9: Body-diode Forward Characteristics

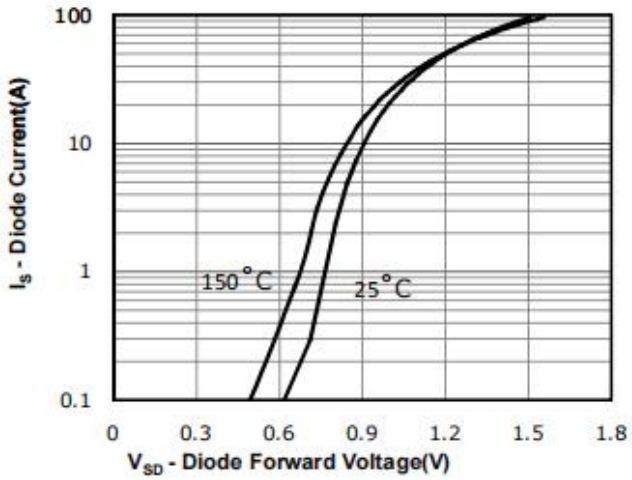


Fig 10: Gate Charge Characteristics

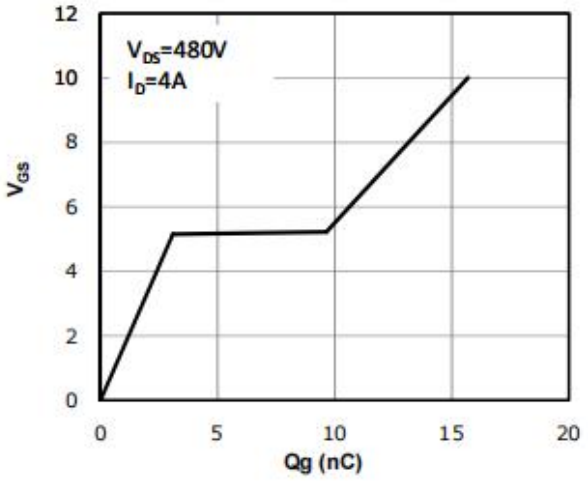


Fig 11: Capacitance Characteristics

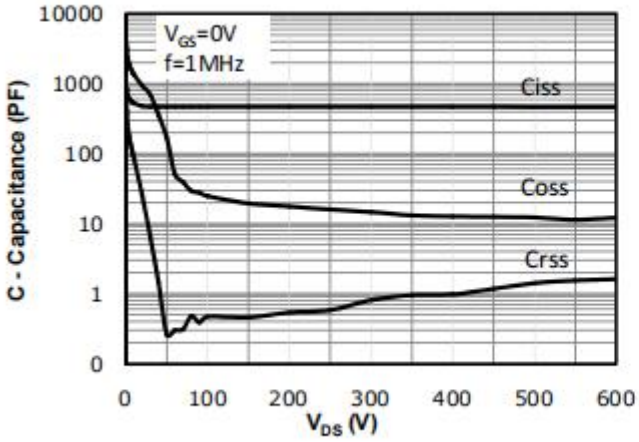


Fig 12: Safe Operating Area

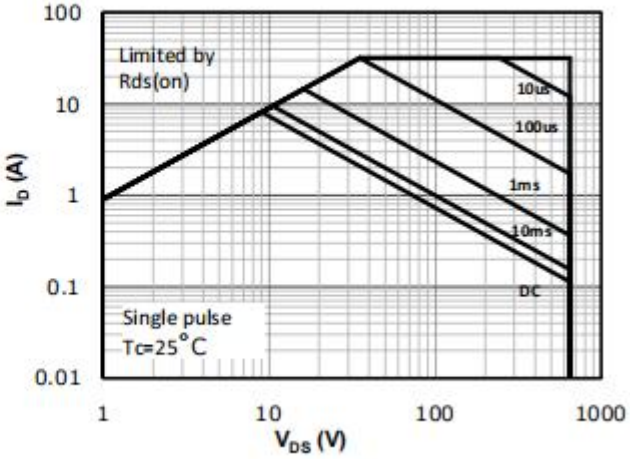
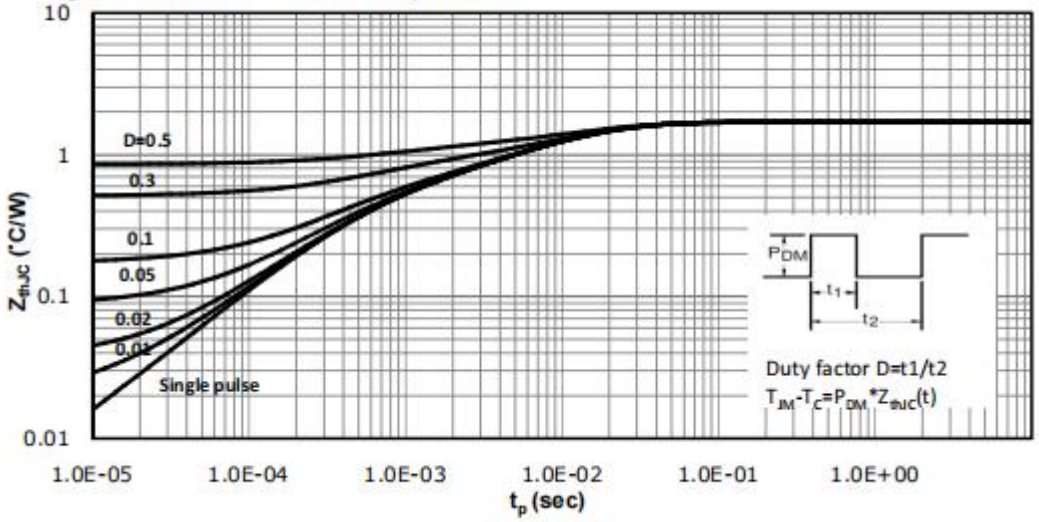
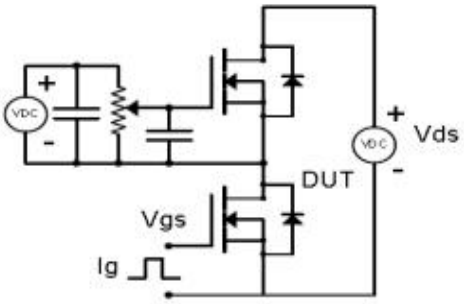


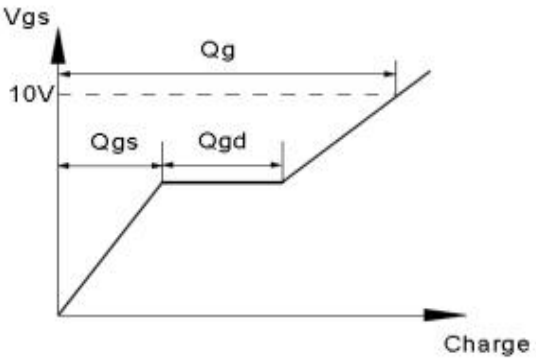
Fig 13: Max. Transient Thermal Impedance



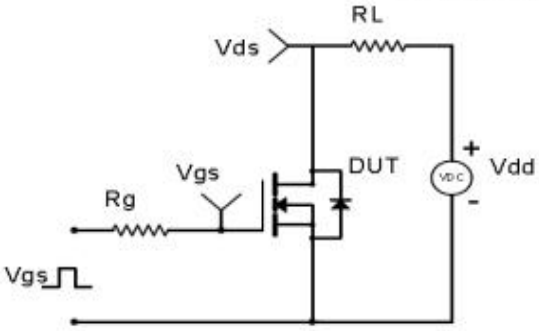
Test Circuit & Waveform

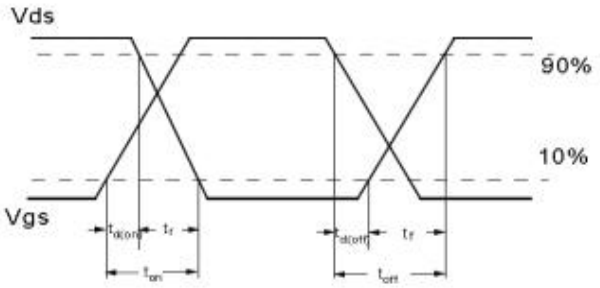
Gate Charge Test Circuit & Waveform



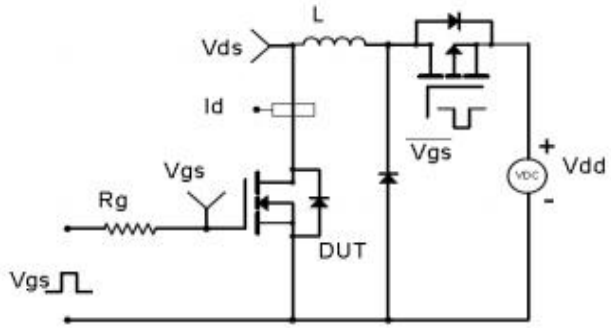


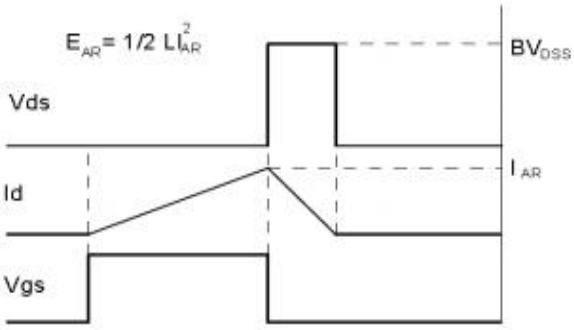
Resistive Switching Test Circuit & Waveforms



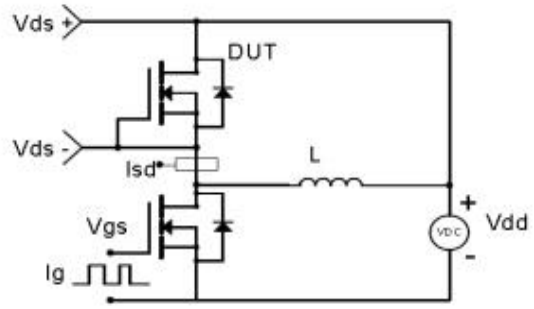


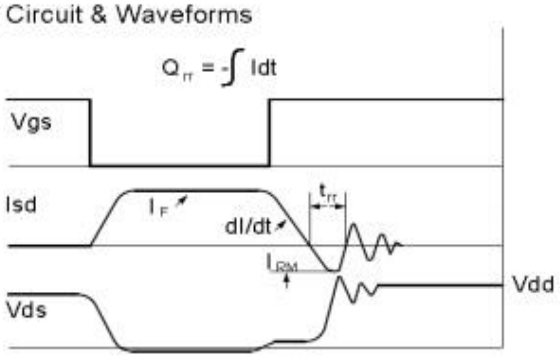
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



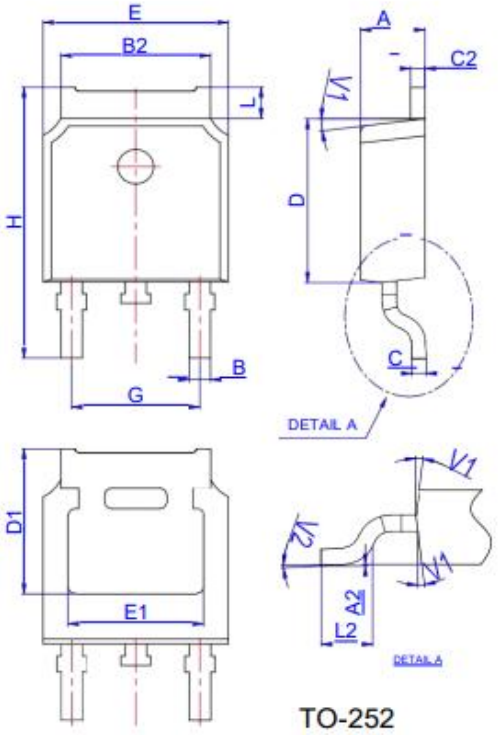


Diode Recovery Test Circuit & Waveforms





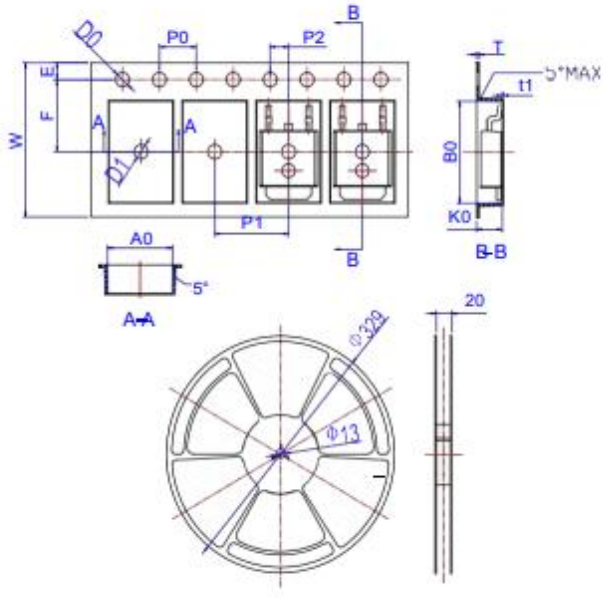
Package Dimensions TO252-3L



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

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