MPM4710

6V, 1A, 2MHz, Synchronous Buck-Boost Power Module

DESCRIPTION

The MPM4710 is a fully integrated, high-efficiency, synchronous buck-boost power module with a built-in inductor. The device can operate from an input voltage (V_{IN}) above, equal to, or below the output voltage (V_{OUT}).

The fixed 2MHz switching frequency (f_{SW}) allows for the use of small external components, while internal compensation and soft start (SS) reduce the external component count. The MPM4710 employs current mode control with a fixed pulse-width modulation (PWM) frequency to improve stability and transient response.

For low-noise applications, a high-logic input on the MODE/SYNC pin allows the device to operate in fixed-frequency PWM mode under all load conditions.

The MPM4710 operates from a 1.2V to 5.5V V_{IN} range, and provides an adjustable V_{OUT} that can be set between 1.5V and 5.5V.

The MPM4710 is available in a small ECLGA-14 (2.5mmx2.5mmx1.2mm) package.

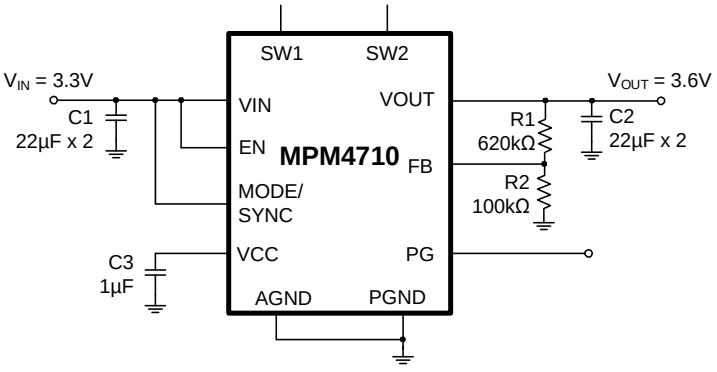
FEATURES

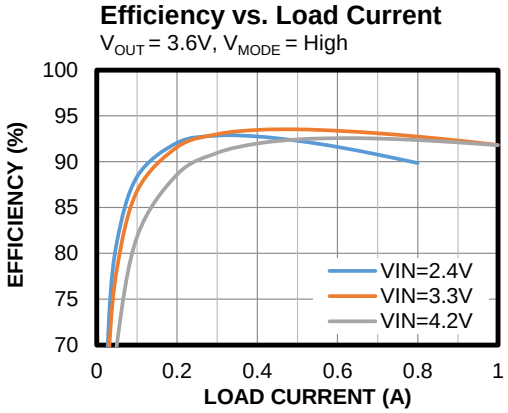
- 1.8V Minimum Start-Up Input Voltage (V_{IN})
- 1.2V to 5.5V Operating V_{IN} Range
- 1.5V to 5.5V Output Voltage (V_{OUT}) Range
- Typical 1A, Max 2A Output Current (I_{OUT})
- Fixed 2MHz or External Synchronous Switching Frequency (f_{SW})
- Selectable Pulse-Skip Mode (PSM) or Pulse-Width Modulation (PWM) Mode
- Typical 25µA Quiescent Current (I_Q)
- Load Disconnect during Shutdown
- Internal Soft Start (SS) and Compensation
- Power Good (PG) Indication
- Short-Circuit Protection (SCP) with Hiccup Mode
- Thermal Shutdown
- Available in an ECLGA-14 (2.5mmx2.5mmx1.2mm) Package

APPLICATIONS

- Optical Modules
- Personal Medical Devices
- Time-of-Flight (ToF) Sensors or Structured Light Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM4710GPA	ECLGA-14 (2.5mmx2.5mm)	*See Below*	3

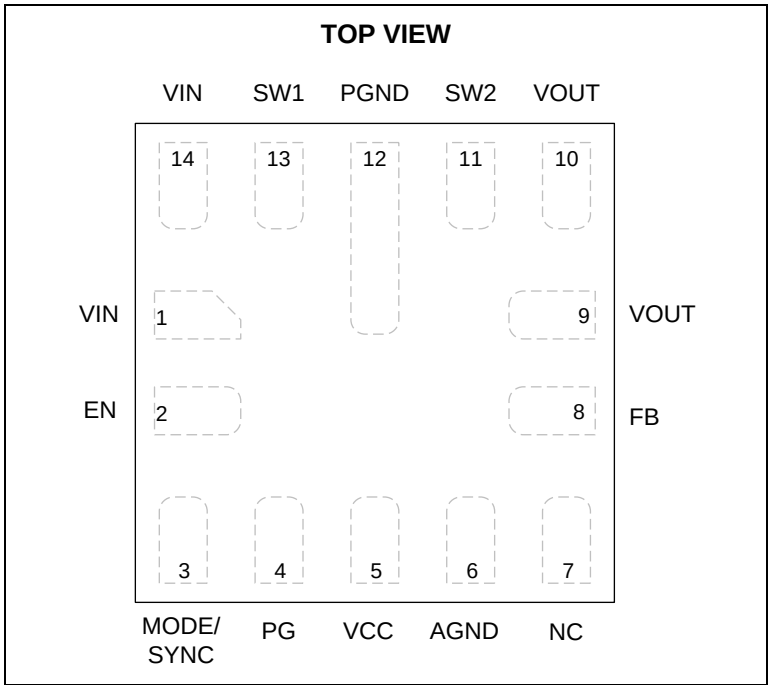
* For Tape & Reel, add suffix -Z (e.g. MPM4710GPA-Z).

TOP MARKING

BUE
YWW
LLL

BUE: Product code of MPM4710GPA
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



ECLGA-14 (2.5mmx2.5mmx1.2mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 14	VIN	**Power stage supply voltage.**
2	EN	**Enable control.** Pull the EN pin high to turn the device on; pull EN low or float EN to turn it off. EN is pulled down to AGND by an internal 1.5MΩ resistor.
3	MODE/ SYNC	**Mode selection.** If the MODE/SYNC pin is low, the device automatically switches between pulse-skip mode (PSM) and fixed-frequency pulse-width modulation (PWM) mode according to the load level. If MODE/SYNC is high, the MPM4710 operates in fixed-frequency PWM mode continuously. An external clock can be applied to MODE/SYNC to synchronize the switching frequency (f_{SW}). MODE/SYNC is pulled down to AGND by an internal 1MΩ resistor. MODE/SYNC should be pulled high or low by a <10kΩ resistor.
4	PG	**Power good indication.** If the feedback (FB) voltage (V_{FB}) exceeds 91.5% of the reference voltage (V_{REF}), the PG pin is pulled high. If V_{FB} drops below 76% of V_{REF}, PG is pulled low.
5	VCC	**Supply voltage for the control stage.** The VCC pin is powered from the higher voltage between the input voltage (V_{IN}) and the output voltage (V_{OUT}). Decouple VCC using a 1µF capacitor.
6	ANGD	**Signal ground.** The AGND pin is not internally connected to power ground (PGND), so ensure that AGND is connected to the PGND pin in the PCB layout.
7	NC	**Not connected.**
8	FB	**Output voltage feedback.** Keep the FB pin and its traces away from noisy nodes, such as SW.
9, 10	VOUT	**Buck-boost converter output.** Place an output capacitor (C_{OUT}) close to the VOUT and PGND pins.
11	SW2	**Test pin.** SW2 is a test pin that can be left floating. The internal MOSFETs are connected to SW2.
12	PGND	**Power ground.** The PGND pin is not internally connected to signal ground (AGND), so ensure that PGND is connected to AGND in the PCB layout.
13	SW1	**Test pin.** SW1 is a test pin that can be left floating. The internal MOSFETs are connected to SW1.

ABSOLUTE MAXIMUM RATINGS (1)

VIN to PGND .....-0.3V to +6V
SWx to PGND .....-0.3V (-2V for <10ns) to 6.5V (8.5V for <10ns)
PG to PGND.....-0.3V to 5.3V
All other pins .....-0.3V to 6V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2) (5) 4.3W
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±2000V

Recommended Operating Conditions (3)

Start-up input voltage (V_{SU}).....1.8V to 5.5V
Operating input voltage (V_{IN})..... 1.2V (4) to 5.5V
Output voltage (V_{OUT}).....1.5V to 5.5V
Operating T_J..... -40°C to +125°C

Thermal Resistance (2) (5) (6) (7)

θ_{JA}..... 29°C/W
θ_{JC_TOP}.....5.3°C/W
θ_{JB}.....13°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) If V_{CC} is powered from a source >1.8V (such as V_{OUT}), the MPM4710 can operate at V_{IN} down to 1.2V. However, the load capability is lower when V_{IN} = 1.2V due to SWA's high on resistance and the low current limit (I_{LIMIT}).
5) The thermal parameter is tested on the MPS evaluation board EVM4710-PA-00B under no airflow cooling conditions in a standard enclosure. The board size is 5cmx5cmx1.6mm, 4-layer, of which the top and bottom layer copper thickness is 2oz, and the inner layer is 1oz.
6) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates T_J in the real system, based on the equation $T_J = \theta_{JC\_TOP} \times P_{LOSS} + T_{CASE\_TOP}$, where P_{LOSS} is the entire loss of the module in real applications, and T_{CASE_TOP} is the case top temperature.
7) The junction-to-board thermal characterization parameter, θ_{JB}, estimates T_J in the real system, based on the equation $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the entire loss of the module in real applications, and T_{BOARD} is the board temperature.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = V_{OUT} = 3.3V, T_J = -40°C to 125°C [8], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$	VCC is floating, V_{IN} rising, V_{IN} is tested once the IC starts up	1.63	1.7	1.77	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	V_{OUT} = 3.3V, V_{IN} falling		0.69		V
V_{CC} UVLO falling threshold	$V_{CC\_UVLO\_FALLING}$	V_{IN} = 1.2V, V_{CC} falling	1.45	1.56	1.67	V
Reference voltage	V_{REF}	T_J = 25°C	495	500	505	mV
		T_J = -40°C to +125°C	492.5	500	507.5	mV
Switching frequency	f_{SW}		1700	2000	2300	kHz
Synchronized frequency range			1000		3000	kHz
Steady state current limit (I_{LIMIT})	I_{LIMIT_SW1}	V_{FB} > 60%V_{REF}	3.5	4.2	5	A
Start-up I_{LIMIT}	I_{LIMIT_SW2}	V_{FB} < 60%V_{REF}	1.7	2.5		A
N-channel MOSFET on resistance	$R_{DS(ON)\_N}$	SWB, SWC		22		mΩ
P-channel MOSFET on resistance	$R_{DS(ON)\_P}$	SWA, SWD		27.5		mΩ
Quiescent current	I_Q	V_{FB} = 0.55V, V_{IN} = 2.5V, V_{OUT} = 3.3V, I_Q is measured from VOUT		25		μA
		V_{FB} = 0.55V, V_{IN} = 2.5V, V_{OUT} = 3.3V, I_Q is measured from VIN		3.3		μA
Shutdown current	I_{SD}	V_{EN} = 0V			3	μA
Soft-start time	t_{SS}	Internal V_{REF} from 0V to 0.5V		1.5		ms
EN and MODE/SYNC low voltage					0.4	V
EN and MODE/SYNC high voltage			1.2			V
EN current	I_{EN}	V_{EN} = 3.3V		2.1		μA
		V_{EN} = 0V		0		μA
Power good (PG) rising threshold	V_{PG_RISING}		87.5	91.5	95.5	% of V_{REF}
PG falling threshold	$V_{PG\_FALLING}$		72	76	80	% of V_{REF}
PG delay	t_{PG}	Low to high		118		μs
		High to low		19		μs
PG sink current capability	V_{PG}	Sink 3mA			0.3	V
Thermal shutdown [9]	T_{SD}			160		°C
Thermal shutdown hysteresis [9]	T_{SD_HYS}			20		°C

Notes:

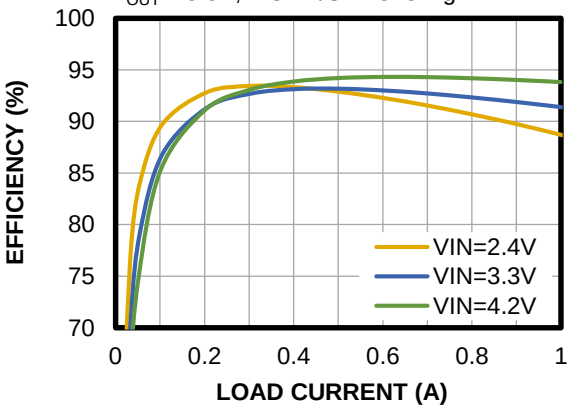
8) Guaranteed by over-temperature (OT) correlation. Not tested in production.
9) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.3V, C_{OUT} = 2 x 22µF + 0.1µF, T_A = 25°C, unless otherwise noted.

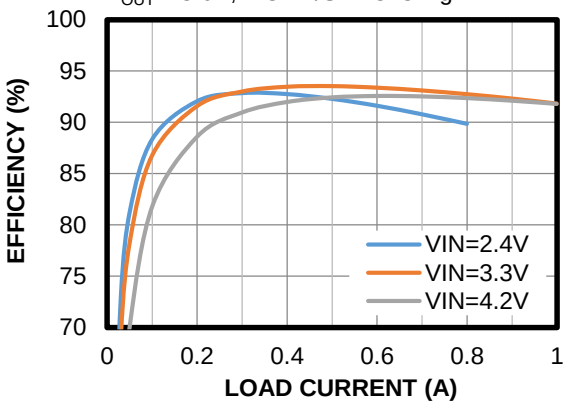
Efficiency vs. Load Current

V_{OUT} = 3.3V, MODE/SYNC is high



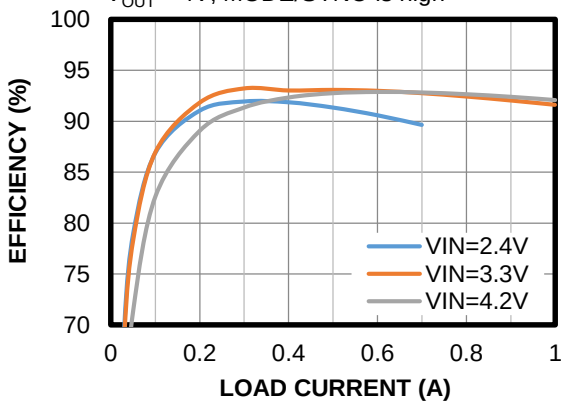
Efficiency vs. Load Current

V_{OUT} = 3.6V, MODE/SYNC is high



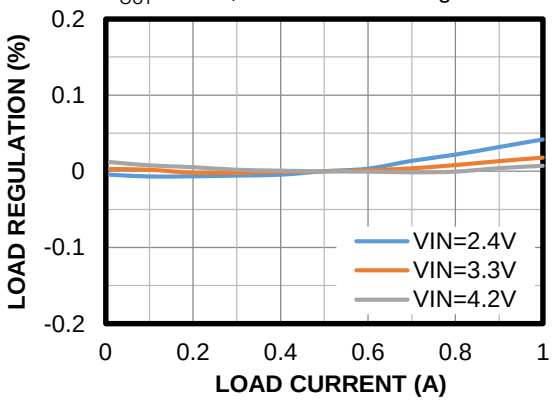
Efficiency vs. Load Current

V_{OUT} = 4V, MODE/SYNC is high



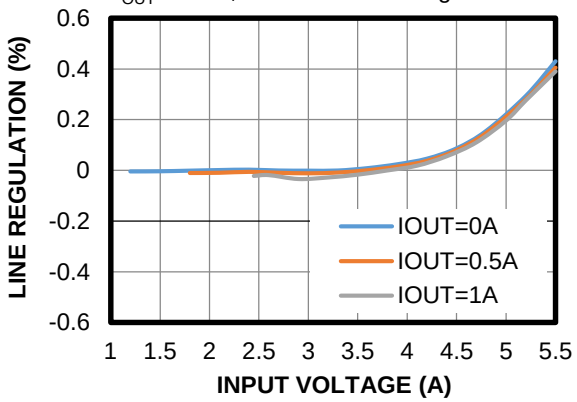
Load Regulation

V_{OUT} = 3.3V, MODE/SYNC is high



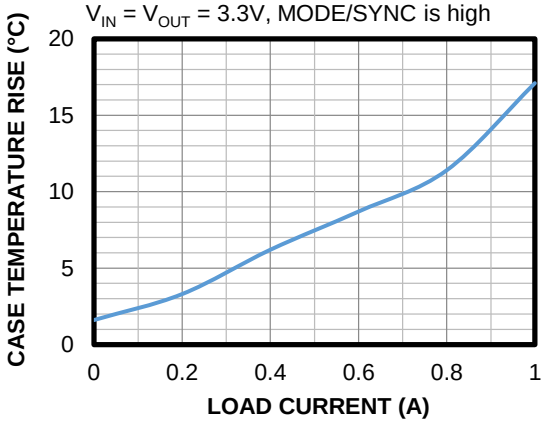
Line Regulation

V_{OUT} = 3.3V, MODE/SYNC is high



Case Temperature Rise

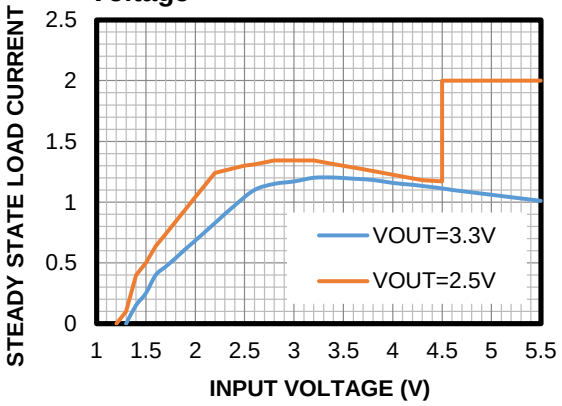
V_{IN} = V_{OUT} = 3.3V, MODE/SYNC is high



TYPICAL CHARACTERISTICS *(continued)*

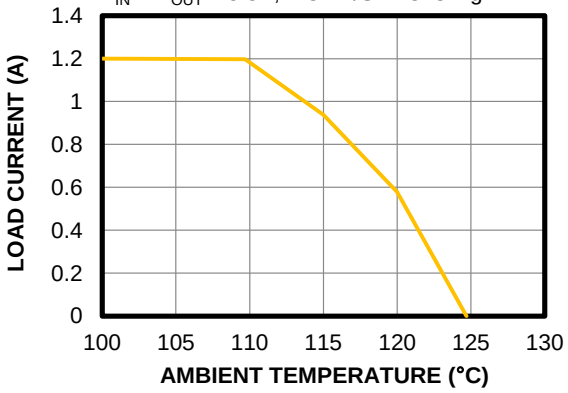
V_{IN} = 3.3V, V_{OUT} = 3.3V, C_{OUT} = 2 x 22µF + 0.1µF, T_A = 25°C, unless otherwise noted.

Steady State Load Current vs. Input Voltage



Load Current vs. Ambient Temperature

V_{IN} = V_{OUT} = 3.3V, MODE/SYNC is high

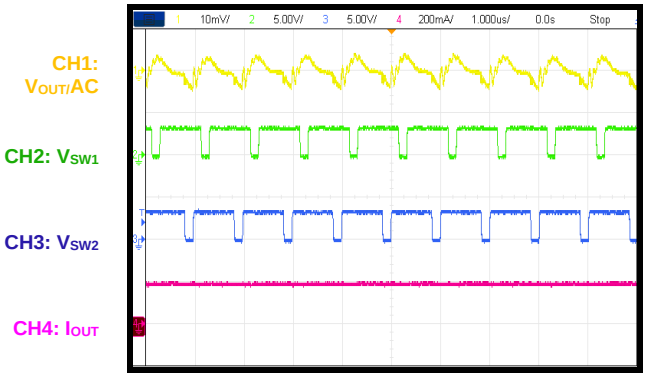


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 3.3V, C_{OUT} = 2 x 22µF + 0.1µF, T_A = 25°C, unless otherwise noted.

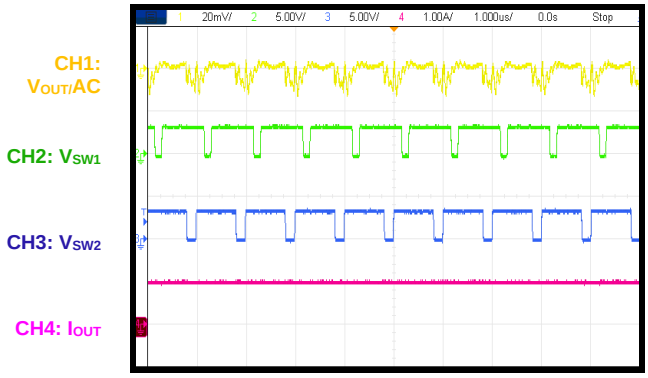
Steady State

I_{OUT} = 0.2A, MODE/SYNC is high



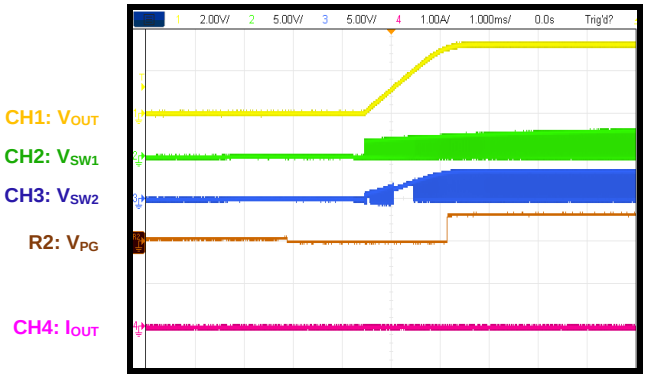
Steady State

I_{OUT} = 1A, MODE/SYNC is high



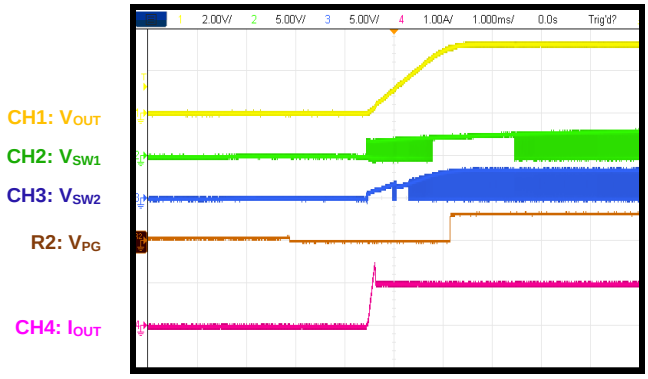
Start-Up

I_{OUT} = 0A, MODE/SYNC is high



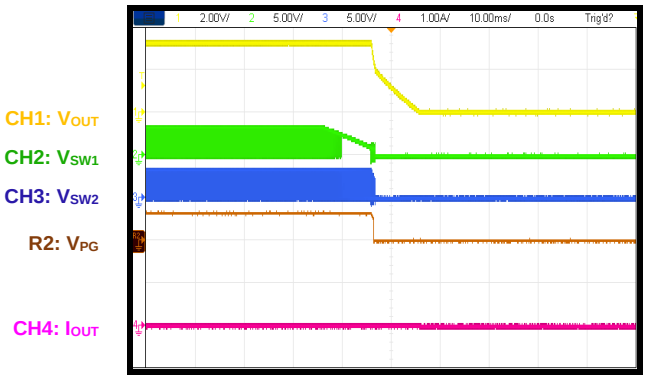
Start-Up

I_{OUT} = 1A, MODE/SYNC is high



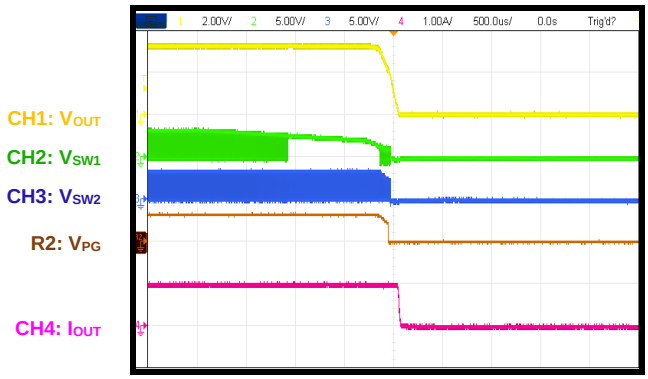
Shutdown

I_{OUT} = 0A, MODE/SYNC is high



Shutdown

I_{OUT} = 1A, MODE/SYNC is high

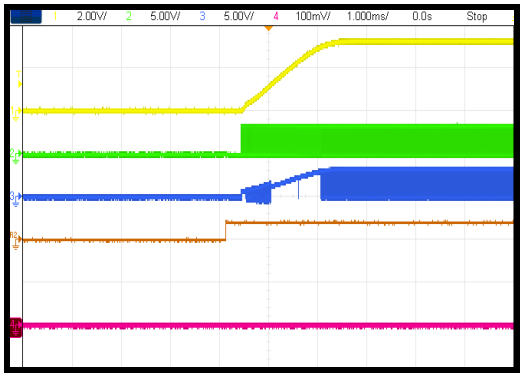


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 3.3V, C_{OUT} = 2 x 22µF + 0.1µF, T_A = 25°C, unless otherwise noted.

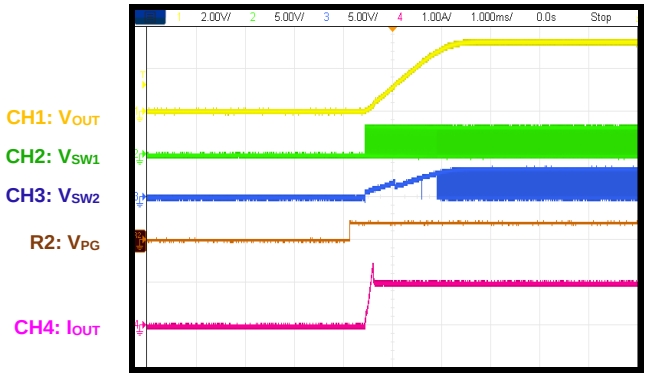
Start-Up through EN

I_{OUT} = 0A, MODE/SYNC is high



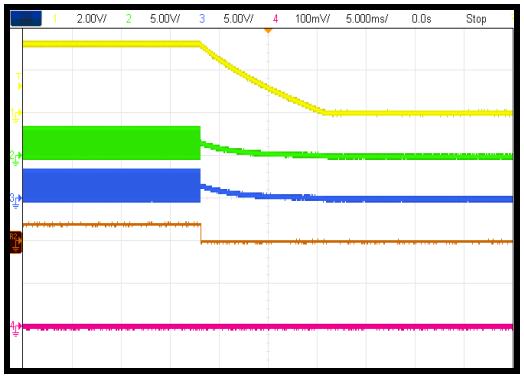
Start-Up through EN

I_{OUT} = 1A, MODE/SYNC is high



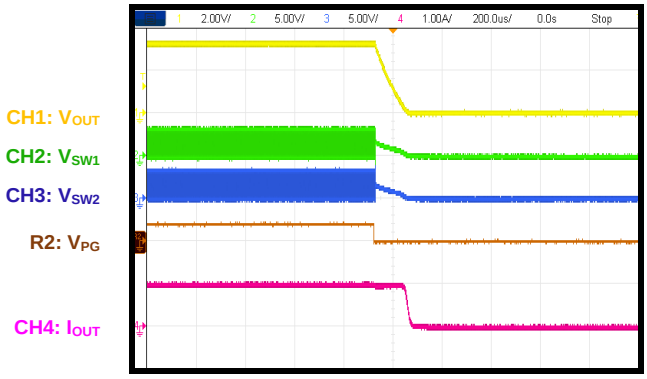
Shutdown through EN

I_{OUT} = 0.01A, MODE/SYNC is high



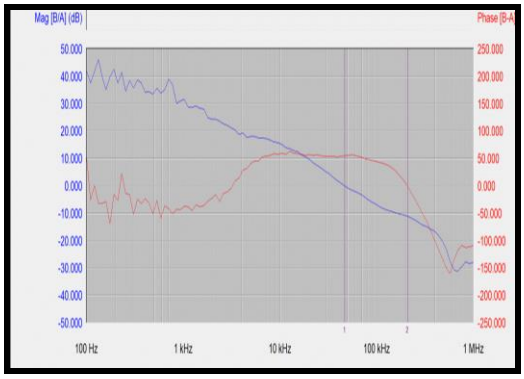
Shutdown through EN

I_{OUT} = 1A, MODE/SYNC is high



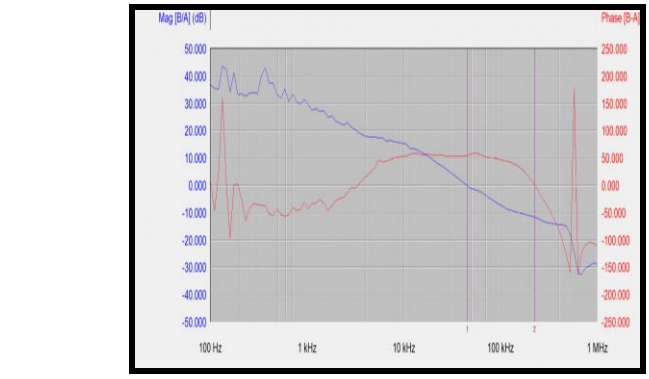
Bode Plot

V_{IN} = 3.3V, V_{OUT} = 3.6V, I_{OUT} = 0.05A, MODE/SYNC is high



Bode Plot

V_{IN} = 3.3V, V_{OUT} = 3.6V, I_{OUT} = 1A, MODE/SYNC is high



FUNCTIONAL BLOCK DIAGRAM

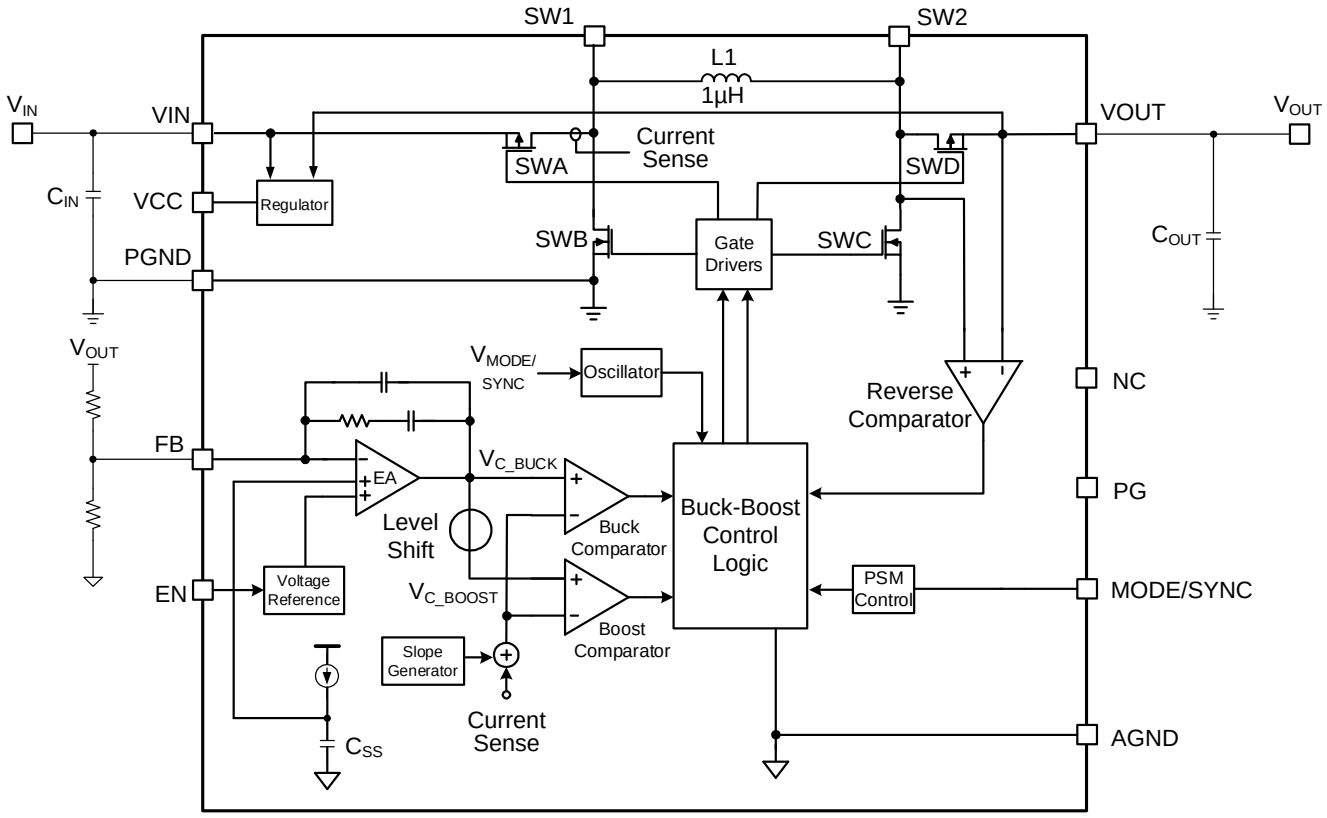


Figure 1: Functional Block Diagram

OPERATION

The MPM4710 is a high-efficiency, dual-mode, buck-boost converter that can regulate the output voltage (V_{OUT}) above, equal to, or below the input voltage (V_{IN}). V_{OUT} is sensed by the feedback (FB) pin via an external resistor divider connected between VOUT and PGND (see Figure 1 on page 10). The difference between the FB voltage (V_{FB}) and the internal reference voltage (V_{REF}) is amplified by the error amplifier (EA) to generate a buck control signal (V_{C_BUCK}). The buck comparator compares V_{C_BUCK} to the internal current ramp signal (the sensed SWA's current with slope compensation) to generate a pulse-width modulation (PWM) signal for SWA and SWB.

A boost control signal (V_{C_BOOST}) is generated from V_{C_BUCK} via the level shift. The boost comparator compares V_{C_BOOST} to the same ramp signal to generate a PWM signal for SWC and SWD. Figure 2 shows the MOSFET topology for the buck-boost converter.

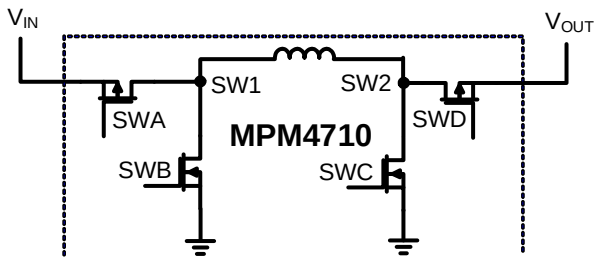


Figure 2: **Buck-Boost MOSFET Topology**

Buck Mode ($V_{IN} > V_{OUT}$)

When V_{IN} significantly exceeds V_{OUT}, the converter operates in buck mode to deliver energy to the load within SWA's maximum duty cycle by switching SWA and SWB. Meanwhile, SWC is off and SWD remains on. V_{C_BUCK} is compared to the current ramp signal to generate a PWM signal. SWA and SWB are pulse-width modulated to provide the required duty cycle and regulate V_{OUT}.

Boost Mode ($V_{IN} < V_{OUT}$)

When V_{IN} is significantly below V_{OUT}, the converter operates in boost mode. In boost mode, V_{C_BUCK} always exceeds the current ramp signal. The offset voltage is added to the current signal, and SWB does not turn on in any cycles. The logic determines whether boost mode is enabled in every cycle. In boost mode, only SWC and SWD switch. Under these conditions, SWC and SWD are pulse-width modulated to provide the required duty cycle and regulate V_{OUT}.

Buck-Boost Mode ($V_{IN} \approx V_{OUT}$)

When V_{IN} is almost equal to V_{OUT}, the converter cannot provide enough energy to the load due to SWA's maximum duty cycle. The current ramp signal cannot reach V_{C_BUCK} within the first PWM period, and SWA remains on with a 100% duty cycle. If SWB remains off in the first period, then the converter operates in boost mode starting in the second PWM period. SWC switches in the second period, and an offset voltage is added to the current ramp signal to allow it to reach V_{C_BUCK}. SWC turns off once the current ramp signal reaches V_{C_BOOST} in the second period, and SWD turns on to conduct the inductor current (I_L). SWA turns off once the current ramp signal reaches V_{C_BUCK} in the second period, and SWB turns on to conduct I_L.

If SWB turns on in the second period, boost mode is disabled in the following cycle. If SWA continues to conduct with a 100% duty in the second period, boost mode is enabled in the following duty cycle. In buck-boost mode, SWA and SWB, and SWC and SWD switch simultaneously.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the device from operating at an insufficient supply voltage. The UVLO circuit monitors the VCC voltage (V_{CC}). During start-up, V_{IN} must exceed its UVLO rising threshold to support a sufficient V_{CC} and enable the IC. Once the IC is enabled, VCC is powered by the higher voltage between V_{IN} and V_{OUT}. This allows the IC to operate, even if V_{IN} drops to 1.2V (unless V_{CC} drops below its UVLO falling threshold).

During start-up, if V_{CC} is biased to a certain voltage from another power supply, the MPM4710 can operate from a 1.2V V_{IN}. If V_{IN} is below 1.2V, then SWA's on resistance is high, and the MPM4710 cannot supply sufficient power to the output. If V_{IN} drops to 0.69V, the MPM4710 stops operating.

VCC Power Supply

When V_{IN} is sufficient and EN is high, V_{IN} charges V_{CC}. If V_{IN} exceeds the UVLO rising threshold, the MPM4710 starts up. The MPM4710's internal circuitry is powered by VCC. Decouple VCC using a <1µF ceramic capacitor. After start-up, VCC is powered by the higher voltage between V_{IN} and V_{OUT}. If VCC is powered by V_{OUT}, the MPM4710 shuts down when V_{IN} drops below its UVLO falling threshold (0.69V) or V_{CC} drops to its UVLO falling threshold (1.56V). It is not suggested to supply the MPM4710 with an input below 1.2V, even if VCC has a bias voltage due to a high SWA on resistance when V_{IN} is low. Even with a 1.2V V_{IN}, the load capability is reduced compared to a high input condition due to a high on resistance.

Internal Soft Start (SS)

The MPM4710 has a soft start (SS) mechanism to ensure that the output smoothly ramps up during start-up. When EN goes high and V_{IN} exceeds the UVLO rising threshold, an internal soft-start (SS) voltage (V_{SS}) ramps up to control V_{REF}. After a 4ms blanking time, if V_{OUT} has not reached 60% of the normal V_{OUT}, or if V_{OUT} is pulled down to 60% of the normal V_{OUT} due to an overload, V_{SS} is pulled down to PGND and the device enters hiccup mode. During start-up or hiccup mode, V_{SS} is clamped at V_{FB} + 0.3V if V_{OUT} does not rise. This prevents a V_{OUT} overshoot if the heavy-load condition disappears suddenly during start-up.

If there is already some voltage on the output during start-up or recovery from hiccup mode, this voltage is discharged by the negative current limit (I_{LIMIT}) (-1A in PWM mode, regardless of the MODE/SYNC setting) to equal V_{SS}. Then V_{OUT} rises normally.

MODE/SYNC Setting

The MPM4710 can be set to pulse-skip mode (PSM) or fixed-frequency PWM mode under light-load conditions by setting the MODE/SYNC pin. Pull MODE/SYNC high to have the device operate in fixed-frequency PWM mode. In this mode, the current conducts while I_L reverses direction. The V_{OUT} ripple is lower than in pulse-skip mode (PSM); however, the power loss is higher due to the high switching frequency (f_{SW}).

Pull MODE/SYNC low to have the device enter PSM automatically when the load decreases. In PSM, a group of switching pulses is initiated when the internal V_{C_BUCK} exceeds the PSM threshold. Group pulses start with SWA and SWC on, and end with SWB and SWD on. SWD turns off if the SWD current flows from VOUT to SW2 in each period.

During start-up or the short-circuit protection (SCP) recovery condition, the MPM4710 operates in fixed-frequency PWM mode, regardless of the MODE/SYNC setting. The negative I_L is limited to -1A, which is the same as in fixed-frequency PWM mode.

Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Two Current Limits

The MPM4710 has two peak current limits. One is a steady state switching I_{LIMIT} (I_{LIMIT_SW1}) (typically 4.2A), while the other is a start-up switching I_{LIMIT} (typically 2.5A). The start-up I_{LIMIT} (I_{LIMIT_SW2}) can control the input inrush current at lower levels when V_{FB} is below 60% of V_{REF} during start-up.

If an overload or short circuit occurs, V_{OUT} drops due to I_{LIMIT_SW1}. If V_{OUT} drops below 60% of its normal output, the MPM4710 stops switching and recovers after about 8ms with hiccup mode. After the switching stops in hiccup mode, V_{SS} is clamped at V_{FB} + 0.3V (where V_{FB} is the divided voltage from the residual V_{OUT}). This smooths V_{SS} when the MPM4710 recovers from hiccup mode.

During the soft-start time (t_{SS}), the MPM4710 blanks during hiccup mode for about 4ms. If V_{OUT} remains below 60% of the normal voltage after the 4ms blanking time, the MPM4710 resumes hiccup mode. If V_{OUT} exceeds 60% of the normal value, the MPM4710 resumes normal operation.

Power Good (PG) Indication

The PG pin is the open drain of a MOSFET that connects to VCC or a voltage source through a resistor (e.g. 100kΩ). Once V_{FB} reaches 91.5% of V_{REF}, PG pulls high. When V_{FB} drops to 76% of V_{REF}, PG pulls low.

PG has self-driving capability. If the MPM4710 is off and PG is pulled up to another DC power source through a resistor, PG can be pulled low

(about 0.7V) via the self-driving circuit.

Over-Voltage Protection (OVP)

If V_{OUT} exceeds 6V, the MPM4710 stops switching. This protects the device from high-voltage stress. Once V_{OUT} drops below 5.8V, switching recovers automatically.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. An internal temperature sensor continuously monitors the IC's junction temperature (T_J). If T_J exceeds the thermal shutdown threshold (160°C), the device shuts down. Once T_J falls below 140°C, the device initiates an SS to resume normal operation.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The resistor divider between VOUT and FB sets V_{OUT}. The high-side (HS) FB resistor (R1) can be calculated with Equation (1):

$$R1 = (\frac{V_{OUT}}{V_{FB}} - 1) \times R2 \quad (1)$$

Where R2 is the low-side (LS) FB resistor (typically between 60kΩ and 360kΩ to improve stability and transient response).

Selecting the Input and Output Capacitors

For stable operation, it is recommended to use low-ESR ceramic capacitors for the input and output capacitors to filter any disturbances in the input and output lines.

For the best performance, choose a >10µF input capacitors (C_{IN}) and >22µF output capacitors (C_{OUT}). C_{OUT} affects loop stability. Place the input and output capacitors as close to the device as possible. See the PCB Layout Guidelines section and the Typical Application Circuit section on page 15 for more details.

PCB Layout Guidelines [9]

Efficient PCB layout (especially of the high-frequency switching power supplies) is critical for stable operation. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place C_{IN} and C_{OUT} close to the VIN, VOUT, and PGND pins.
2. Place the ceramic capacitor, especially the small package size (0402) bypass capacitor, as close to the VOUT and PGND pins as possible to minimize high-frequency noise.
3. Place the VCC decoupling capacitor close to the VCC and AGND pins.
4. Keep the FB resistor divider close to the FB pin.
5. Ensure that the PGND, VIN, and VOUT copper layout is wide enough to conduct a high current and lower the die temperature.
6. Place multiple vias on the PGND copper around the IC to improve thermal performance.

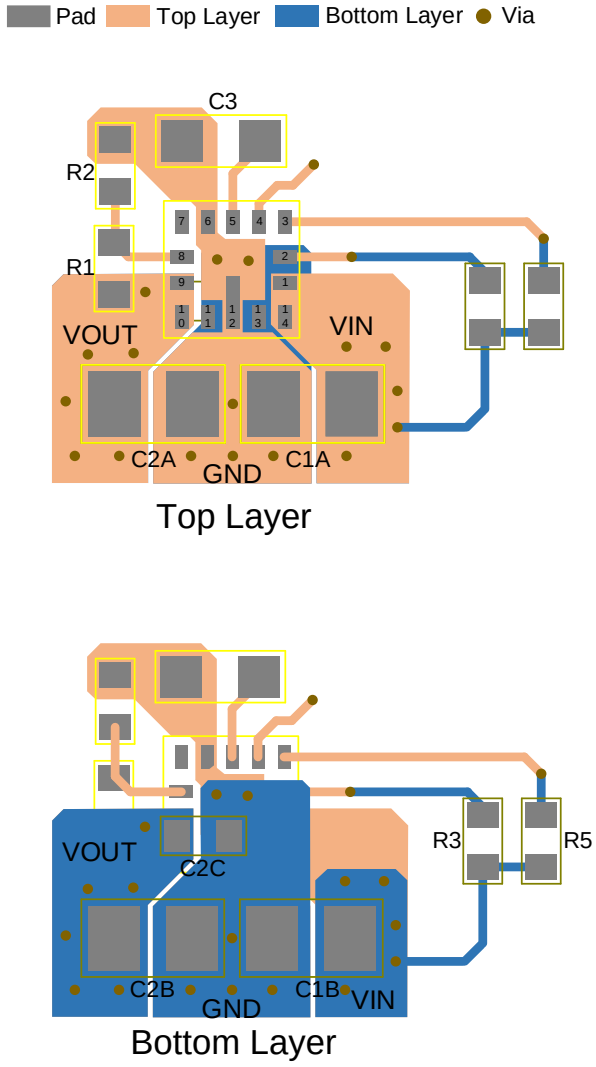


Figure 3: Recommended PCB Layout

Note:

10) The recommended PCB layout is based on Figure 4 on page 15.

TYPICAL APPLICATION CIRCUIT

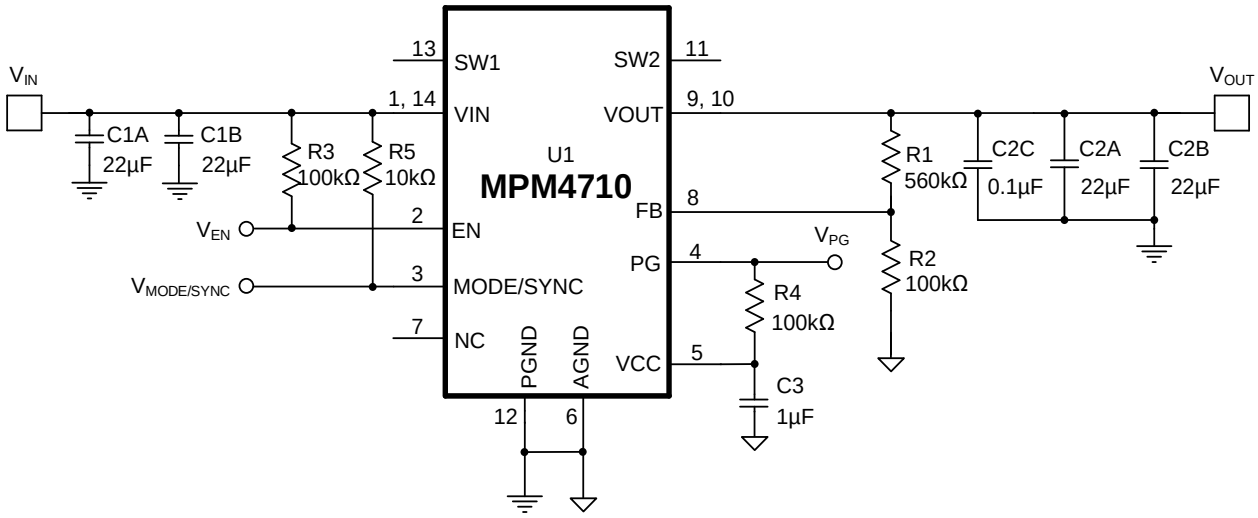
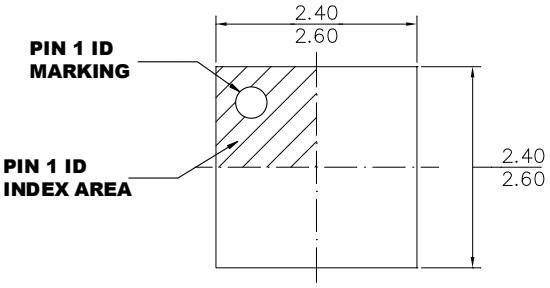


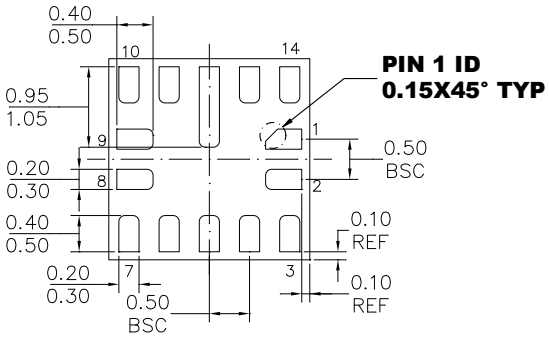
Figure 4: Typical Application Circuit (V_{OUT} = 3.3V)

PACKAGE INFORMATION

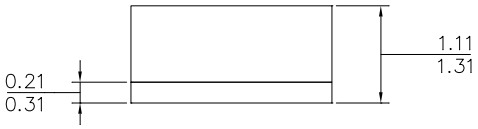
ECLGA-14 (2.5mmx2.5mmx1.2mm)



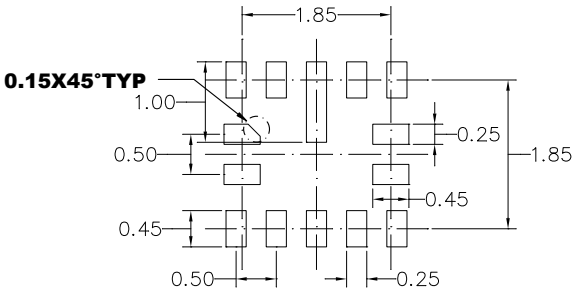
TOP VIEW



BOTTOM VIEW



SIDE VIEW

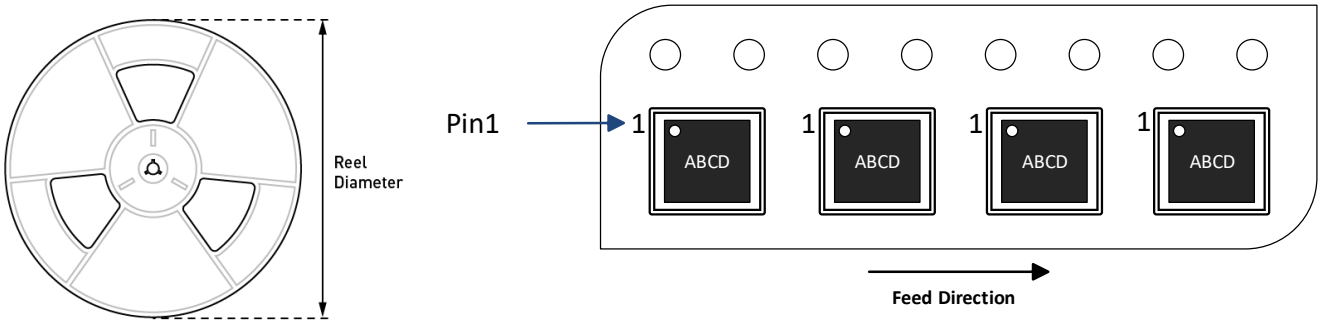


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantiy/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM4710GPA-Z	ECLGA (2.5mmx2.5mm x1.2mm)	2500	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/17/2023	Initial Release	-