SL6341D

USB 3.2 Gen1x1 HUB Controller

DataSheet

Doc Rev. 2.01
30.Dec.2024

Revision History

Revision	Date	Description	Reviser
1.00	2023/5/10	First Release	ljl
2.00	2024/9/22	SL6341D-QFN56-6x6 Package modification and update description for DCDC/LDO/Crystal etc.	ljl
2.01	2024/10/31	SL6341D Strapping pin for BC1.2 description update.	ljl

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Chapter 1 General Description

Corechip SL6341D is a 4-port, low-power, high-performance and configurable USB3.2 Gen 1x1 Hub Controller. It is compliant with the USB3.2 Revision 1.0 specification. SL6341D integrates USB3.0 Super Speed transmitter/receiver physical layer(PHY) and USB2.0 high speed PHY. It supports Super Speed, High Speed, Full Speed and Low Speed USB Connections and is fully compatible to all USB 3.0, USB2.0 and USB 1.1 hosts. The integrated 5V to 3.3V regulator enables SL6341D to be powered directly from 5V USB VBus, reducing BOM cost while offering high power efficiency.

SL6341D features the native fast-charging and complies with USB-IF battery charging specification Rev1.2, it could fast-charge Apple, Samsung Galaxy devices, and any device compliant with BC1.2/1.1. It also allows portable devices to draw up to 1.5A from SL6341D charging downstream ports (CDP1) or dedicated charging port (DCP2). It can also enable systems to fast charge handheld devices even during “Sleep” and “Power-off” states. The BC1.2 Feature is disabled by default, Customers can modify the strapping pin for configuring it enabled.

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1 CDP, charging downstream port, the Battery Charging Rev.1.2-compliant USB port that does data communication and charges device up to 1.5A.

2 DCP, dedicated charging port, the Battery Charging Rev.1.2-compliant USB port that only charges devices up to 1.5A, similar to wall chargers.

Chapter 2 Features

2.1 Compliant with USB 3.2 Specification Revision 1.0

- Upstream port supports super speed(SS) high speed(HS) and full speed(FS) traffic
- Downstream ports support SS, HS, FS, and low speed(LS) traffic
- 1 control pipe and 1 interrupt pipe
- Backward compatible to USB specification Revision 2.0/1.1

2.2 Featuring fast-charging on all downstream ports

- Compliant with USB Battery Charging Revision v1.2, supporting SDP(Standard Downstream Port), CDP, DCP, and ACA-Dock
- Downstream ports can be turned from a Standard Downstream Port (SDP) into Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)
- Downstream devices can be charged while upstream VBUS is not present, which can be applied on wall charger applications

2.3 On-chip 32-bit micro-processor

- RISC-like architecture
- 1 cycle instruction execution (maximum)
- Performance: 6 MIPS @ 24MHz (maximum)
- With 4K-byte RAM, 4K-byte internal ROM

2.4 Integrated USB transceiver

- Improving output drivers with slew-rate control for EMI reduction
- Internal power-fail detection for ESD recovery
- Integrated USB3.2 Gen 1x1 transceiver and USB 2.0 transceiver

2.5 Advanced power management and low power consumption

- Supporting USB3.0 U0/U1/U2/U3 power management states
- Supporting USB2.0 suspend and resume
- Supporting individual/gang mode over-current detection for all downstream ports
- Supporting individual/gang mode power-enable for all downstream ports

2.6 Configurable settings by SPI-flash/EEPROM/pin strapping

- Configurable BC1.2 charging function

- Supporting full in-system programming firmware upgrade by SPI-flash and EEPROM

- Supporting compound-device (non-removable setting on downstream ports)

- Supporting customization VID/PID(for USB.30 and USB2.0 independently)

- Configurable 1-wire, 3-wires, 4-wires led mode for downstream ports (SL6341B supported)

*SL6341x means SL6341 serialized package chip, ask sales for more.

2.7 Flexible design

- Automatic switching between self-powered and bus-powered modes

- Supporting PHY tuning

- Supporting register setting by firmware

- Allow downstream ports to connect up to 8 devices, 4 x USB3.0 non-removable devices with 4 x USB2.0 non-removable devices or exposed ports

2.8 Low BOM cost

- Single external 24 MHz crystal / Oscillator clock input

- Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors

- Built-in 5 to 3.3V LDO regulator

2.9 Available package type

SL6341D --- QFN 56 (6mmx6mm-0.35mm)

2.10 Applications

- Standalone USB hub/Docking station

- Tablet/Ultrabook/NB

- Motherboard

- Monitor built-in hub, SL6341x GPIOs can be programmed as I2C interface to easily update scalar firmware through USB interface

- TV built-in hub

- Compound device, such as hub-reader application

- USB wall charger

- Other consumer electronics

- Customized applications

Dynamically disable/enable ports

GPIO signaling of ambient light sensor or rotation/position sensor

Chapter 3 Block Diagram

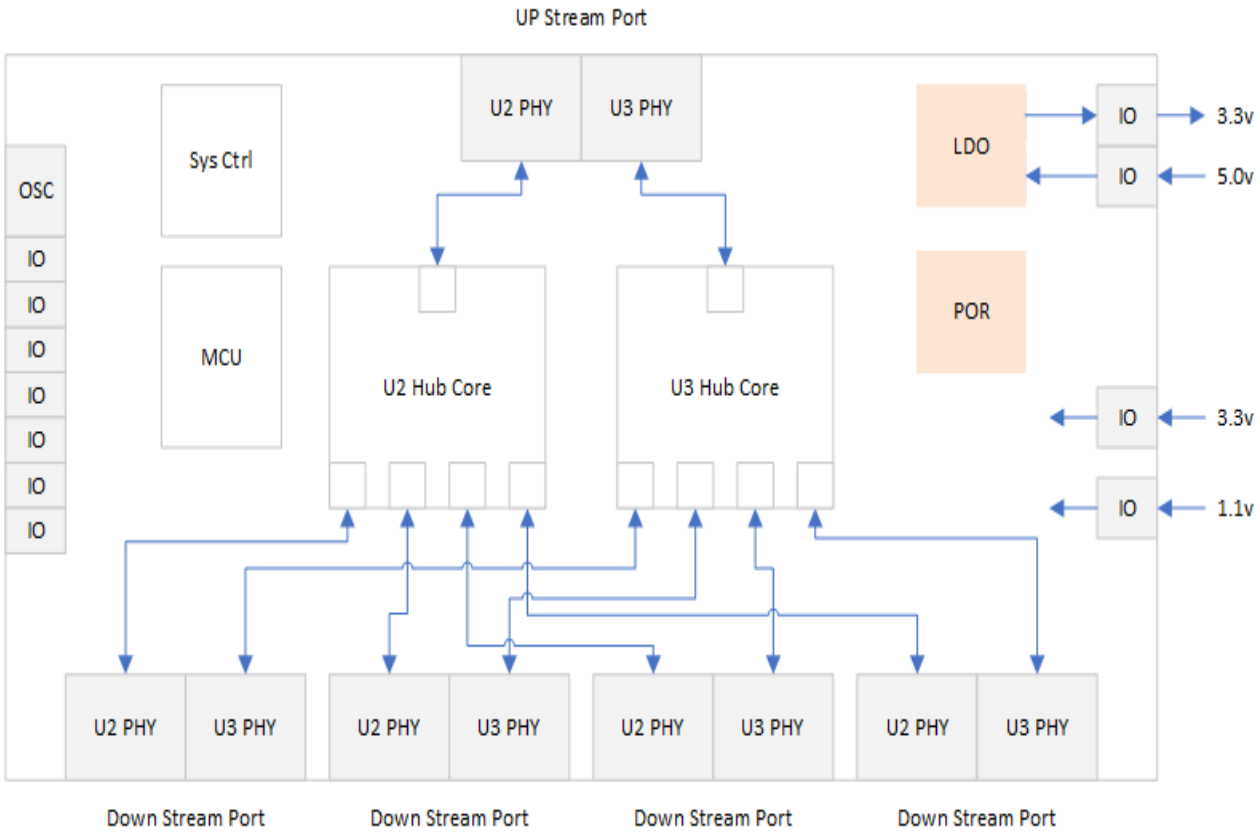


Figure 3.1 – SL6341D Block Diagram

Chapter 4 PIN ASSIGNMENT

4.1 Pinout

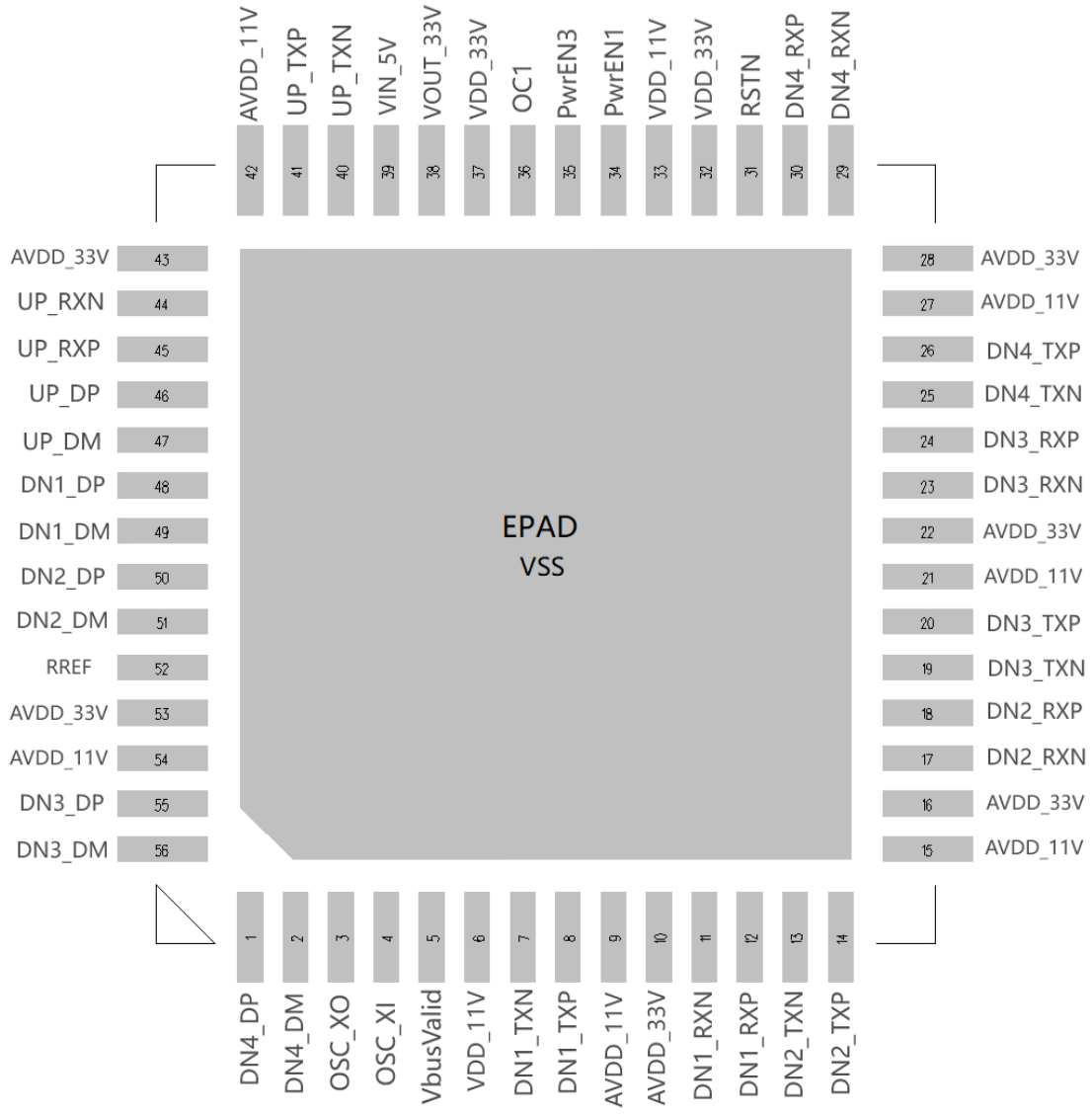


Figure 4.1 – SL6341D QFN56(6x6-0.35) Pin out Diagram

4.2 Pin Description

Table 4.2.1 USB2.0 Interface

SL6341D	PinName	Type	Description
46	UP_DP	B	USB2.0 DP for Upstream Port
47	UP_DM	B	USB2.0 DM for Upstream Port
48	DN1_DP	B	USB2.0 DP for Downstream Port 1
49	DN1_DM	B	USB2.0 DM for Downstream Port1
50	DN2_DP	B	USB2.0 DP for Downstream Port 2
51	DN2_DM	B	USB2.0 DM for Downstream Port2
55	DN3_DP	B	USB2.0 DP for Downstream Port 3
56	DN3_DM	B	USB2.0 DM for Downstream Port3
1	DN4_DP	B	USB2.0 DP for Downstream Port 4
2	DN4_DM	B	USB2.0 DM for Downstream Port4
52	RREF	I	USB2.0 Reference Input, connect to 200ohm 1% Resister

Table 4.2.2 USB3.2 Gen1 Interface

SL6341D	PinName	Type	Description
40	UP_TXN	O	USB3.0 Differential Data Receiver Tx- for Upstream Port
41	UP_TXP	O	USB3.0 Differential Data Receiver Tx+ for Upstream Port
44	UP_RXN	I	USB3.0 Differential Data Transmitter Rx- for Upstream Port
45	UP_RXP	I	USB3.0 Differential Data Transmitter Rx+ for Upstream Port
7	DN1_TXN	O	USB3.0 Differential Data Receiver Tx- for Downstream Port1
8	DN1_TXP	O	USB3.0 Differential Data Receiver Tx+ for Downstream Port1
11	DN1_RXN	I	USB3.0 Differential Data Receiver Rx- for Downstream Port1
12	DN1_RXP	I	USB3.0 Differential Data Receiver Rx+ for Downstream Port1
13	DN2_TXN	O	USB3.0 Differential Data Receiver Tx- for Downstream Port2
14	DN2_TXP	O	USB3.0 Differential Data Receiver Tx+ for Downstream Port2
17	DN2_RXN	I	USB3.0 Differential Data Receiver Rx- for Downstream Port2
18	DN2_RX	I	USB3.0 Differential Data Receiver Rx+ for Downstream

	P		Port2
19	DN3_TXN	O	USB3.0 Differential Data Receiver Tx- for Downstream Port3
20	DN3_TXP	O	USB3.0 Differential Data Receiver Tx+ for Downstream Port3
23	DN3_RXN	I	USB3.0 Differential Data Receiver Rx- for Downstream Port3
24	DN3_RXP	I	USB3.0 Differential Data Receiver Rx+ for Downstream Port3
25	DN4_TXN	O	USB3.0 Differential Data Receiver Tx- for Downstream Port4
26	DN4_TXP	O	USB3.0 Differential Data Receiver Tx+ for Downstream Port4
29	DN4_RXN	I	USB3.0 Differential Data Receiver Rx- for Downstream Port4
30	DN4_RXP	I	USB3.0 Differential Data Receiver Rx+ for Downstream Port4

Table 4.2.3 OSC & Reset

SL6341D	PinName	Type	Description
---	TE	I	Test Enable
4	OSC_XI	I	Crystal/OSC Clock input
3	OSC_XO	O	Crystal Clock output
31	RSTN	I	Reset input, Active Low

Table 4.2.4 Digital GPIOs Interface

SL6341D	PinName	Type	Description
---	PwrMode	B/PU	Power Mode Selection, It is also the power mode indicator 0 : Set Hub to BusPower Mode 1 : Set Hub to SelfPower Mode (default)
5	VbusValid	I/PD	Vbus Valid or invalid Selection, Determined by external circuit. 0 : Set Hub to be VbusInvalid State(default) 1 : Set Hub to be VbusValid State
---	DBG_TXD	O/PU	Debug uart Tx Pin

---	DBG_RXD	I/PU	Debug uart Rx Pin
---	SPI_CS	O/PU	Strapping stage : Mcu Enable 1 : enable internal Mcu(default) 0 : disable internal Mcu Normal stage : spi chip selection signal
---	SPI_CLK	B/PU	Spi clock signal
---	SPI_MOSI	O/PD	Strapping stage : mcu IIC or spi selection 1 : iic eeprom 0 : spi flash (default) Normal stage : spi Master Output Slave Input signal
---	SPI_MISO	I/PU	Spi Master Input Slave Output signal
---	LED4	O/PD	Strapping stage : DnPort4 non-removable setting bit 1 : Connected non-removable device under DnPort4 0 : No non-removable device under DnPort4 (default) Normal stage : LED4, not used under 3-wire or 1-wire mode 1 : light on LED4 for DnPort 4 when 4-wire mode 0 : light off LED4 for DnPort 4 when 4-wire mode
---	LED3	O/PD	Strapping stage : DnPort3 non-removable setting bit 1 : Connected non-removable device under DnPort3 0 : No non-removable device under DnPort3 (default) Normal stage : LED3, when under 3-wire mode, It is the LED_DRV signal, not used under 1-wire mode 1 : light on LED3 for DnPort 3 when 4-wire mode 0 : light off LED3 for DnPort 3 when 4-wire mode
---	LED2	O/PD	Strapping stage : DnPort2 non-removable setting bit 1 : Connected non-removable device under DnPort2 0 : No non-removable device under DnPort2 (default) Normal stage : LED2, when under 3-wire mode, It is the LED2 signal for 3-wire mode, not used under 1-wire mode 1 : light on LED2 for DnPort 2 when 4-wire mode 0 : light off LED2 for DnPort 2 when 4-wire mode
---	LED1	O/PD	Strapping stage : DnPort1 non-removable setting bit 1 : Connected non-removable device under DnPort1 0 : No non-removable device under DnPort1 (default) Normal stage : LED1, when under 3-wire mode, It is the LED1 signal for 3-wire mode, It is also the LED1 signal under 1-wire mode 1 : light on LED1 for DnPort 1 when 4-wire mode 0 : light off LED1 for DnPort 1 when 4-wire mode
---	OC4	I/PU	Over Current indicator for downstream port 4
---	OC3	I/PU	Over Current indicator for downstream port 3
---	OC2	I/PU	Over Current indicator for downstream port 2

36	OC1	I/PU	Over Current indicator for downstream port 1 (The only OC indicator under gang mode)
---	PwrEn4	O/P D	Strapping stage : gang/individual mode setting 0 : gang mode enabled (default) 1 : individual mode enabled Normal stage : power enable output for downstream port 4 1 : output power enable as high level 0 : output power enable as low level
35	PwrEn3	O/P D	Strapping stage : BC1.2 Charger enable 0 : disable BC1.2 Charger function (default) 1 : enable BC1.2 Charger function Normal stage : power enable output for downstream port 3 1 : output power enable as high level 0 : output power enable as low level
---	PwrEn2	O/P D	Strapping stage : dummy1(Reserved for later use) Normal stage : power enable output for downstream port 2 1 : output power enable as high level 0 : output power enable as low level
34	PwrEn1	O/P D	Strapping stage : dummy0(Reserved for later use) Normal stage : power enable output for downstream port 1 (The only PwrEn output under gang mode) 1 : output power enable as high level 0 : output power enable as low level

Table 4.2.5 Power Domain

SL6341D	PinName	Type	Description
39	VIN_5V	I	5v Adapter Input or Vbus input
38	VOUT_33V	O	3.3v Power Output
53,10,16,22,28,43	AVDD_33V	I	3.3v Analog power
54,9,15,21,27,42	AVDD_11V	I	1.1v Analog power
32,37	VDD_33V	I	3.3v Digital power
6,33	VDD_11V	I	1.1v Digital power
---	VSS	-	GND
57	EPAD	P	EPAD

4.3 Notation Type:

O Output

I Input

B Bi-directional

P Power / Ground

A Analog

PU Internal pull up

PD Internal pull down

Chapter 5 Electrical Characteristics

5.1 Maximum Ratings

Table 5.1–Maximum Ratings

Absolute Maximum Rating					
Symbol	Parameter	Min	Max	Unit	Note
Ts	Storage Temperature	-55	150	℃	
Tj	Junction Temperature	-40	125	℃	
VDD50	5V Input Voltage	-0.3	5.5	V	LDO : -0.5 ~ 5.5
VDD33	3.3V LDO Output Voltage	-0.5	3.96	V	U2/U3 : -0.66 ~ 3.96 IO : -0.5 ~ 3.8
VDD11	1.1V DCDC Input Voltage(External Input)	-0.22	1.32	V	U2/U3 : -0.22 ~ 1.32 IO : -0.5 ~ 1.8
Vin	Input Voltage at I/O pins	-0.5	3.8	V	GPIO PIN
Vout	Output Voltage at I/O pins	-0.5	3.8	V	GPIO PIN
Pd	Power Dissipation	---	1	W	
Vesd	Electrostatic Discharge	-2000	2000	V	HBM 1C Level
I_{latch}	Latch Up Current	---	100	mA	

5.2 Operating Ratings

Table 5.2 – Operating Condition

Operating Condition					
Symbol	Parameter	Min	Typ	Max	Unit
Ta	Operating Ambient Temperature	-40	---	85	℃
VDD50	5V Input Voltage for LDO	4.5	5	5.5	V
VDD33	3.3V LDO Output Voltage	2.97	3.3	3.63	V
VDD11	1.1V DCDC Input Voltage(External Input)	0.99	1.1	1.21	V

5.3 DC Characteristics

5.3.1 DC Characteristics except USB Signals

Table 5.3 – DC Characteristics except USB Signals

DC Characteristics except USB Signals					
Symbol	Parameter	Min	Typ	Max	Unit
VDD_IO	Digital Input IO Voltage	2.97	3.3	3.63	V
VDD_CORE	Digital Input Core Voltage	0.99	1.1	1.21	V
V_{IL}	Digital IO Input Low Voltage	-0.3	0	0.8	V
V_{IH}	Digital IO Input High Voltage	2	3.3	3.63	V
V_{oL}	Digital IO Output Low Voltage	---	0	0.4	V
V_{OH}	Digital IO Output High Voltage	2.4	3.3	3.63	V
I_{oL}	Digital Low Level Output Current	---	12	---	mA
I_{OH}	Digital High Level Output Current	---	12	---	mA
I_L	Input Leakage Current	-10	---	10	uA
I_{OZ}	Tri-State Output Leakage Current	-10	---	10	uA
R_{PU}	Internal Pull-up Resistor	27	40	64	KΩ
R_{PD}	Internal Pull-down Resistor	30	46	80	KΩ

5.3.2 USB 2.0 Interface DC Characteristics

The SL6341D conforms to DC characteristics for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

5.3.3 USB 3.0 Interface DC Characteristics

The SL6341D conforms to DC characteristics for Universal Serial Bus specification rev.3.0. Please refer to this specification for more information.

5.4 AC Characteristics

Table 5.4 –AC Characteristics：System Clock

AC Characteristics：System Clock					
Symbol	Parameter	Min	Typ	Max	Unit
F_{clk}	Clock Frequency	-20	24M	20	ppm
C1, C2	Load Capacitance	---	12~15	---	pF
ESR	Max equivalent series resistance	---	40	---	Ω

5.5 Power Consumption

SL6341D integrates 5V-to-3.3V LDO regulator. If supplying 5V power, internal regulators convert 5V to 3.3V, Users should use external DCDC for 1.1V supplier. The following 5V(work as Vbus) Power consumption includes the internal LDO and external DCDC power consumption and conversion loss. In other words, if using 5V as input power, 1.2V and 3.3V power can be ignored; if using external 1.2V and 3.3V power as input sources, the total power consumption will be the sum of 1.2V and 3.3V (LDO/DCDC itself's power consumptions are not included under this condition)

Table 5.5 – Power Consumptions for SL6341D

Number Of Active USB3.1 Ports	Using 5V Vbus Power Input		Using 1.1V&3.3V Power Input				Unit
	5V		1.1V		3.3V		
	Config	R/W	Config	R/W	Config	R/W	
Suspend	40.3		23.5		12.8		mW
1	276	363	99	169	84	84	mW
2	370	486	199	226	120	120	mW
3	536	603	253	284	156	156	mW
4	622	740	310	343	192	192	mW

Number Of Active USB2.0 Ports	Using 5V Vbus Power Input		Using 1.1V&3.3V Power Input				Unit
	5V		1.1V		3.3V		
	Config	R/W	Config	R/W	Config	R/W	
Suspend	40.3		23.5		12.8		mW
1	102	114	34	39	27	33	mW
2	113	156	35	54	34	43	mW
3	126	194	37	66	40	55	mW
4	138	230	39	82	46	69	mW

Note :

1. Config State is entered when insert the U2/U3 Device without data transferring.
2. R/W State is entered when insert the U2/U3 Device and using AJA for data transferring.
3. The test result represents silicon level operating current without considering additional power consumption contributed by external circuit. The power consumption could be different depending on configurations.

Chapter 6 Function Description

6.1 Strapping Pin

There are several pins with Strapping function as Table 6.1 showing. Strapping Pins are under work when the chip is during the POR(Power On Reset State), the chip will sample the strapping pin signal as a configuration for some function setting. There are some Pull-up or Pull-down resister internal by default that will determine the default strapping pin value. If another value wants to be set, the external Pull-up or Pull-down resister could be used. And a POR or re-power should be applied for the setting work properly.

Table 6.1 -Strapping Pin List for SL6341D(QFN56)

*More Pin Strapping Function SL6341x needed.

Pin	Normal	Strapping	Default Val	Strapping Function Description
5	VbusValid	VbusValid	0	0：VbusValid is under invalid state 1：VbusValid is under valid state
35	PwrEN3	BC1.2 ChargerEnable	0	0：Disable BC1.2 Function 1：Enable BC1.2 Function
34	PwrEn1	Dummy0	0	Reserved

6.2 self power or bus power

The USB system software examines hub descriptor information to determine the hub's characteristics. By examining the hub's characteristics, the USB system software ensures that illegal power topologies are not allowed by not powering on the hub's ports if doing so would violate the USB power topology. The device status and configuration information can be used to determine whether the hub can be used in a given topology.

The *MaxPower* field in the configuration descriptor is used to report to the system the maximum power the hub will draw from USB power when the configuration is selected. The external devices attaching to the hub will report their individual power requirements. Software shall ensure that at least ONE UNIT LOAD(150mA for USB3.0 spec) is available for each exposed downstream port on a bus powered hub.

The *bmAttributes* field in the configuration descriptor is used to report to the system the power required from local power source or bus. And the value of power is derived from *MaxPower* field.

The actual power source at runtime may be determined using the GetStatus(DEVICE) request.

Table 6.2 - Standard Configuration Descriptor

Standard Configuration Descriptor				
Offset	Field	Size	Value	Description

7(Byte8)	bmAttributes	1	Bitmap	Configuration characteristics: D7: Reserved (set to one) D6: Self-powered D5: Remote Wakeup D4...0: Reserved (reset to zero) A device configuration that uses power from the bus and a local source reports a non-zero value in bMaxPower to indicate the amount of bus power required and sets D6. The actual power source at runtime may be determined using the GetStatus(DEVICE) request. If a device configuration supports remote wakeup, D5 is set to one.
8(Byte9)	bMaxPower	1	mA	Maximum power consumption of the device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units when the device is operating in HS mode and in 8 mA units when operating at GenX speed. Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered or not. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it shall return to the Powered state.

The GetStatus() request will return the runtime device status. The request is as following :

bmRequestType	bRequest	wValue		wIndex	wLength	Data
100000000b	GET_STATUS	Zero	Standard_Status_Type	Zero	2	Device Status

Table 6.3 – GetStatus() device status

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			LTM Enable	U2 Enable	U1 Enable	Remote Wakeup	Self-Powered
D15	D14	D13	D12	D11	D10	D9	D8
Reserved							

The *Self Powered* field indicates whether the device is currently self-powered or not. If D0 is reset to zero, the device is bus-powered. If D0 is set to one, the device is self -powered. The *Self-Powered* field may not be changed by the SetFeature() or ClearFeature() requests.

SL6341D BusPowered mode and SelfPowered mode relative settings : For SL6341D, SelfPowered Mode is always available and BusPowered Mode is disabled.

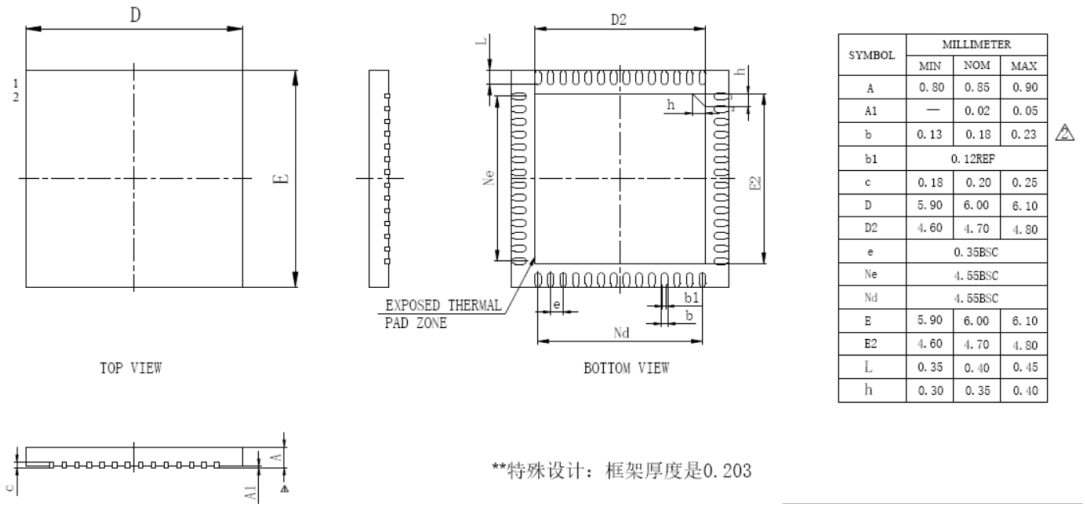
6.3 On-Chip Power Regulator

SL6341D requires 3.3V and 1.1V source power for normal operation of internal core logic and USB physical layer (PHY). SL6341D integrates one low-drop power regulator(LDO) which converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source; and the 1.1V core power should be supplied by external chip. The main features for the LDO chip just as following :

Feature	value
Input Power Range	4.5V ~ 5.5V
Current Driving Cap	300mA@max
Low Power Consumption	85uA w/o loading
Current short Protection	450mA@typical

LDO inputs The regulators' maximum currents loading are 300mA (5-3.3V) which provide enough tolerance for normal SL6341D operation (below 100mA).

Chapter 7 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	—	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.60	4.70	4.80
e	0.35BSC		
Ne	4.55BSC		
Nd	4.55BSC		
E	5.90	6.00	6.10
E2	4.60	4.70	4.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 7.1 – SL6341D QFN56 (6x6x0.85-0.35) Package

Figure 7.2 – Package Top Size Marking